Ruby B. Lee

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RESEARCH INTERESTS

Instruction-set architecture, multimedia architecture, security architecture, computer architecture. High-performance microprocessors. Media processor architectures. Security architecture for wireless Internet, virtual private networks, privacy, and intellectual property protection; cryptography acceleration. Technology for interconnected information appliances, servers and infrastructures. Theory of efficient permutations. Designing societal values into technology infrastructures and architectures.

EDUCATION

- Ph.D. in Electrical Engineering (minor in Computer Science), Stanford University, Stanford, California, June 1980.
- M.S. in Computer Science and Computer Engineering, Stanford University, Stanford, California, June 1975.
- A.B. (with distinction) in Computer Science and Comparative Literature, College Scholar program, Cornell University, June 1973.

APPOINTMENTS

- Forrest G. Hamrick Professor in Engineering and Professor of Electrical Engineering, with an affiliated appointment in Computer Science, Princeton University, September 1998 - present. Director and founder of the Princeton Architecture Lab for Multimedia and Security, 2001-present.
- Consulting Professor of Electrical Engineering, Stanford University, 1995-1998, Consulting Associate Professor of Electrical Engineering, Stanford University, 1989-1995.
- Hewlett-Packard Company, Sept. 1981 - Aug. 1998 (full-time employment concurrent with above consulting professor appointments). Chief architect, '92-'98. Lead Architect, '90-92. Manager, microprocessor design '86-'89. Lead microprocessor designer, '84-'86. Computer architect, '81-'84.
- Acting Assistant Professor of Electrical Engineering, Stanford University, 1980-1981.

INDUSTRIAL EXPERIENCE

Sept 1981 to Sept 1998 **Computer Architect, Hewlett-Packard Company (HP).** Different positions within HP are summarized below.

Sept 1997 to Sept 1998 **Chief Architect, Enterprise Systems Group, HP Cupertino.** Formed and led an inter-divisional Security Architecture Team for e-commerce and extended enterprises, to help define HP's security strategy and design the underlying architectural framework at the extended enterprise, platform, and hardware levels.

May 1992 to Sept 1997 **Chief Architect, Computer Systems Organization, HP Cupertino.** Responsibilities included the evolution of HP's PA-RISC processor architecture for HP-UX workstations and servers: PA-RISC 1.0, PA-RISC 1.1 and PA-RISC 2.0. Chief architect of a cross-functional multimedia architecture team, which pioneered real-time media processing, e.g., MPEG1 video/audio decoding, in software (with Mpower multimedia user interface). Architected the PA-RISC Multimedia Acceleration eXtensions, MAX-1 and MAX-2 – first multimedia instructions in general-purpose processors. Co-led an HP-Intel architecture team for IA-64 (EPIC) architecture.

Jan 1990 to May 1992 **Lead Architect, Information Architecture Group, HP Cupertino.** Involved in a special team commissioned to assimilate the Apollo technology (after its acquisition by HP), resulting in cross-country and cross-disciplinary teamwork and leadership products, such as the HP9000/700 "Snakes" workstations.

Oct 1989 to Feb 1990 **Research Grants Program, Information Architecture Group, HP.** Promoted and evaluated research requests from universities, including requests for HP equipment donations. Also evaluated HP investments in startup companies.

Nov 1986 to Sept 1989 **Project Manager, Computer Systems Group, HP.** Managed a VLSI processor design team, for a PA-RISC processor in full-custom CMOS. This single-chip processor included on-chip memory-management and caches, instruction prefetching and streaming, and support for cache-coherent multiprocessors, external caches, external second-level TLBs, and coprocessors. Responsible for design and verification, and also section-wide planning, scheduling and monitoring.

April 1984 to Oct 1986 — **Technical Lead, Stirling Processor Design, HP Labs.** Lead system/ logic designer of first CMOS, low-cost, PA-RISC microprocessor. Responsible for system design, pipeline design, bus definition, testability design, control unit implementation, some verification and silicon bringup.

Jan 1983 to March 1984 — **System Designer, SPECTRUM Program, HP Labs.** Investigated fault-tolerant processors, embedded controllers and $5K workstations.

Sept 1981 to March 1983 — **Computer Architect, SPECTRUM (PA-RISC) Program, HP Labs.** Founding member of the SPECTRUM program, now called PA-RISC, the core processor technology used in the HP9000 UNIX workstations and servers, the HP3000 MPE/iX servers, and the HP1000 real-time controllers. Promoted the streamlined RISC approach with pathlength reduction features in the PA-RISC processor architecture, with key contributions in branch optimizations, memory addressing, cache hints, pipeline design, interrupt handling, performance estimations and methodology, instruction-set design and encoding, and hardware feasibility studies in different technologies. Also architected the PA Assists architecture (including the floating-point coprocessor) and Real-mode PA for embedded processors.

June 1976 to Aug 1976 — **Graduate Research Associate, IBM Research Lab, San Jose.** Worked on a graphical interface to a relational database system.

ACADEMIC EXPERIENCE

Sept 1998 to present — **Forrest G. Hamrick Professor in Engineering and Professor of Electrical Engineering, Princeton University.** Affiliated appointment in the Computer Science department.

My research is currently focussed on architectures with very high performance multimedia and secure information processing, for Internet information appliances and servers. I teach a new graduate course in *Processor Architectures for New Paradigms*, and a revised undergraduate course in *Computer Architecture*. Founder and Director of the Princeton Architecture Lab for Multimedia and Security (PALMS), from 2001.

Sept 1995 to Sept 1998 — **Consulting Professor of Electrical Engineering, Stanford University.** See below.

Sept 1989 to Sept 1995

(concurrent with HP employment)

Consulting Associate Professor of Electrical Engineering, Stanford University. Thesis co-advisor for Ph.D. students. Taught graduate computer architecture and organization courses, once every few years, with some team-teaching in-between. Supervision of independent research projects. Participated in DASH multiprocessor, SNAP arithmetic, and Flynn's computer architecture research groups. Provided career guidance and research ideas for students.

Courses taught:

Advanced Computer Architecture (EE486)
Advanced Computer Organization (EE482)
Special Studies and Reports in Electrical Engr. (EE391)

Jan 1990 to Jan 1992
(concurrent with HP employment)

HP Industrial Liaison to Stanford Center for Integrated Systems. Provided HP with greater awareness of Stanford research, resulting in increased HP funding, e.g., HP fabricating gratis a Stanford SNAP floating-point chip.

June 1980 to Aug 1981

Acting Assistant Professor of Electrical Engineering, Stanford University. Taught introductory and advanced graduate computer architecture courses. Research in hardwired dataflow, novel VLSI architectures, systolic arrays, parallel architectures, bus design and instruction-set design. Consulted on parallel processors.

Courses taught:

Computer System Design (EE282)
Highly Parallel Computer Architectures (EE701)
Special Studies and Reports in Electrical Engr. (EE391)
Computer Architecture Seminar (EE385b)

Sept 1975 to June 1980

Research Assistant, Stanford University. Research in parallel processors, and various computer architecture topics. Maternity leave-of -absence in 1977.

Sept 1973 to June 1975

Teaching Assistant, Stanford University.

Courses assisted:

Introductory Programming
Systems Programming
Advanced Computer Organization.

PRINCETON SERVICE AND COMMITTEES:

- Council of the Princeton University Community elected committee member, 2001-2004, elected executive committee member 2001-2002.
- Faculty Advisory Committee on Policy, 2001-2002.
- President's task force on the Status of Women Faculty in Science and Engineering, 2001-.
- Electrical Engineering Department, Computer Engineering Coordinator, 2001-.
- Princeton University Faculty Hiring Committee for under-represented groups in Science and Engineering, chaired by Dean of Faculty, 2001.
- Undergraduate Adviser to the EE senior class of 2002, in 2001-2002.
- Princeton presidential team member to 9 universities' Presidents' summit at MIT on Gender Inequities for Women Faculty in Science and Engineering, Jan 2001.
- Advisory Board member for Princeton University Center for Arts and Cultural Policy Studies, Woodrow Wilson School for Public and International Affairs, 2000-present.
- Invited to speak to School of Engineering and Applied Sciences Advisory Board annual meeting, "Security in Internet and Wireless Transactions", April 20, 2000.
- Undergraduate Adviser to the EE class of 2002, in 2000-2001.
- Committee member, EE department external outreach committee, 1999-2000.
- Committee member, EE faculty search committee, 1999.
- Inter-disciplinary committee for establishing a new Luce Professorship in Information Technology, Consciousness and Culture at Princeton University, 1999-2001. (Approved by Luce foundation – faculty search in progress).
- Committee Member, Electrical Engineering Department Strategic Planning Committee, Steve Forrest (chair), 1998-1999. Co-authored a document, "The Department of Electrical Engineering: Initiatives in Engineering Research and Education for the 21st Century: A Strategic Plan", May 1999. Plan endorsed and being implemented.
- Chair of EE Computer Engineering junior faculty search committee, 1998-2000.
- Undergraduate Adviser to the EE class of 2002, in 1999-2000.
- Invited by Provost's office to speak at the new faculty orientation, September 1999, on "Princeton through New Eyes".
- Invited to speak to both undergraduate and graduate women in science and engineering, 1998-2001.
- Invited to speak to alumni, "Defining the Engines of the Information Age", May 1999.

PRINCETON COURSES TAUGHT:

Spring 1999:	ELE 580a: Advanced Topics in Computer Engineering: Processor Architectures for New Paradigms (overall rating: 4.5/5.0).
Fall 1999:	ELE 475: Computer Architecture
	ELE 497: Senior Independent Work
Spring 2000:	ELE 572: Processor Architectures for New Paradigms (overall rating 4.4/5)
	ELE 330: Multimedia and its Impact in the Next Millennium (team teaching)
Fall 2000:	ELE 475: Computer Architecture (overall rating 4.4/5)

Spring 2001: ELE 572: Processor Architectures for New Paradigms
ELE 330: Multimedia and its Impact in the Next Millennium (team teaching)
Fall 2001. ELE 475: Computer Architecture.
ELE 497: Senior Independent Work (5 seniors)

PAST STUDENTS

- Daniel Zucker, Ph.D. in Electrical Engineering, Stanford University, June 1997, "Architecture and Arithmetic for Multimedia Enhanced Processors".
  Co-advisor with Prof. Michael Flynn.
  Current position: Chief Technology Officer, ePocrates, Inc., California.
- Alice Yu, Ph.D. in Electrical Engineering, Stanford University, December 2001, "Improvement of Video Coding Efficiency for Multimedia Processing".
  Co-advisor with Prof. Michael Flynn.

Also:

- Joseph Bracken, M.S. in Electrical Engineering, Princeton University, November 2000. "Adding Security to the MP3 Algorithm". Law school, fall 2001.
- Abdulla Bubshait, M.S. in Electrical Engineering, Princeton University, June 2001. "Multiplication in Public Key Cryptography".
- Keigo Hirakawa, B.S. in E.E., June 2000. "Measuring Impact: Putting the Efficiency of SIMD Architecture on the Line".
- Marc Yun, B.S. in E.E., June 2000. "Study of Secure Digital Audio Formats for Consumer Playback of Electronically-Distributed Music".

CURRENT PH.D. STUDENTS

Current Ph.D. candidates in Electrical Engineering, Princeton University:

1. Zhijie Shi (passed general examinations Spring 1999)
2. Xiao Yang (passed general examinations Spring 2000)
3. John Patrick McGregor (passed general examinations, Fall 2000), HP scholar
4. Ahmet Murat Fiskiran (passed general examinations, Spring 2001), Kodak Fellow
5. David Karig (passed generals part 1), Department of Defense Fellow
6. Ioannis Avramopoulos (passed generals part 1) – on leave 2000.

Current Masters and Bachelors thesis advisees:

- Mitsuhiro Miyazaki (M.S.E.E.)
- Michael Cohen
- Aaron Cunningham
- Ian Lampl
- Ganesh Ramayanarayan

CONSULTING ACTIVITIES:

- Scientific Advisory Board, Inductive Devices, Inc., Pasadena, California, 2001.
- Scientific Advisory Board, Mindspeak, Inc., Princeton, New Jersey, 2001.
- Founder and Chairman of the Board, Teleputers, LLC, Princeton, New Jersey, 2001.
- Scientific Advisory Board, Fullcomm, 2000.
- Consultant, Hewlett-Packard Company, 1998, 1999.
- Consultant, Silicon Magic, Inc., 1999.
- Consultant, PicoTurbo, 1999.

PROFESSIONAL ACTIVITIES:

- Fellow of ACM, October 2001.
- Program Co-chair, IEEE ICCD 2001.
- Associate Editor-in-Chief, IEEE Micro. 2001.
- Program Co-chair, IEEE ICCD 2000.
- Referee for technical journal and conference papers, including ASPLOS 2000, ISCA 2000, ICCD 2000, HPCA 2000, ARITH 2000, ASAP 2000, IEEE Transactions on Multimedia, Journal for VLSI, IEEE Micro, etc.
- Senior Member of IEEE, 2001.
- Member of New York Academy of Sciences, SPIE, IS&T.
- Executive member of IEEE TCMM, 1992, 1993, 1994.
- Editorial board member for IEEE Micro, 1994-2000.
- Editorial board member for IEEE Spectrum, 1996-1998.
- Advisory board for Hewlett-Packard Journal, 1993-1998.
- Guest Editor of IEEE Micro special issue, Vol. 14 No. 2, April 1994, on “Hot Chips V”.
- Guest Editor of IEEE Micro special issue, Volume 16 Number 4, August 1996, on “Media Processing”.
- Invited panelist and speaker at conferences, colloquiums and seminars.
- Program Chair or Committee Member for Hot Chips Conference, IEEE Compcon Conference, VLSI Technology, Circuits and Systems Conference, Design Technology Conference, Technical Women's Conference, and many HP forums.

HONORS AND AWARDS:

Elected Fellow of the Association of Computing Machinery (ACM), October 2001.

Elected Senior Member of IEEE, February 2001.

Awarded an IEEE Computer Society Certificate of Appreciation, on February 22, 1999, in recognition of the outstanding special issue developed as Guest Editor of the August 1996 Special Issue of IEEE Micro on “Media Processing”.

Awarded an IEEE Computer Society Certificate of Appreciation, on January 22, 1999, in recognition of dedicated service as a member of the IEEE Micro editorial board during 1994-1998.

Princeton 250th Anniversary Fund for Innovation in Undergraduate Education Award, 1999, for co-developing a new course on "Multimedia and its Impact in the Next Millennium".

Appointed the Forrest G. Hamrick Professor in Engineering, Princeton University, October 1998.

Awarded an IEEE Computer Society Certificate of Appreciation, on 25 August 1997, for service to the IEEE Computer Society by serving as a Program Co-Chair of the Hot Chips Symposium.

Invited and selected for listing, every year since around 1996 or 1997, in Who’s Who in the World (from 1997), Who’s Who in America, Who’s Who of American Women, Who’s Who in the West, etc.

Awarded 88 U.S. and international patents (20 U.S. Patents), on instruction-set architecture, multimedia architecture, subword parallelism, subword permutations, pipeline design, cache hints, coprocessors and assists, multiprocessors.

Best Paper Award, Design Technology Conference, 1986.

Phi Beta Kappa, elected sophomore/junior year, 1972.

Alpha Lambda Delta, freshman women’s honorary, elected 1971.

Deans’ Scholarship (merit based), Cornell University, 1971-1973.

Federation of Cornell Women’s Scholarship (merit based), 1971-1973.

Elected into College Scholar Program, Cornell University, 1970-1973.

“Leaders of Tomorrow” national high school oratorical contest, co-winner 1970.

PATENTS

I have been granted 20 U.S. Patents to date, of which I am the primary inventor of 16 of these. I have also been granted about 68 international patents (Europe – individual countries, Canada, Asia - Japan, etc.). Listed below are the U.S. Patents only:

1. U.S. Patent 6,079,012, "Computer that selectively forces ordered execution of store and load operations between a CPU and a shared memory", Dale C. Morris, Bernard L. Stumpf, Barry J. Flahive, Jeffrey D. Kurtze, Stephen G. Burger, Ruby B. L. Lee and William R. Bryg, filed Nov 6 1997, continuation of Ser. No. 234,207, April 28, 1994, granted June 20, 2000. (8 claims).

2. U.S. Patent 5,883,824, "Parallel adding and averaging circuit and method", Ruby Lee and John Beck, filed 11/29/93, granted 2000.

3. U.S. Patent 5,757,377, "Expediting Blending and Interpolation via Multiplication", Ruby B. Lee and Michael J. Mahon, granted May 26, 1998.

4. U.S. Patent 5,734,599, "Performing a Population Count using Multiplication", Ruby B. Lee and Steven Bass, granted March 31, 1998.

5. U.S. Patent 5,721,697, "Performing Tree Additions Via Multiplication", Ruby B. Lee, filed May 17, 1996, granted Feb 24 1998 (16 claims).

6. U.S. Patent 5,673,321, "Efficient Selection and Mixing of Multiple Sub-Word Items Packed into Two or More Computer Words", Ruby Bei-Loh Lee, filed June 29, 1995, granted Sept 30, 1997 (17 claims).

7. U.S. Patent 5,636,351, "Performance of An Operation on Whole Word Operands and on Operations in Parallel on Sub-Word Operands in a Single Processor", Ruby B. Lee, filed February 17, 1995, granted June 3 1997 (32 claims).

8. U.S. Patent 5,579,253, "Computer multiply instruction with a subresult selection option" Ruby B. Lee, Charles R. Dowdell, Joel D. Lamb, filed Sept 2, 1994, granted Nov. 26, 1996 (6 claims).

9. U.S. Patent 5,574,676, "Integer Multiply Instructions Incorporating a Subresult Selection Option", Ruby B. Lee, Charles R. Dowdell, Joel D. Lamb, filed Sept 2, 1994, granted Nov 12, 1996 (9 claims).

10. U.S. Patent 5,467,131, "Method and Apparatus for Fast Digital Signal Decoding", Vasudev Bhaskaran and Ruby B. Lee, granted November 14, 1995.

11. U.S. Patent 5,448,509, "Efficient Hardware Handling of Positive and Negative Overflow Resulting from Arithmetic Operations", Ruby B. Lee and Joel D. Lamb, filed Dec 8, 1993, granted September 5, 1995.

12. U.S. Patent 5,424,967, “Shift and Rounding Circuit and Method”, Ruby B. Lee, filed Nov 23, 1993, granted June 13, 1995.

13. U.S. Patent 5,390,135, “Parallel Shift and Add Circuit and Method”, Ruby B. Lee and Joel D. Lamb, filed Nov 23, 1993, granted Feb 14, 1995.

14. U.S. Patent 5,278,985, “Software Method for Implementing Dismissible Instructions on a Computer”, Daryl Odnert, Michael J. Mahon, Dale C. Morris, Jerome C. Huck, Ruby B. Lee, Stephen G. Burger, William R. Bryg, Vivek S. Pendharkar, filed Oct 31, 1990, granted Jan 11, 1994 (3 claims).

15. U.S. Patent 5,051,896, "Apparatus and Method for Nullifying Delayed Slot Instructions in a Pipelined Computer System", Ruby B. Lee and Allen J. Baum, filed March 21, 1988, based on filing of June 28, 1985, granted September 24, 1991 (3 claims).

16. U.S. Patent 4,928,239, "Cache Memory with Variable Fetch and Replacement Schemes", Allen Baum, William R. Bryg, Michael J. Mahon, Ruby B. Lee, Steven S. Muchnick, filed May 26, 1989, based on filing of June 27, 1986, granted May 22, 1990 (8 claims).

17. U. S. Patent 4,829,424, "Maximal Length Immediates with Fixed Sign Position", Ruby B. Lee, filed June 28, 1985, granted May 9, 1989 (5 claims).

18. U.S. Patent 4,763,242, "Computer Providing Flexible Processor Extension, Flexible Instruction Set Extension, and Implicit Emulation for Upward Software Compatibility", Ruby B. Lee and Michael J. Mahon, filed October 23, 1985, granted August 9, 1988 (13 claims).

19. U.S. Patent 4,755,966, "Bidirectional Branch Prediction and Optimization", Ruby B. Lee and Allen J. Baum, filed June 28, 1985, granted July 5, 1988 (2 claims).

20. U.S. Patent 4,722,050, "Method and Apparatus for Facilitating Instruction Processing of a Digital Computer", Ruby B. Lee, Allen J. Baum and Russell Kao, filed March 27, 1986, granted January 26,1988 (18 claims).

PATENT DISCLOSURES PENDING:

1. HP case 01092724-4, filed 9/26/95, D. Morris, B. Flahive, S. Burger, R. Lee, M. Ziegler, B. Stumpf, J. Huck and J. Kurtze.
2. HP case 01093837-1, filed 8/1/95, R. Lee.
3. HP case 01094612-1, filed 7/7/95, R. Lee.
4. HP case 01093846-4, filed 5/17/95, R. Lee.
5. Princeton,NJ, case 2001-01, filed May 5, 2001, R. Lee, et al.
6. Princeton,NJ, case 2001-02, filed May 5, 2001, R. Lee, et al.
7. Princeton,NJ, case 2001-03, filed May 5, 2001, R. Lee, et al.
8. Princeton,NJ, case 2001-04, filed May 5, 2001, R. Lee.

Plus other applications in the process of filing to the U.S. Patent Office.

PROVISIONAL U.S. PATENT APPLICATIONS FILED:

1. USPTO Serial No. 60/202,250, filed 5/5/2000.
2. USPTO Serial No. 60/202,243, filed 5/5/2000.
3. USPTO Serial No. 60/202,244, filed 5/5/2000.
4. USPTO Serial No. 60/202,246, filed 5/5/2000.
5. USPTO Serial No. 60/202,245, filed 5/5/2000.

INVENTION DISCLOSURES FILED WITH PRINCETON UNIVERSITY:

1. Ruby Lee and Xiao Yang. Princeton Docket No. 00-1710-1. May 1, 2000.
2. Ruby Lee, Xiao Yang and Manish Vachharajani. Princeton Docket No.: 00-1711-1. May 1, 2000.
3. Ruby B. Lee. Princeton Docket No. 00-1712-1. October 25, 1999.
4. Ruby B. Lee. Princeton Docket No. 00-1713-1. October 25, 1999.
5. Ruby B. Lee. Princeton Docket No. 00-1713-1. October 25, 1999.
6. Ruby B. Lee and Zhijie Shi. Princeton Docket No. 00-1709-1. October 25, 1999.
7. Ruby B. Lee and Zhijie Shi. Princeton Docket No. 00-1709-1. October 25, 1999.

INVITED PRESENTATIONS (RECENT)

"Designing Security into the Core Hardware of Information Appliances and Servers", invited Plenary talk, Emerging Information Technology Conference, November 9, 2001.

"Computer Arithmetic – A Processor Architect's Perspective", invited Keynote speech, IEEE International Symposium on Computer Arithmetic, June 11, 2001.

"Has Scaling created a microprocessor monster?", invited panelist with Dave Patterson, Yale Patt and 3 circuit designers, International Solid State and Circuits Conference (ISSCC), San Francisco, February 2001.

"New Instruction-Set Architecture for Secure Internet Multimedia Appliances and Servers", invited presentation, Multimedia and Networking Technology conference, November 1999.

"Media Processor Architectures for Secure Information Appliances" invited presentation, CAP '99, May 6, 1999.

"Multimedia Extensions for General-Purpose Processors, including (codename)", Hewlett-Packard broadcast seminar, December 11, 1997, Cupertino, California.

"Multimedia Extensions for General-Purpose Processors", invited keynote speech, IEEE Signal Processing Systems: Design and Implementation, November 3-5, 1997, United Kingdom.

"Exploiting Parallelism in Media Processing", invited keynote speech, High Performance Computer Architecture conference, Feb 2-5, 1997, San Antonio, Texas.

"Multimedia Extensions for General-Purpose Microprocessors", (invited), Microprocessor Forum, October 1996, San Jose, California.

"Accelerating Multimedia with Subword Parallelism in Microprocessors", The Distinguished Lecture Series X, (invited) videolecture recorded March 24, 1995, released July 1995, University Video Communications, California, http://www.uvc.com/.

"Multimedia Workstations and Systems", (invited), Frost and Sullivan Strategic Multimedia Conference, Oct 3-4, 1994, New York, New York.

"Pervasive Collaborative Multimedia", (invited), IEEE ISSCC Solid-State Circuits and Technology Workshop on Multimedia Services, Algorithms and Chips, February 15, 1994, San Francisco, California.

CONTRIBUTIONS TO BOOKS

Ruby B. Lee. Instruction Set Architecture for Multimedia Signal Processing. *Invited book chapter. In the "Computer Engineering Handbook"*, edited by Vojin G. Oklobdzija, CRC Press, December 2001.

Ruby B. Lee and A. Murat Fiskiran. Multimedia Instructions in Microprocessors for Native Signal Processing. *Invited book chapter. In "Programmable Digital Signal Processors: Architecture, Programming and Applications"*, edited by Yu Hen Hu, Marcel Dekker, Inc., December 2001.

Ruby Lee. Precision Architecture. *In "Reduced Instruction Set Computers", Second Edition*, edited by William Stallings, IEEE Computer Society Press, 1990, pp. 216-230.

Ruby Lee and Alan Wiemann. New Design Methodologies and Circuits Needed for Parallel VLSI Supercomputers. *In "Advanced Computer Architecture Tutorial"*, edited by Dharma Agrawal, IEEE Computer Society Press, Order Number 667, 1986.

Ruby Lee. Performance Bounds in Parallel Processor Organizations. *In "High Speed Computers and Algorithm Organization"*, edited by David Kuck et al, Academic Press, 1977.

PAPERS

Ruby B. Lee. Alphabets of Permutation Primitives for 2-D Multimedia Processing. *Invited journal paper, in preparation.*

Ruby B. Lee. Superdata Execution: exploiting superscalar resources for higher performance. *Submitted for publication, November 2001.*

Ruby B. Lee, J. Patrick McGregor, David Karig and Zhijie Shi. An Architectural Approach to Mitigating Distributed Denial of Service Attacks Resulting from Buffer Overflow. *Submitted for publication, November 2001.*

Ruby B. Lee, Zhijie Shi and Xiao Yang. Efficient Permutations for Fast Software Cryptography. *IEEE Micro*, Vol. 21 No. 6, pp. 56-69, December 2001.

John P. McGregor and Ruby B. Lee. Architectural Enhancements for Fast Subword Permutations with Repetitions in Cryptographic Applications. *Proceedings of the IEEE International Conference on Computer Design*, pp.453-461. Austin, Texas, September 2001.

A. Murat Fiskiran and Ruby B. Lee. Performance Impact of Addressing Modes on Encryption Algorithms. *Proceedings of the IEEE International Conference on Computer Design*, pp. 542-545, Austin, Texas, September 2001.

Ruby B. Lee, A. Murat Fiskiran and Abdulla Bubshait. Multimedia Instructions in IA-64. *Invited paper, Proceedings of 2001 IEEE International Conference on Multimedia and Expo (ICME 2001)*, Tokyo, Japan, August 22-25, 2001.

John P. McGregor and Ruby B. Lee. Performance Impact of Data Compression on Virtual Private Network Transactions. *Proceedings of the 25th IEEE Conference on Local Computer Networks, pp. 500-510*, November 2000.

Xiao Yang and Ruby Lee. Fast Subword Permutation Instructions Using Omega and Flip Network Stages. *Proceedings of the International Conference on Computer Design, pp. 15-22*, September 2000.

Daniel F. Zucker, Ruby B. Lee, and Michael J. Flynn. Hardware and Software Cache Pre-fetching Techniques for MPEG Benchmarks. *IEEE Transactions on Circuits and Systems for Video Technology. Vol. 10 No. 5, pp. 782-796.* August 2000.

Ruby Lee. Subword Permutation Instructions for Two-Dimensional Multimedia Processing in MicroSIMD Architectures. *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors, pp. 3-14.* July 2000.

Zhijie Shi and Ruby Lee. Bit Permutation Instructions for Accelerating Software Cryptography. *Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors, pp. 138-148*. July 2000.

Zhen Luo and Ruby B. Lee. Cost-Effective Multiplication with Enhanced Adders for Multimedia Applications. *Proceedings of ISCAS 2000, IEEE International Symposium on Circuits and Systems, Vol. I, pp. 651-654*, May 2000.

Xiao Yang, Manish Vachharajani and Ruby B. Lee. Fast Subword Permutation Instructions Based on Butterfly Networks. *Proceedings of SPIE, Media Processors 2000, pp. 80-86*, January 2000.

Ruby B. Lee. Efficiency of microSIMD architectures and index-mapped data for media processors. Invited paper. *Proceedings of Media Processors 1999, IS&T/SPIE Symposium on Electric Imaging: Science and Technology, pp. 34-46*, January 1999.

Daniel Zucker, Ruby Lee, and Michael Flynn. An Automated Method for Software Controlled Cache Prefetching. *Proceedings of the 31st. Hawaii International Conference on System Sciences*, January 1998.

T. Conte, P. Dubey, M. Jennings, R. Lee, A. Peleg, S. Rathnam, M. Schlansker, P. Song, and A. Wolfe. Challenges to Combining General-Purpose and Multimedia Processors. *IEEE Computer, Volume 30 Number 12, pp. 33-37*, December 1997.

Alice Yu, Ruby Lee, and Michael Flynn. Performance Enhancement of H.263 Encoder Based on Zero Coefficient Prediction. *Proceedings of the Fifth ACM International Multimedia Conference, pp. 21-29*, November 1997.

Ruby Lee. Multimedia Extensions for General-Purpose Processors. Invited paper. *Proceedings of the IEEE Signal Processing Systems Design and Implementation, pp. 9-23.* November 1997.

Alice Yu, Ruby Lee, and Michael Flynn. Early Detection of All-Zero Coefficients in H.263. *Proceedings of the Picture Coding Symposium, pp. 159-164*, September 1997.

P. Wong, D. Tretter, C. Herley, N. Moayeri, R. Lee. Imaging Processing Considerations for Digital Photography. *Proceedings of IEEE Compcon, pp. 280-285*, February 23-26, 1997.

Alice Yu, Ruby Lee, Michael Flynn. An Evaluation of Video Fidelity Metrics. *Proceedings of IEEE Compcon, pp. 49-60*, February 23-26, 1997.

Ruby Lee, Larry McMahan. Mapping of Application Software to the Multimedia Instructions of General-Purpose Microprocessors. *Proceedings of Multimedia Hardware Architectures 1997, IS&T/SPIE Symposium on Electric Imaging: Science and Technology*, Feb 10-14, 1997.

Daniel Zucker, Ruby Lee, Michael Flynn. Achieving Subword Parallelism by Software Reuse of the Floating-Point Data Path. *Proceedings of Multimedia Hardware Architectures 1997, IS&T/SPIE Symposium on Electric Imaging: Science and Technology*, Feb 10-14, 1997.

Ruby Lee, Michael Smith. Media Processing: A New Design Target. *IEEE Micro, Volume 16 Number 4, pp. 6-9,* August 1996.

Ruby Lee. Subword Parallelism with MAX-2. *IEEE Micro*. Vol. 16 No. 4, pp.51-59, August 1996.

Daniel Zucker, Michael Flynn, Ruby Lee. A Comparison of Hardware Prefetching Techniques for Multimedia Benchmarks. *Proceedings of 3rd. IEEE International Conference on Multimedia Computing and Systems*, Hiroshima, Japan, June 17-23, 1996.

Ruby Lee. HP's Multimedia instructions Speed Video. Invited submission. *In Bernard Cole's feature section on Multimedia Computing, E.E. Times*, April 17, 1996.

Ruby Lee, Jerry Huck. 64-bit and Multimedia Extensions in the PA-RISC 2.0 Architecture. *Proceedings of IEEE Compcon, pp. 152-160*, Feb 25-28, 1996.

Daniel Zucker, Michael Flynn, Ruby Lee. Improving Performance for Software MPEG Players. *Proceedings of IEEE Compcon, pp. 327-332*, Feb 25-28, 1996.

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