integration with digital circuits. Short-channel MOSFET's offer the promise of high $g_m$ and high $f_T$, but have generally suffered from low $r_0$ and low available gain. We are reporting here the design and fabrication of a submicrometer channel length DMOS transistor which offers a significant increase in $r_0$, a higher $g_m$, an increase in breakdown voltage, and a reduced body effect when compared to regular NMOS transistors. The cost of integration of this device is two mask steps and two implants. Only photoresist patterning is required, and the process temperature budget is easily accommodated into any CMOS process.

The available gain of a typical NMOS with $t_{ox} = 15$ nm and $L_g = 1$ $\mu$m is about 10 at $V_{GS} - V_T = 1$ V and $V_{DS} = 3$ V. DMOS devices have been fabricated with an available gain of 250 at the same $t_{ox}$, $L_g$, $V_{GS} - V_T$, and $V_{DS}$. This represents a factor of 25 improvement in gain, and is due to increases in $g_m$ and $r_0$ of 1.4 and 18, respectively. The factor of 1.4 increase in $g_m$ is expected to increase the cutoff frequency to well above 10 GHz. In addition to the improvement in gain, the breakdown voltage of a DMOS with $V_t = 1$ V is over 6 V, and $V_T$ sensitivity of DMOS to substrate bias has decreased slightly compared to NMOS with identical $V_T$.

DMOS and NMOS were fabricated on the same chip, with both $V_T$'s adjusted to 1 V. The DMOS channel consists mostly of a light n-type "drift" region formed by a light As implant, which is similar to that in a buried-channel MOS. A high concentration of boron is implanted into and diffused from the source side, thus leading to the formation of a 0.1-$\mu$m "halo." This halo forms a barrier to electron injection from source to channel, and prevents drain induced barrier lowering. The halo also determines the $V_T$ of the device.

The combination of diffused and drift region significantly changes the E-field distribution in the channel. According to 2-D simulation, the peak field is reduced in the pinched channel near the drain, whereas a secondary smaller peak is formed near the source. As a result, electrons are launched from the source at near saturation velocity, but fields everywhere are sufficiently low so that very little substrate current is generated. This hypothesis is supported by experimental evidence indicating that $g_m$ is nearly independent of $L$ for $L_g \leq 1.4$ $\mu$m. The calculated carrier velocity in DMOS is $7 \times 10^6$ cm/s, compared to $5 \times 10^6$ cm/s in NMOS.

This work highlights the need for accurate 2-D process and device simulation. While the quantitative accuracy of our SUPRA/MINIMOS simulations has not yet been assessed, it is clear that they have provided excellent quailitative guidance. Further experimentation and simulation is expected to yield even higher gains and breakdown voltages.

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*Student paper.*

**IIA-4 Surface Potential Fluctuations in MOS Devices Induced by the Random Distribution of Channel Dopant Ions**—J. T. Watt and J. D. Plummer, Center for Integrated Systems, Stanford University, Stanford, CA 94305.

One of the fundamental assumptions used in semiconductor device analysis is that dopants create a locally uniform volume charge density which is related to the potential through Poisson's equation. In reality, doping introduces discrete ions which create potential fluctuations because of their random distribution. It was shown by Nicollian and Goetzberger [1] that surface potential fluctuations in MOS devices are caused primarily by charge at the Si/$SiO_2$ interface rather than channel dopant ions. These results, however, were based on lightly doped devices with large interface charge. With the advent of device scaling and improvements in MOS processing, channel doping densities have been constantly increasing while interface charges have been virtually eliminated. This has lead to a renewed interest in the effect of substrate doping on surface potential fluctuations.

The ac split $CV$ technique [2] has been used to measure the gate–channel capacitance of n- and p-channel MOSFET's with channel doping densities in the range $3 \times 10^{16}$–$4 \times 10^{18}$ cm$^{-3}$ at both 295 and 77 K. Comparison to simulation has revealed a stretch-out of the measured characteristics which can be well modeled assuming a lateral threshold voltage nonuniformity with a Gaussian probability distribution. The standard deviation of the threshold voltage distribution varies from 25 to 375 mV as doping density increases with very little dependence on dopant type or temperature. The observed variance of the threshold voltage has been accurately predicted by a three-dimensional model based on the method of images which includes only the contribution from a random distribution of dopant ions in the depletion region.

In addition to affecting the charge–voltage characteristics, surface potential fluctuations also affect carrier transport in MOS devices by introducing potential barriers in the channel. The resulting thermally activated transport process causes a reduction in the effective carrier mobility at low inversion charge densities which has been characterized for both n- and p-channel devices at room and liquid-nitrogen temperature. While the mobility behavior of holes has been predicted by a simple barrier model [3], there is additional degradation in the case of electrons which may be due to ionized impurity scattering.

The results of this study clearly demonstrate the presence of surface potential fluctuations in MOS devices resulting from the random channel dopant ion distribution. While the effects of the surface potential fluctuations do not become significant until doping densities approach the $10^{18}$ cm$^{-3}$ level at room temperature, measurable departures from simple theory occur over the entire doping density range studied. At liquid-nitrogen temperature the fluctuations induced by the channel dopant ions are substantial even at doping densities in the $10^{16}$ cm$^{-3}$ range and must be considered to accurately model device behavior.

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**IIA-5 Transconductance Enhancement Mechanisms in Ultra-Thin ( $\leq$1000 Å ) Silicon-on-Insulator MOSFET's**—J. C. Sturm and K. Tokunaga, Department of Electrical Engineering, Princeton University, Princeton, NJ 08544; and J.-P. Colinge, Hewlett Packard Laboratories, 3500 Deer Creek Rd., Palo Alto, CA 94304.

Recently, several advantages of ultra-thin ( $\leq$1000 Å ) silicon-on-insulator (SOI) films for MOSFET's have been described. These include improved short-channel threshold voltage stability and reduced hot-electron effects [1], [2]. We here describe two new advantages of SOI FET's in ultra-thin films. Compared to bulk FET's of similar dimensions and doping levels, these new effects have been observed to give up to a 35-percent increase in drain saturation current or transconductance. Both experimental data and modeling will be presented.

In a FET, a portion of the vertical electric field from the gate electrode is terminated on carriers in the conducting channel and a portion is terminated on substrate charge in the depletion region underneath the channel. In a bulk FET, this substrate charge grows as one goes from the source to the drain because of the increasing

channel–substrate voltage. This extra charge comes at the expense of carriers in the channel and is the cause of the body effect. In a MOSFET in a very thin SOI film, the SOI film is already completely depleted through at the threshold condition. For a thick underlying oxide, the effective substrate charge is then fixed, eliminating the body effect and leaving more electric field to terminate on carriers in the channel. More carriers in the channel lead to a higher drain current. Simple modeling for a gate oxide of 200 Å, a film or substrate doping of $4 \times 20^{16}$ cm$^{-3}$, and an SOI thickness of 800 Å predicts a saturation current increase of 30 percent. A second effect which serves to increase current in such structures is the effect of vertical field on carrier mobility [3]. The reduced vertical field in an ultra-thin SOI FET should lead to a higher mobility. This effect is especially important near the drain end of the device. Both effects together predict a 40 percent saturation current increase in the SOI FET's.

Experimentally, we have compared the drain saturation current in simultaneously processed n-channel bulk and ultra-thin film (1000 Å) SOI transistors with a film or substrate doping of $1 \times 10^{17}$ cm$^{-3}$ and a gate oxide of 250 Å. The SOI films were prepared by high-energy oxygen implantation and subsequent annealing at 1250°C. Although the SIMOX annealing conditions are known to be suboptimal, a 25 to 35 percent increase in the saturation current in the SOI FET's over their bulk counterparts was observed. A higher drain saturation voltage was also observed, consistent with earlier observations of reduced hot-electron effects. By varying the substrate bias, higher effective mobility in the SOI structure and the negligible effect of channel-substate voltage on effective mobility in the SOI structures were confirmed.

It should be noted that the kink effect is absent in the ultra-thin film SOI FET's, and that the results were adjusted to account for the difference in threshold voltage in the two structures. In general, an increase in saturation current should lead to faster circuits. Recently, fully depleted thin-film SOI CMOS circuits showed about a 30 percent decrease in ring oscillator speed (to 30 ps at room temperature) over non-fully depleted films for a 0.8-$\mu$m technology [4]. Our experiments and modeling results to date are for long-channel structures only, and short-channel work in is progress.

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**IIA-6 ITF-BSCC Technology for 16Mbit DRAM Cell**—Shunji Takase, Hideki Itoh, Hidetoshi Wakamatsu, Akio Kita, Fumio Ichikawa, and Masayoshi Ino, VLSI Research and Development Laboratory, OKI Electric Industry Co., Ltd., 550-1, Higashiasakawa, Hachioji, Tokyo 193, Japan.

A buried stacked capacitor cell (BSCC) [1] is one of the most suitable cell structures for 16-Mbit DRAM's. There are, however, two kinds of unfavorable current leakage paths such as 1) between the storage node and the substrate caused by the gate controlled diode structure along the trench sidewall $SiO_2$ [2] and 2) between the neighboring cell contacts caused by the punchthrough under the field $SiO_2$.

To improve these problems, the technology of BSCC with ion implantation through the field $SiO_2$ (ITF-BSCC) is reported in this paper. The key point of ITF-BSCC is a $p^+$ region which is formed 0.4–0.6 $\mu$m from the Si substrate surface under the active region and isolation region. This $p^+$ region acts as isolation under the field $SiO_2$ and as the potential barrier for the leakage current of the gate-controlled diode. The concentration of this $p^+$ region should be optimized from the view points of the potential barrier along the trench sidewall $SiO_2$ and the cell contact junction leakage current.

This $p^+$ region can be fabricated by boron ion implantation at 180–200 keV to a dose of 5E11–1E12 cm$^{-2}$ into all the surface of Si substrate after the isolation region formation. This ion implantation also combines the channel stop ion implantation of conventional LOCOS. All steps of processes except this boron ion implantation are the same as those of conventional BSCC.

The leakage current of the gate-controlled diode with trenches fabricated by ITF-BSCC process and conventional BSCC process were measured. The peak leakage current of ITF-BSCC is 3–5 times as low as that of conventional BSCC, because the $p^+$ region surrounds the trenches at 0.4–0.6-$\mu$m depth under the cell contact $n^+$ region and acts as the potential barrier for the leakage current which is generated at the trench sidewall under this $p^+$ region flowing up to the cell contact $n^+$ region. By fabricating ITF-BSCC in the p-well, the peak leakage current is reduced to 1.1E-16A/trench, and this is low enough to keep the holding time garanteed value.

Also, the leakage current between the neighboring cell contacts is measured. By fabricating ITF-BSCC in the p-well, the cell contact spacing, 0.9 $\mu$m is achieved. This is because the reduction of boron concentration under the field $SiO_2$ can be avoided during the field oxidation. The spacing is small enough for 16-Mbit DRAM's.

As the result, ITF-BSCC technology can realize high performance and high density for 16-Mbit DRAM's.

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**IIA-7 Alpha-Particle-Induced Hard Error Mechanism in DRAM's**—H. Kurosawa, H. Iwai, M. Ishihara, and K. Shimohigashi,* Device Development Center, Hitachi Ltd., 2326 Imai Omeshi, Tokyo 198, Japan.

$\alpha$-particle irradiation induces not only soft errors, but hard errors in DRAM as well. The latter, the increase of leakage current from storage nodes in cells and the refresh time decrease, are observed with intentional $\alpha$-particle irradiation [1]. This report describes the mechanism of the leakage current increase.

The following is confirmed experimentally. $\alpha$-particle irradiation induces the leakage current increase of $n^+$-p junctions in a cell. The current has two modes. One is due to the interface-trapped charge on the LOCOS surface and the other is caused by defects in the silicon substrate; the former is about 1.5 times larger than the latter. This phenomenon is observed using a plane, striped with 4-$\mu$m width and 2-$\mu$m width $n^+$-p junction diodes. It is concluded from the above data that the rate of current increase on the LOCOS surface is 0.32 fA/$\mu$m · h and the one in the silicon substrate is 0.22 fA/$\mu$m$^2$ · h during irradiation with 90-$\mu$Ci $^{241}$Am.

Leakage current on the LOCOS surface is influenced by the interface-trapped charge. This charge can be analyzed with *C-V* characteristics using a MOS diode with 500-nm oxide thickness on the p-substrate [2]. Interface-trap densities near the center of the silicon energy bandgap irradiated with 90-$\mu$Ci $^{241}$Am for 2 h are 3 times larger than nonirradiated densities. The rate of increase is $2.5 \times 10^8$ cm$^{-2}$ · eV$^{-1}$/h · $\mu$Ci, and this current depends on the LOCOS thickness. That is, the number of induced hole-electron