Suppressed Phosphorus Autodoping in Silicon Epitaxy for Ultrasharp Phosphorus Profiles by Low Temperature Rapid Thermal Chemical Vapor Deposition

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The production of ultra-sharp phosphorus doping profiles in silicon by low pressure chemical vapor deposition epitaxy is hampered by autodoping effects, which are attributed to phosphorus segregation and redeposition. In this work the phosphorus autodoping effect is completely suppressed by interrupting the growth process to clean the surface ex-situ while the reactor is purged at the same time. A low-temperature in-situ hydrogen bake (10 torr, 800°C, 1-2 min) after reloading the wafer reduces both carbon and oxygen contamination below secondary ion mass spectroscopy detection limits, and yields a high quality n-type/intrinsic silicon interface that is suitable for device application.

INTRODUCTION

Phosphorus and arsenic autodoping effects in low temperature chemical vapor deposition (CVD) of epitaxial silicon have hindered the production of sharp n-type profiles that are desirable for device structures. The autodoping effect has been observed for many n-type silicon dopants sources such as arsenic, phosphorus, and antimony (1), and many different deposition systems such as low pressure chemical vapor deposition (LPCVD), ultra high vacuum chemical vapor deposition (UHVCVD) and molecular beam epitaxy (MBE) (1,2,3). In our laboratory the autodoping effect limits the phosphorus concentration fall off in samples grown by rapid thermal chemical vapor deposition (RTCVD) at 700°C to ~200 nm / decade which is similar to what is observed in other LPCVD systems (3). This is over an order of magnitude slower than the rate of decay of boron profiles, for which 10 nm / decade is achieved using diborane as a dopant source.

Phosphorus autodoping effects are frequently blamed on two potential causes: (i) dopant segregation to the surface (3); and (ii) dopant redeposition from reactor surfaces during growth (4). In this paper we discuss the growth of a sharp phosphorus profile grown in a low pressure, low-temperature rapid thermal chemical vapor deposition (RTCVD) system. Using an interrupted growth process, the sample surface is cleaned in order to remove excess phosphorus with a wet ex-situ etch combined with an in-situ hydrogen bake (5,6), while the reactor is purged with a blank growth in parallel with the ex-situ clean. This concept has been used for a silicon n-channel MODFET structure grown by UHVCVD, but the interrupted interface suffered from oxygen and carbon contamination (2). In this work, an in-situ low-temperature clean, 1-2 minutes at 800°C in 10 torr of hydrogen, reduces oxygen and carbon levels below SIMS detection limits and still yields an ultra-sharp profile. The interrupted interface is found to be nearly indistinguishable to epitaxial silicon grown without interrupting the process characterized by photoluminescence (PL)

intensities from strained SiGe layers grown above the cleaned surface and by secondary ion mass spectroscopy (SIMS) of the burried interfaces. Most of this paper will describe the development of this low-temperature (800°C) cleaning process, so that interfaces with low oxygen and carbon can be achieved with out the need of a high temperature bake, which would lead to excessive diffusion of the phosphorus profile.

EXPERIMENTAL PROCEDURE

All structures were grown using a RTCVD cold-wall reactor with a quartz growth chamber heated by halogen lamps located outside the vacuum system (9). The system is pumped by a rotary vane pump and the vacuum integrity relies on o-ring seals. Samples are loaded through a load-lock, also pumped by a rotary vane pump. Source gases used in this work are $Si_2H_2Cl_2$, GeH_4, and PH_3. Hydrogen was used as the carrier gas, which was purified through a Nanochem resin based purifier that insures impurity concentrations to be less than 10 ppb. All silicon and SiGe epitaxy was grown at temperatures of 625°C and 700°C respectively and the reactor pressure was maintained at 6 torr with a dichlorosilane (DCS) partial pressure of approximately 0.052 torr. The growth rates were approximately 100 Å/min and 30 Å/min for the SiGe and Si epitaxy , and oxygen and carbon levels are typically below $2x10^{18}/cm^3$ and $5x10^{17}/cm^3$ respectively.

To examine the quality of various cleaning techniques, silicon substrates were subjected to various wet chemical cleans followed by in-situ hydrogen bakes before epitaxy of $Si_{0.8}Ge_{0.2}$ at 625°C (200Å) followed by a 700°C silicon cap (450Å). All buried Si / $Si_{0.8}Ge_{0.2}$ interfaces were characterized using PL from the pseudomorphically strained SiGe layers as a test of the interface quality (8). Photoluminescence spectra were measured from samples at temperatures of 77 K using a liquid nitrogen cooled Ge detector and an argon laser excitation. The pump power density was approximately ~5 W/cm^2. The luminescence intensity from the strained SiGe layer is extremely sensitive to the carrier lifetime in the SiGe layer and at the hetero-interfaces [7,11]. Interface contamination will lead to increased non-radiative recombination of excited carriers and reduce the overall luminescence intensity emitted from the $Si_{1-x}Ge_x$ layer. The integrated luminescence emitted from the capping $Si_{1-x}Ge_x$ layers were, therefore, compared to the integrated luminescence intensity emitted from the bulk silicon to qualitatively describe the quality of the interface.

Buried interfaces were also characterized using SIMS done at Evans East, in East Windsor, NJ. A 3 keV Cs^+ primary ion beam was used to bombard the surface of the sample and obtain the secondary ions. Sputter rates were between 5-15 Ångstroms/second, producing oxygen and carbon detection limits of approximately $2x10^{18}/cm^3$ and $5x10^{17}/cm^3$ respectively for most samples. Sputter rates were determined using profilometry leading to ~5% uncertainty in depth profiles. Chemical species concentrations were measured to within 15% error.

A standard procedure for the ex-situ wet clean was established beginning with the

removal of the native oxide from 5-50 ohm-cm resistivity p-type 4" substrates using a ~1 minute dilute HF dip. The surface is then chemically oxidized to both smooth and clean the surface by consuming the top 5-20Å of silicon surface (10). The oxide is removed using a dilute HF dip, which leaves the surface hydrogen terminated (11). Preparation of the final wet oxidation of the surface was predominately done by emersion of the wafer in H_2SO_4:H_2O_2 3:1 at 70°C. A standard RCA (12) clean was found to be slightly worse as measured by photoluminescence of subsequently grown SiGe/Si capping layer. DI rinses of the wafer surface after the last oxide removal were avoided in all cases except noted, as there exists compelling evidence in the literature that post HF dip rinses reoxidize the silicon surface (13). The DI total organic content was 45 ppb and the resistivity was 18 MOhms-cm.

Following the wet clean the wafer is introduced to the reactor on a single 4 inch wafer quartz stand through a load-lock, which is evacuated to ~50 mtorr by a standard rotary-vane mechanical pump. The wafer is put through a minimum of 4 pump-purge cycles in the load-lock, before the wafer is introduced to the growth chamber. The pump-purge cycle consists of filling the load-lock to ~ 1 torr with dry nitrogen before evacuation. One cycle approximately 5 minutes. After purging the load-lock, the wafer is transferred to the growth chamber which is kept at between 1-10 torr of hydrogen. Immediately following the wafer transfer from the load-lock to the reactor a flow of 1 slpm of hydrogen is passed through the reactor and the reactor pressure is maintained at 1 torr. Immediately before growth the hydrogen flow rate is increased to 3 slpm and the pressure is raised to 6 torr followed by heating the wafer to the growth temperature of 625°C. When the growth temperature is reached, growth is begun by injecting dichlorsilane into the reactor chamber followed by germane injection approximately 5 seconds later, to give a SiGe layer growth rate of 100 Å/min.

Germane is known to react with silicon dioxide to form the volatile species GeO_x. Oxide removal using germane at temperatures of 650-700°C has been reported (16). This report found, however, that for sub-monolayer oxides, germanium adsorbs preferentially to the bare silicon surface rather than forming the volatile germanium-oxide. The sequence of dichlorosilane followed by germane was chosen to allow the SiGe layer to grow as soon as the germane is injected. Because the SiGe layer grows quickly on the silicon surface with no observably long incubation time, and the germane molecule prefers the open silicon surface site over that of the oxide site, it is concluded that the germane induced oxide desorption plays a negligible role in the measured oxygen concentrations found at the buried Si / SiGe interfaces. It is, later, conclusively shown that the low temperature clean technique used to grow the ultra-sharp phosphorus profile does not depend on germane.

EFFECT OF HF CONCENTRATION AND HYDROGEN BAKES

A study of the HF concentration used in the last dilute HF dip of the wet clean on the surface quality was done. The wet cleaning described earlier was reformulated, in which

the HF concentration in the final 20 minute dilute HF dip used to strip the chemical oxide was varied from 50-0.1% (pH=0.4-3). After the HF dip, the wafer is moved to the load-lock from the chemical hood. The hydrogen passivated surface is exposed to laboratory atmosphere for 5-20 minutes after removal from the etch solution. High quality interfaces were achieved even after 15-20 minutes of exposure to air, indicated by intense PL from $Si_{1-x}Ge_x$ layers grown above the exposed surface. A monotonic increase in the relative PL intensity from the $Si_{0.8}Ge_{0.2}$ layer was found as the HF concentration was decreased from 0.4-3 (figure 1). Surface morphology roughens as the pH of the HF solution is lowered from 7.8 to 0.4 due to 111 micro-faceting of the etched silicon surface (15). The PL intensity dependence on pH may be linked to the 111 microfaceting of the surface because of the surface roughness at low pH, but chemical contamination of the surface can not be ruled out as an explanation.

Even after using the optimum HF concentration for the ex-situ clean the PL intensity is not as intense as from SiGe layers grown on in-situ grown buffer layers without interrupt. In order to further improve the surface quality after the ex-situ clean we examine in-situ hydrogen baking to further clean the surface. As a first step the condition under which hydrogen does not add more contamination to the interface is examined. To determine whether the hydrogen ambient in the growth chamber contributes any contamination to the wafer surface. After the growth of epitaxial buffer layers the growth was interrupted. The reactor pressure was set between 0.5-250 torr in pure H_2 and the wafers were heated to 700°C for 2-15 minutes. The pressure was then adjusted to 6 torr and DCS was added to resume growth. For pressures equal to and above 6 torr detection of oxygen and carbon were limited by the sensitivity of SIMS. It is believed that at 700°C the desorption rate of oxygen and carbon from the silicon surface is very slow (4), so these measurements only reflect adsorption. Adsorption rates were determined from the integrated carbon and oxygen concentrations found at the interface, determined by SIMS, divided by their respective annealing times (figure 2). The observed increase in detected oxygen and carbon measured at the test interfaces exposed at hydrogen pressures below 6 torr is thought to be due to reduced hydrogen termination of the silicon surface at lower hydrogen pressures (16). The increase in open silicon surface sites, at low hydrogen pressures, will increase the sticking coefficient of impinging oxygen and hydrocarbons from the reactor atmosphere during the hydrogen bake, and therefore leading to increasing oxygen and carbon absorption rates.

To further clean the surface, after the optimum dilute HF dip (0.1% HF), wafers were then subjected to an in-situ bake in hydrogen before growing an epitaxial SiGe/Si cap. A maximum temperature of 800°C was used to minimize the thermal budget of the in-situ clean. A 700°C, 10 minute bake at 6 torr was found to give no improvement of the quality of the Si/SiGe interface as probed by PL from the SiGe layer (figure 2) consistent with ref. 4 and 5. The wafer is heated to 800°C for 1 minute at 0.5-250 torr after which the temperature is reduced to 625°C while stabilizing the pressure to 6 torr. After both pressure and temperature are stable DCS and GeH_4 were injected into the reactor to begin growth of the SiGe / Si capping layer. PL from the thin 200 Å $Si_{.8}Ge_{.2}$ as a fuction of pressure is shown in figure 3, and the corresponding integrated oxygen and carbon concentrations, determined by SIMS, for the same samples are shown in figure 4. The PL

intensity is clearly brightest for 1-10 torr bakes, and improved over the ex-situ clean without the hydrogen bake, although the intensity is still slightly dimmer than the PL from an uninterrupted growth of a SiGe/Si layer grown on a silicon buffer layer. Oxygen and carbon concentrations are found to be lower than those without hydrogen bake, representing a clear reduction of oxygen and carbon over only the ex-situ clean. A 2 minute hydrogen bake at 800°C at 10 torr resulted in an interface indistinguishable, by SIMS, from that of an uninterrupted growth.

PHOSPHORUS PROFILE AND DEVICE APPLICATION

The combination of an ex-situ clean and an in-situ clean, have been used to demonstrate sharp phosphorus profiles with low interface contamination. This process has been used to make an ultra-sharp profile for the channel doping in a vertical p-channel MOSFET. Channel lengths as short as 25 nm have been obtained, which rely on the sharp edge of the phosphorus profile (17). The process flow used to grow the ultra-sharp phosphorus profile started first with growth of a thin 300 Å phosphorus doped layer grown at 700°C at a growth rate of 30 Å/min and a phosphorus concentration of $10^{18}/cm^3$ at 6 torr. The growth was halted immediately after the growth of the phosphorus layer was finished (after the phosphine was turned off). The phosphorus doped sample was then removed from the reactor and a blank wafer was loaded into the reactor on the single wafer quartz sample holder. The reactor is then purged by growing an undoped sample, while the phosphorus doped sample surface is oxidized in H_2SO_4:H_2O_2 (3:1) solution at 70°C and then etched in a dilute HF:DI (1% HF in DI) dip. This process was repeated several times in order to insure that the potentially phosphorus rich surface was completely removed. After the last HF dip the wafer was reloaded, as described earlier into the purged reactor. To obtain a contamination free surface with minimal phosphorus diffusion the top surface of the sample was subjected to a short 1 minute, 800°C hydrogen bake at 10 torr, after which the pressure was reduced to 6 torr and the temperature was dropped to 700°C. DCS was injected into the growth chamber as soon as the temperature and pressure stabilized, approximately 30 seconds after the hydrogen bake was finished, initiating the growth of a thin intrinsic silicon layer grown directly above the etched surface to complete the sharp turn-off of the phosphorus profile. In figure 5a, the phosphorus profiles of the uninterrupted process is compared with the interrupted process. The uninterrupted process clearly shows the long phosphorus concentration decay length of 200 nm / decade, whereas the interrupted process completely suppresses the autodoping effect and produces a phosphorus concentration decay length of 17 nm / decade. The oxygen and carbon concentrations at the interface, as seen in figure 5b, are below SIMS detection limits. The best, previously reported, phosphorus concentration decay length for low pressure chemical vapor deposition that is oxygen and carbon free at the top phosphorus edge, that the authors are aware of, is 100 nm / decade of phosphorus concentration (3).

CONCLUSION

In conclusion, phosphorus profiles were grown with a 17 nm / decade fall off at the top edge as measured by SIMS. The phosphorus profile was produced using an interrupt process, which included removing the wafer from the growth chamber to both purge the reactor and to etch the top surface of the sample, before intrinsic silicon was grown above the phosphorus layer. In order to produce high quality silicon epitaxy above the phosphorus doped layer while maintaining a low thermal budget for the ultra-sharp phosphorus profile, a low temperature cleaning technique was developed for the Princeton RTCVD system. A 1-2 minute, 800°C bake of the silicon surface in 10 torr of hydrogen is used to reduce oxygen and carbon concentrations at the interface to below SIMS detection limits, for high quality silicon epitaxy on the phosphorus surface leaving an interrupt interface nearly indistinguishable from an epitaxial layer grown without interrupt. This cleaning result is the lowest thermal budget, that the authors are aware of, for a low pressure chemical vapor system that reduces both carbon and oxygen below SIMS detection limits and is the shortest phosphorus concentration fall off with undetectable oxygen and carbon contamination near the phosphorus profile, known to the authors.

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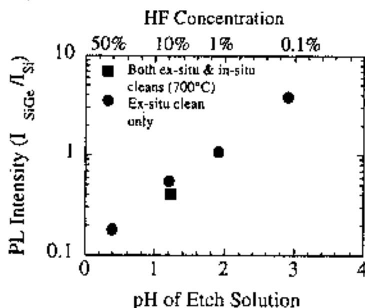

Figure 1. Photoluminescence ratio, which reflects interface quality, as a function of HF dip pH before the growth of the capping SiGe/Si layer. One sample was baked after the ex-situ clean (pH=1.3) at 700°C for 10 minutes in 6 torr of hydrogen before the SiGe/Si cap was grown.

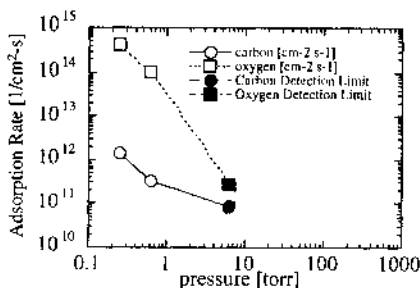

Figure 2 Oxygen and carbon adsorption rates in RTCVD reactor t 700°C as a function of hydrogen pressure. The points at 6 torr were limited by SIMS resolution.

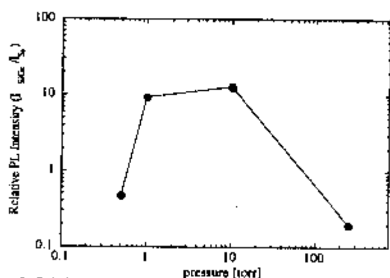

Figure 3. Relative photoluminescence intensity from SiGe layers grown directly above ex-situ cleaned silicon substrates exposed to an in-situ 1 minute bake at 800°C in 0.5-250 torr of hydrogen, before the SiGe/Si epitaxial cap is grown. The relative photoluminescence intensity from SiGe layers grown on in-situ grown buffer layers without interrupt are approximately 30-40.

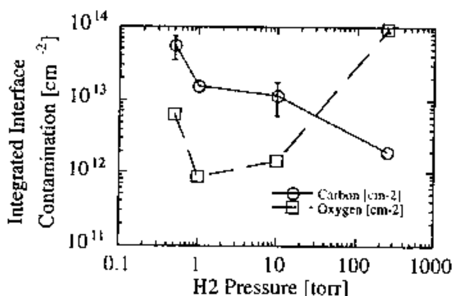

Figure 4. Oxygen and carbon concentrations, determined by SIMS, at the interface between the substrate surface and SiGe/Si cap, in the samples of figure 3. The oxygen and carbon concentrations are plotted as a function of hydrogen pressure during the in-situ 1 minute 800°C bake, before the SiGe/Si cap is grown on the ex-situ cleaned silicon substrate.

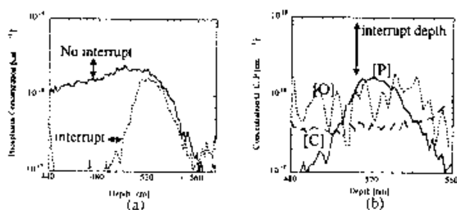

Figure 5. (a) phosphorus profiles grown at 700°C using phosphine with and without an interrupt process to suppress the phosphorus autodoping effect, showing improvement of phosphorus doping fall-off from 200 to 25 nm/decade. (b)Tthe carbon, oxygen and phosphorus profiles from the interrupt process. No carbon or oxygen are detected at the interrupt interface.