Technologies for Large-Area Electronics on Deformable Substrates

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Abstract

For large-area electronics to have an increasingly large-impact on consumer applications, flexible substrate technology and lower cost patterning technologies must be developed. In this paper, the mechanics of rolling and deforming thin foil substrates in two and three dimensions are discussed. The impact of such deformations on semiconductor devices and materials are presented. The effects of cylindrical deformation can be mitigated by using thin substrates, but spherical deformation requires device islands on soft substrates. For pattern formation, the transfer of ink down to a feature size of the order of microns has been demonstrated using a modified version of offset printing. While there are several practical issues which must be addressed, such as ink stability while drying, it appears possible to scale such printing to the micron scale and below.

Introduction

The conventional goal of the semiconductor industry is to make things small. However, there is an emerging market for large-area electronics, or "macroelectronics," where the product must be large by definition. These applications are generally driven by real world interfaces such as flat panel displays, large-area sensor arrays (e.g. X-ray imaging plates), MEMS arrays, etc. Current generations of these products are made on glass substrates using amorphous or polycrystalline semiconductor technology (typically amorphous or polycrystalline silicon). For future products, it is highly desirable that they be lightweight, flexible, and rugged. Furthermore, the drastic reduction of cost per unit area of these products is difficult as long as they are made with standard photolithography and etching. This paper will discuss two issues: novel substrate approaches and the mechanics to develop flexible and even three-dimensional surfaces, and the scaling of offset printing technology to small feature sizes.

Rollable and Deformable Substrates

Cylindrical Deformation

The most common amorphous silicon (a-Si) TFT's are made on glass substrates with a maximum process temperature of 300 – 350 °C. For lightweight flexible electronics, over the past few years many groups have developed a-Si TFT's on plastic (e.g. polyimide) substrates with a maximum process temperature of 110-200 °C [1-6], or even on stainless steel foil substrates (e.g 3 – 200 μm thick) [7,8]. For processing on stainless steel foil substrates, a planarizing and insulating oxide must first be deposited, but after that step processing is much more straightforward for a-Si TFT's than that on plastic. For example, there are no concerns about outgassing in vacuum systems, shrinkage (as with plastic), allowable process temperature, etc. Polysilicon TFT's with process temperatures of 950 °C have been successfully fabricated on steel foils [8]. The results described in the rest of this section of the paper are from amorphous silicon (a-Si) TFT's with a bottom gate, back-channel etch structure. After conventional fabrication on flat substrates, individual transistors were stressed mechanically by deforming the substrate in a cylindrical shape by bending it around a small diameter metal cylinder, whose radius was varied as low as 0.5 mm (Fig. 1).

When a thin film substrate is cylindrically deformed, the inside surface of the foil is in compression and the outside surface is in tension. If the mechanical stiffness of the TFT layers on the surface is small compared to that of the substrate [9], it is well known that for a radius of curvature ρ, the magnitude of the strain ε on the two surfaces is

$$\varepsilon = t / 2\rho \qquad (1)$$

where t is the thickness of the foil. In the middle of the foil is a so-called "neutral plane" where the strain is zero. Note that the strain in the surface layers, which will lead to failure of the devices made in these layers, can be reduced simply by reducing the substrate thickness. Because of the relatively small strains caused in these experiments (typically < 0.01), there was relatively little plastic flow in the substrates during deformation. The TFT's on both the stainless steel and polyimide substrates were measured both after fabrication and after being released from the cylindrical deformation. For TFT's on 25-μm stainless steel substrates, there was little change in their parameters for bending down to radii of 2.5 mm, corresponding to a surface strain of 0.5% [10]. For tighter radii of curvature, the TFT's failed before a noticeable shift in their characteristics was observed, with a typical failure mode being delamination of the TFT structure from the passivating oxide on the steel.

TFT's were also fabricated on 25-μm polyimide (Kapton E) substrates. In this case, the soft plastic substrate is "compliant," so the neutral plane shifts towards the TFT surface. This substantially reduces the strain in the TFT layer [11]. Fig 2 shows the change in transistor parameters of maximum on current, leakage current, threshold voltage, and field effect mobility in saturation after deformation, normalized by their respective values before deformation. When the TFT's were on the inward side of the foil, so that they were under compression, no change in characteristics was observed when the TFT's were deformed to a radius of 0.5 mm (corresponding to a surface strain of 2.2%) and released after one minute. When the TFT's were on the outside of the foil (under tension), a noticeable change was already observed at a strain of 0.5% (radius of ~ 2 mm). In this case the TFT film was beginning to crack, with the cracks running perpendicular to the strain direction, presumably as a strain release mechanism (Fig. 3). Up to a strain of 0.5%, however, no change in device characteristics was observed.

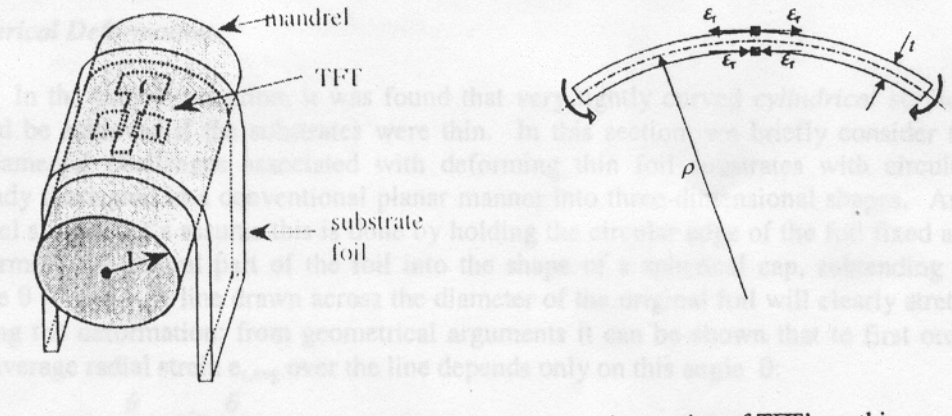


Fig. 1. Schematic diagram of cylindrical deformation testing of TFT's on thin foil substrates and of strain distribution.

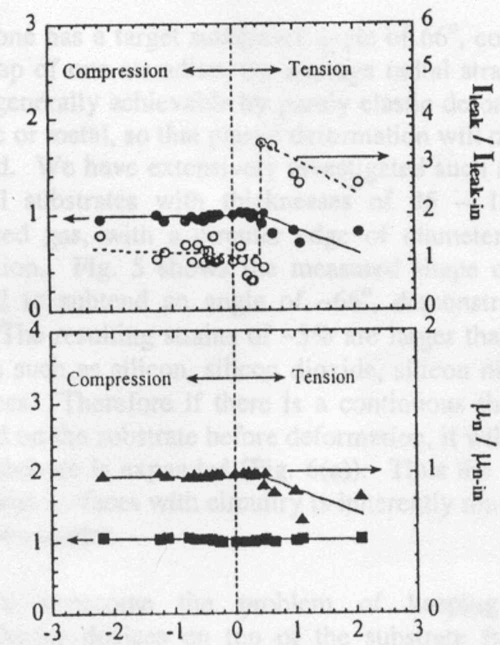


Fig. 2. Transistor parameters of a-Si TFT's on 25-micron polyimide substrates after one minute of cylindrical deformation and release, normalized to their values before deformation [11].

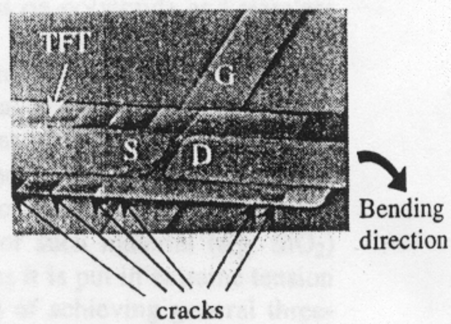


Fig. 3. Micrograph of TFT deformed under tension with cracks in the a-Si island [11]

Spherical Deformation

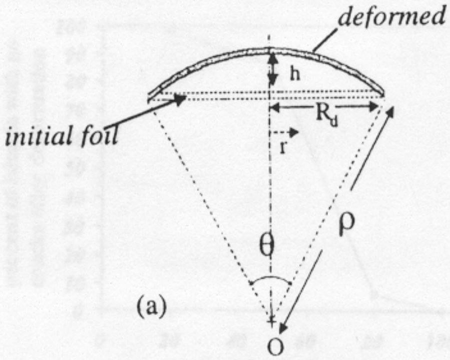
In the previous section, it was found that very tightly curved *cylindrical* surfaces could be achieved if the substrates were thin. In this section, we briefly consider the fundamental challenges associated with deforming thin foil substrates with circuitry already fabricated in a conventional planar manner into three-dimensional shapes. As a model system, let's assume this is done by holding the circular edge of the foil fixed and deforming the central part of the foil into the shape of a spherical cap, subtending an angle θ (Fig. 4). A line drawn across the diameter of the original foil will clearly stretch during the deformation; from geometrical arguments it can be shown that to first order the average radial strain $e_{r,avg}$ over the line depends only on this angle θ:

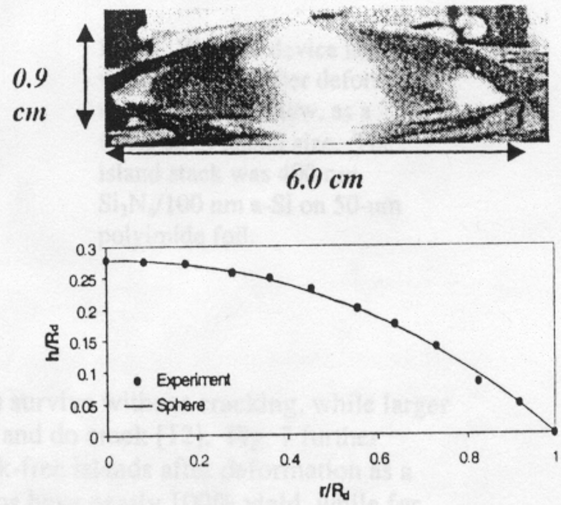
$$\varepsilon_{r,avg} = \frac{\frac{\theta}{2} - \sin\frac{\theta}{2}}{\sin\frac{\theta}{2}} \approx \frac{\theta^2}{24} \qquad (2)$$

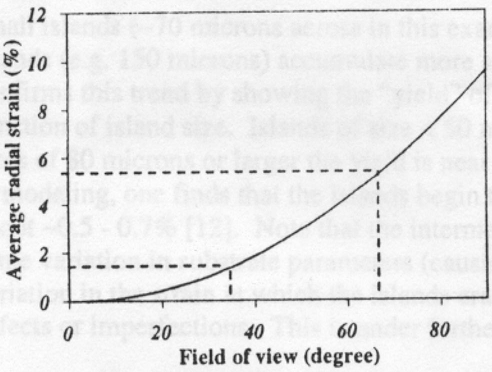
This strain is independent of the foil thickness, so that unlike the case of cylindrical deformation, reducing the substrate thickness will not reduce the strain for a given shape.

If one has a target subtended angle of 66°, corresponding to a solid angle covered by the cap of one steradian, the average radial strain is 5.6%. Such a strain is beyond what is generally achievable by purely elastic deformation with substrate materials such as plastic or metal, so that plastic deformation will occur and the foil will be permanently deformed. We have extensively investigated such structures on polyimide and stainless steel foil substrates with thicknesses of 25 – 100 μm. They were deformed by pressurized gas, with a circular edge of diameter 5-8 cm clamped fixed during the deformation. Fig. 5 shows the measured shape of such a 25-micron thick steel foil deformed to subtend an angle of ~66°, demonstrating that a spherical shape indeed results. The resulting strains of ~5% are larger than the fracture limits of brittle device materials such as silicon, silicon dioxide, silicon nitride, etc, which are on the order of 1% or less. Therefore if there is a continuous thin film of such material (e.g. SiO_2) deposited on the substrate before deformation, it will crack as it is put in extreme tension as the substrate is expanded (Fig. 6(a)). Thus the problem of achieving general three-dimensional surfaces with circuitry is inherently more complicated than that of the rolled foils shown earlier.

To overcome the problem of keeping previously fabricated thin film semiconductor devices on top of the substrate from cracking when the substrate is deformed, islands of "hard" semiconductor device material (100 nm of amorphous silicon on top of 400 nm of silicon nitride) were patterned on top of a "soft" polyimide substrate before deformation. For comparison, the Young's moduli of silicon and polyimide are ~200 and ~10 GPa, respectively. Furthermore, plastic flow in the polyimide begins already at a very low strain. Therefore the substrate can deform and then flow under the island as the foil is deformed, minimizing the strain in the island and preventing it from cracking. Optical micrographs of a-Si/Si_3N_4 islands on 50-micron polyimide substrates deformed at 150 °C (to further soften the polyimide) are shown in Fig. 6 (b-c). Note that



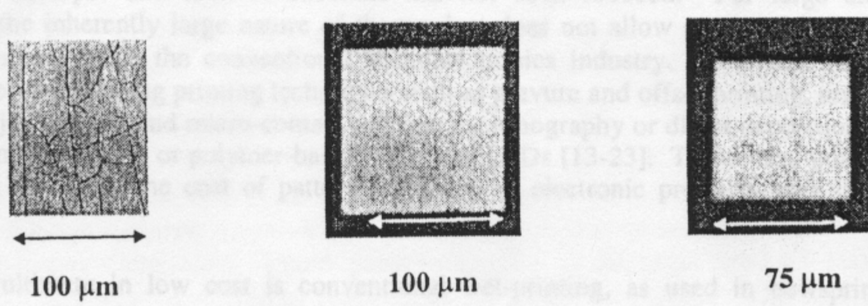




(b)

Fig. 5. Stainless steel foil after deformation by gas pressure, and measured shape of height vs. radius.

Fig.4. (a) Schematic diagram of foil deformation into a spherical cap, and (b) average radial strain across the foil after deformation as a function of the field of view θ).



(a) (b) (c)

Fig. 6. Micrographs after spherical deformation to ~65° field of view of (a) unpatterned 0.5 micron of SiO_2 on 25-µm stainless steel foil, (b) 400 nm Si_3N_4/100 nm a-Si on 50-um polyimide foil patterned to a ~120-µm island, and (c) the same layer structure as (b) patterned to a ~75-µm island.

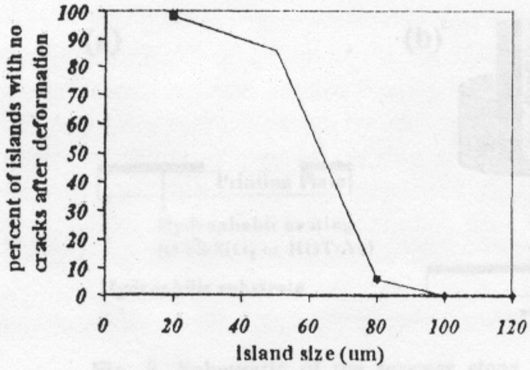


Fig.7. Yield of device islands without cracks after deformation to ~65° field of view, as a function of island size. The island stack was 400 nm Si_3N_4/100 nm a-Si on 50-um polyimide foil.

small islands (~70 microns across in this example) survive without cracking, while larger islands (e.g. 150 microns) accumulate more strain and do crack [12]. Fig. 7 further confirms this trend by showing the "yield" of crack-free islands after deformation as a function of island size. Islands of size < 50 microns have nearly 100% yield, while for sizes of 80 microns or larger the yield is near zero. Comparing the experimental results to modeling, one finds that the islands begin to fail when the highest strain in them is about ~0.5 - 0.7% [12]. Note that the intermediate yield for intermediate sizes implies some variation in substrate parameters (causing a variation in the island strain), or a variation in the strain at which the islands crack, implying a failure mechanism related to defects or imperfections. This is under further investigation.

Offset printing of UV-curable polymers

The microelectronics industry is continuously pushing to reduce the minimum feature size of electronic devices. While this trend has drastically reduced the cost per feature, the cost per unit area of substrate has not been reduced. For large area electronics, the inherently large nature of the product does not allow one to reduce the cost by shrinking as in the conventional microelectronics industry. Therefore many groups are today exploring printing techniques such as gravure and offset printing, screen printing, inkjet-printing and micro-contact printing for lithography or direct deposition of patterned semiconductor- or polymer-based TFTs and LEDs [13-23]. The central goal of this work is to reduce the cost of pattern formation of electronic products over large areas.

The ultimate in low cost is conventional wet-printing, as used in newsprint, magazines, etc. Therefore we have tried to scale conventional offset printing down to the micron size range. This wet printing technique involves transferring liquid inks from a flat and chemically patterned surface onto an unpatterned target substrate [24-27]. As suggested by Fig. 8, there are four technological issues that arise in this process: (1) fabrication of printing plates, (2) deposition and distribution of ink on the plates for pattern definition, (3) rheological and surface control of ink patterns during printing, and (4) rapid stabilization of printed patterns.

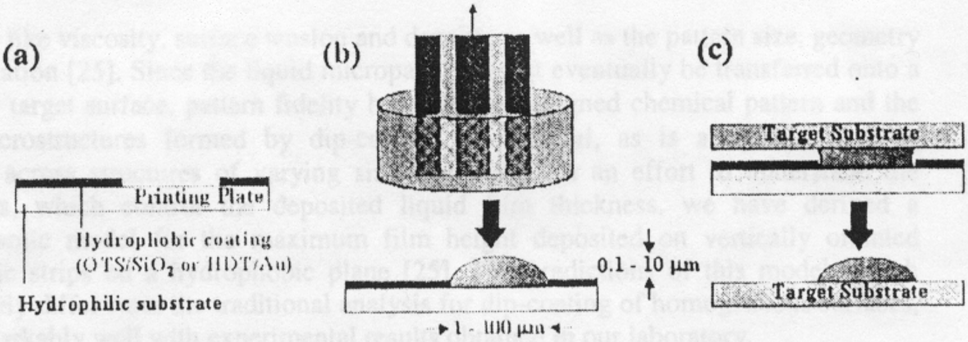


Fig. 8. Schematic of the process steps for offset printing of electronic materials. (a) Fabrication of the printing plates. A hydrophilic substrate such as oxidized silicon or glass is coated with a hydrophobic monolayer of octadecyltrichlorosilane (OTS) or hexadecanethiol (HDT), which is selectively removed by reactive ion etching or deep-UV irradiation. (b) Deposition of the ink on the printing plate by dip-coating. Depending on the feature size, which ranges between 1-100 µm, and deposition parameters, the thickness of the ink structures ranges between 0.1-10 µm. (c) Ink transfer from the stamp to an unpatterned target substrate.

Printing Plate Fabrication

The samples we have used in our studies are prepared from [001]-oriented *p*-type doped silicon wafers or glass slides using optical lithography. The silicon wafers are first cleaned by immersion in a solution of concentrated H_2SO_4 and H_2O_2 (volume ratio of 7 to 3) at 90°C for 30 min, thoroughly rinsed in ultrapure, deionized water (18 MΩ−χµ) and then coated with a self-assembled monolayer of octadecyltrichlorosilane (OTS) [28]. The silane groups of the OTS molecules react with the native SiO_2 layer of the silicon surface forcing the hydrophobic alkane tails to orient in the opposite direction thus producing a uniform hydrophobic surface. The contact angles of glycerol and water on OTS are measured to be 95° ± 3° and 112° ± 3°, respectively, in agreement with previous measurements [29].

The next process step is the definition of a surface pattern via exposure of the OTS layer through a chromium mask on a fused silica glass substrate with intense ArF-laser radiation (wavelength λ = 193 nm, pulse energy E = 28 mJ, pulse rate f = 9 Hz) for ~ 10 minutes. The UV light induces breakage of the bonds between the OTS molecules and the SiO_2 surface [30] effectively removing the OTS from exposed regions. An alternative method to this selective deep-UV photocleavage of the OTS molecules from silicon or glass surfaces is reactive ion etching with a low-power oxygen plasma, preceded by conventional photolithography.

Ink deposition by dip-coating

The thickness of a liquid coating deposited on the hydrophilic portions of a chemically micropatterned surface by the method of dip-coating depends on the liquid properties like viscosity, surface tension and density, as well as the pattern size, geometry and orientation [25]. Since the liquid micropatterns must eventually be transferred onto a secondary target surface, pattern fidelity between the designed chemical pattern and the liquid microstructures formed by dip-coating is essential, as is a uniform coating thickness across structures of varying size and shape. In an effort to understand the parameters, which control the deposited liquid film thickness, we have derived a hydrodynamic model for the maximum film height deposited on vertically oriented hydrophilic strips on a hydrophobic plane [25]. The predictions of this model, which significantly differ from the traditional analysis for dip-coating of homogeneous surfaces, agree remarkably well with experimental results obtained in our laboratory.

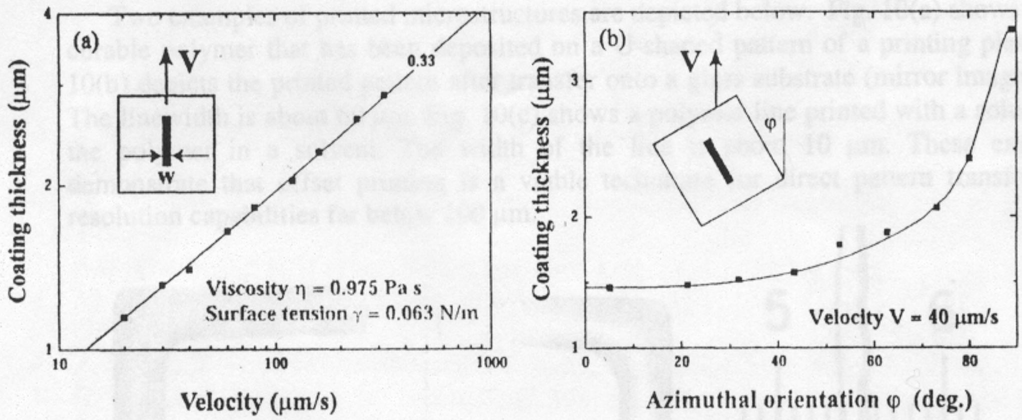


Fig. 9. (a) Thickness of liquid coated line as a function of plate withdrawal speed V. The solid line represents a power-law relation $h \sim V^{\beta}$ with $\beta = 0.33$, as predicted by the theoretical model. (b) Thickness of liquid coated line as a function of dipped line orientation. Note nearly cosntant thickness up to a 45° angle.

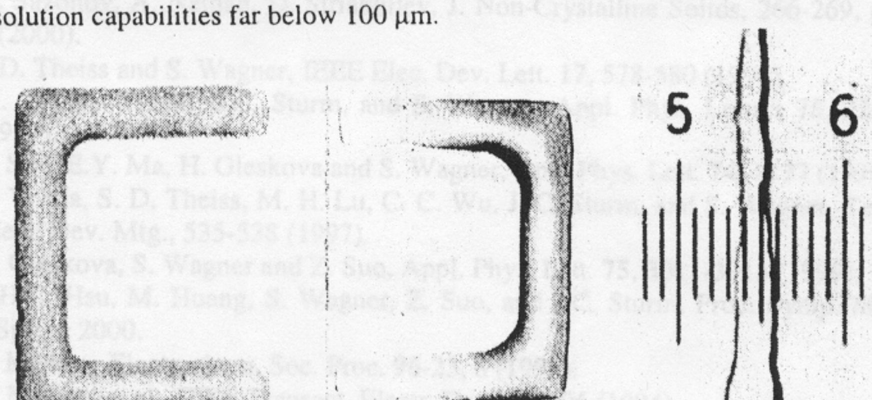
Figure 9(a) shows the coating thickness h on narrow hydrophilic lines as a function of the speed of withdrawal V during dip-coating of glycerol [$C_3H_5(OH)_3$]. The coating thickness increases with increasing withdrawal velocity according to $h \sim V^{\beta}$ with $\beta = 0.33$. The theoretical model predicts an exponent of $\beta = 1/3$. Fig. 9(b) shows the dependence of the coating thickness h on the azimuthal orientation φ of hydrophilic lines. As can be seen, h does not vary much for tilt angles $\varphi < 45°$. Thus, the pattern orientation does not influence the entrained film thickness up to an angle of 45 degrees, which means patterns of a wide range of orientation will be coated with the same thickness.

Aspects of ink transfer

When liquid is transferred to a non-porous substrate and the separation of the plates becomes small, the liquid is squeezed between the plates beyond the boundaries of the hydrophilic regions [26]. Therefore, the spacing of the printing plates must be controlled and maintained above a certain minimum value. A suitable solution is to place rigid spacer elements on the printing plate, which mechanically impede too close a contact between stamp and target surface. These spacers must be hydrophobic or they will attract ink during the deposition process. The spacer thickness must be tuned such that the contact line on the target substrate matches the designed pattern on the stamp as closely as possible.

Since contact between the stamp and target plates leads to a redistribution of liquid, the required spacer thickness depends on the pattern geometry. Two limiting cases are straight, long lines, and circular pads. For lines the redistribution of ink occurs only in the direction transverse to the channels, while for the circular pads, the ink spreads radially in-plane. Assuming identical ink profile heights for circles and lines, the plate separation required to maintain registry of designed and printed dimensions is about 25% smaller for circles than for lines [26].

Two examples of printed microstructures are depicted below. Fig. 10(a) shows a UV-curable polymer that has been deposited on a U-shaped pattern of a printing plate. Fig. 10(b) depicts the printed pattern after transfer onto a glass substrate (mirror image) [27]. The linewidth is about 60 μm. Fig. 10(c) shows a polymer line printed with a solution of the polymer in a solvent. The width of the line is about 10 μm. These examples demonstrate that offset printing is a viable technique for direct pattern transfer with resolution capabilities far below 100 μm.



(a) (b) (c)

Fig. 10. (a) UV-curable polymer deposited on a U-shaped pattern on a printing plate and (b) pattern after transfer to a glass surface. The width of the lines is about 60 μm. (c) Polymer line (printed as a solution) after solvent evaporation. The separation between the labels "5" and "6" is about 50 μm.

Summary

The mechanics of creating rolled and arbitrary three dimensional electronic surfaces after fabricating electronics in a conventional planar fashion on thin foil substrates has been discussed. Rolling can be achieved without damaging electronics on substrate surfaces by reducing the thickness of the substrate and using compliant substrates. For arbitrary shapes such as spherical caps, thin substrates are not sufficient to reduce the strain in the device materials, and alternate approaches like islands on soft substrates are required. To develop low cost patterning technologies, the scaling of offset printing has been investigated. Making and inking masks is now fundamentally understood. Solutions are being developed for practical issues associated with the transfer of the ink.

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