

Enabling Technologies for Plastic Displays

J.C. Sturm*, H. Gleskova*, T.N. Jackson**, S.J. Fonash***, and S. Wagner*,

*Center for Photonics and Optoelectronic Materials (POEM), Department of Electrical Engineering,
Princeton University, Princeton, NJ 08544 USA

** Department of Electrical Engineering, Pennsylvania State University, University Park, PA
16802

*** Materials Research Institute, Pennsylvania State University, University Park, PA 16802

ABSTRACT

This paper demonstrates the state of critical technologies for the integration of Thin Film Transistors (TFTs) onto plastic substrates for display applications. The transistor technologies examined include polycrystalline silicon, amorphous silicon, and organic semiconductor TFTs. Fundamental work in new regimes of operation enabled by plastic substrates, such as the effect of rolling and 3-D deformation are also developed, leading to design guidelines. Finally, printing approaches for organic semiconductors are shown to demonstrate potential paths towards roll-to-roll display manufacturing. Altogether, the results point toward the possibility of printing transistors anywhere and bending them into nearly any shape.

Keywords: TFT, thin-film transistor, polysilicon, polycrystalline silicon, amorphous silicon, plastic, organic semiconductor, deformation, rolling, printing

1. Introduction

Plastic substrates for displays have the advantages over glass that they are lightweight, potentially thinner, potentially flexible and deformable, rugged and less prone to breakage, and more amenable to future roll-to-roll manufacturing techniques. These product and manufacturing advantages make it highly desirable to develop critical display technologies on such substrates. Of critical importance are technologies for transistors for pixel electronics as well as peripheral control circuitry. This paper examines developments in amorphous silicon, polycrystalline silicon, and organic semiconductor TFTs on plastic substrates. For silicon TFT materials the challenges are process integration challenges relating to the maximum process temperatures for plastic (for polysilicon), and in the fundamental effects of bending and deformation on TFT performance (for amorphous silicon). Transistors and circuitry on plastic can now be successfully rolled to mm-scale radii or deformed into 3-D shapes. An alternative approach for low temperature TFTs are organic semiconductors, which are deposited on non-crystalline substrates at low temperatures, and shown here to be capable of moderately complex circuits at MHz speeds. These semiconductors are amenable to direct printing techniques, as is demonstrated through the dry-printing of organic dyes into a polymeric organic semiconductor for the full color integration of organic LED's.

2. High Performance Polycrystalline TFT's on Plastic Substrates by Transfer Techniques

Even though poly-Si TFTs on flexible plastics are very attractive for applications such as wearable/mobile information displays and large area electronics due to their light-weight, flexibility, and shock-resistance, the fabrication of high performance transistors on plastics is extremely challenging for several reasons. First of all, the maximum process temperature must be lower than the plastic substrate's glass transition temperature (typically <300C), which is very low compared to the conventional semiconductor processing temperatures. This inherent temperature limitation leads to low crystallinity of the active film and poor electrical performance (low carrier mobility and device instabilities). Secondly, due to microscopically rough and uneven surface of most plastics, it is difficult to adopt conventional microelectronic processing techniques like lithography and surface planarization. Finally, device processing on flexible substrates can suffer from a lack of reproducibility and manufacturability due to their general mechanical and thermal instabilities during fabrication processing.

We previously reported a novel separation process, where we spin-coated a high temperature ($T_g \sim 300^\circ\text{C}$) polymer film on a mother substrate, subsequently built TFT device, and separated the plastics with device on it [1]. Using this separation approach we were able to fabricate low temperature a-Si TFT on plastic substrate with little modification from the fabrication processes for conventional substrates such as glass and silicon wafer. This novel process solved the second and third issues of plastic substrate.

However, fabrication of any high temperature (so high performance) TFT on plastics is still limited by the plastic material. So, we have come up with a more advanced approach, which decouples high temperature processes from the plastic materials involved. Based on previous separation idea, we applied the plastic film after the completion of device fabrication on conventional substrates and transferred the device from the mother substrate to the plastic film by removing a sacrificial release layer between device and the substrate. This separation process circumvents the inherent limitations of plastics. Figure 1 depicts the schematic of the process flow for this separation technology.

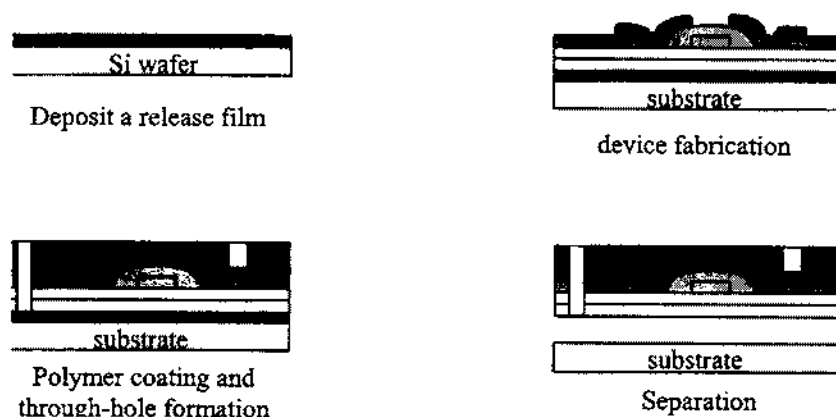


Figure 1. Schematic of our fabrication process flow for high temperature and high performance poly-Si TFT on plastics.

As seen in Figure 1.1, prior to device fabrication, a release (sacrificial) layer is deposited on an oxidized silicon wafer, which we call the 'mother substrate'. We use an as-deposited column/void network film [2] which has very high surface-to-volume ratio like porous silicon. A 3000\AA thick silicon oxide (low temperature oxide; LTO) capping layer is deposited on top of the sacrificial release layer using a chemical deposition (CVD) system. A 1000\AA thick a-Si precursor film is deposited in a low pressure chemical vapor deposition (LPCVD) system using SiH_4 source gas at 300mT and 530°C . Metal (nickel) seeds are formed on the precursor film and annealed at 570°C for metal induced lateral crystallization (MILC). During the MILC process, polysilicon crystals grow laterally in the direction of carrier transport in the channel region, resulting in polysilicon grain structure virtually free of large angle grain boundaries. The active region is patterned using optical lithography using an e-beam generated chrome mask with a proximate type aligner. Subsequently, pattern is transferred on the active polysilicon film using reactive ion etching (RIE). A 1000\AA thick gate oxide is grown on the active region using a diffusion furnace with dry oxygen gas at 1100°C . A 3000\AA thick gate electrode silicon film is deposited at 530°C with the LPCVD reactor. After patterning the gate electrode using photolithography and RIE, the source and drain are self-aligned and doped with boron ion implantation (11B , 33KeV , $1\text{E}15\text{cm}^{-2}$) for the p-channel TFT. The gate electrode is implanted at the same time. The dopants are activated at 850°C for 30 minutes in nitrogen ambient in a tube furnace. After source, drain, and gate contact windows are opened using photolithography and oxide wet etching, nickel metal pads are formed using ebeam evaporation and lift-off process. Figure 2 shows the transfer characteristics of the high temperature poly-Si TFTs fabricated using the above process sequence.

This device exhibits a linear field effect mobility (holes) of $174\text{ cm}^2/\text{V}\cdot\text{s}$, on/off ratio of $(I_{\text{on}}/I_{\text{off}}) > 10^8$ @ $V_{\text{ds}} = -0.1\text{V}$, off current of $< 10^{-13}\text{ A/micron width}$, sub-threshold slope of $< 200\text{mV/dec}$, and threshold voltage of -1.1V . These results are in many ways comparable to p-channel FETs in bulk silicon made with CMOS technologies which

require process temperatures on the order of 1000°C. Fig 3. shows the finished devices on plastic substrates after transfer.

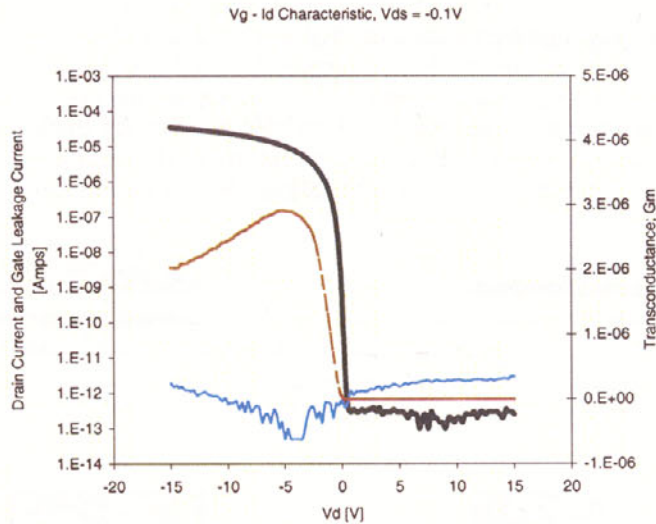


Figure 2. Transfer characteristics of a high temperature p-channel poly-Si TFT with channel length/width = 20 μm / 100 μm at $V_{ds} = -0.1\text{V}$

The TFT devices were separated using KOH (25%) solution at 65°C (5min). During this release process, the sacrificial column/void network film was selectively removed. After the separation, I_d - V_g characteristics were rechecked and showed no sign of degradation. Figure 3(a) is an optical micrograph (top view) of the device after separation. It shows through-holes around the devices (served as chemical conduit during the separation step, see Figure 1), and source/drain/gate contacts (serve as electrical probing pads). Figure 3(b) shows a piece of a transferred device on plastic, which was attached to another plastic tape.

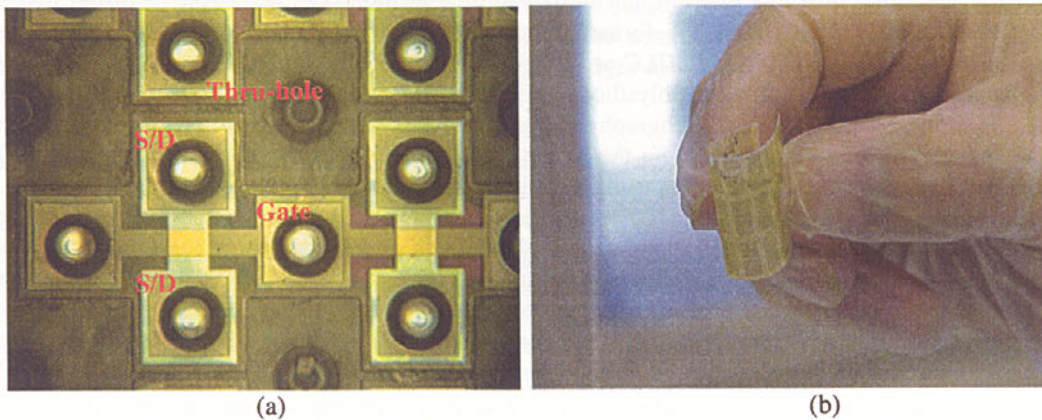


Figure 3. (a) Top view of optical micrograph of transferred device showing device structure and through holes around device. Gate/source/drain contact pads are also shown (b) transferred device on the thin plastic.

3. Organic TFTs on Plastic Substrates

3.1 Introduction

Organic semiconductor thin film transistors (OTFTs) have received increasing attention in recent years. The use of organic semiconductors as the active layer in thin film transistors (TFTs) provides advantages over conventional thin film active layer materials such as hydrogenated amorphous silicon (a-Si:H), including reduced processing temperature. This allows the use of inexpensive substrate materials of arbitrary size and temperature compatibility, including flexible polymers and perhaps even cloth or paper. Potential applications for organic TFTs include pixel access devices in active matrix displays, and low cost electronics for smart cards or merchandise tags [3-6].

OTFTs have been demonstrated using a variety of organic semiconductors, including both polymers and small molecule materials. To date, OTFTs fabricated using pentacene as the active layer material have shown the best performance [7-8]. For pentacene OTFTs on rigid substrates we have demonstrated carrier field-effect mobility greater than $3 \text{ cm}^2/\text{V}\cdot\text{s}$, subthreshold slope less than $0.4 \text{ V} / \text{decade}$, near-zero threshold voltage, and on/off current ratio larger than 10^8 . All these characteristics are similar to or better than those typically obtained for a-Si:H TFTs.

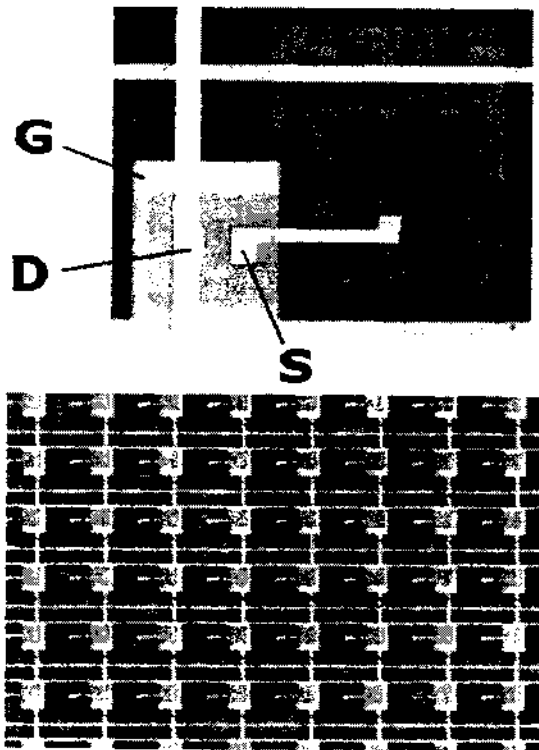


Fig. 4. OTFT single pixel and pixel array section fabricated on polymeric substrate.



Fig. 5. PEN OTFT substrate with devices, circuits and PDLC test displays.

3.2 Polymer Substrate Device Fabrication

Although roll-to-roll processing is attractive for low-cost manufacturing-scale OTFT display fabrication, for simplicity polyethylene naphthalate (PEN) substrates were mounted to glass carriers for this work. Prior to mounting, the PEN substrates were pre-shrunk at $150 \text{ }^\circ\text{C}$ for two hours. After substrate mounting, indium-tin oxide (ITO) pixel electrodes, nickel gate electrodes, a silicon dioxide gate dielectric layer, and palladium source and drain contacts were all deposited by ion-beam sputtering and patterned by photolithography and lift-off. Before pentacene active layer

deposition the silicon dioxide gate dielectric was vapor treated with octadecyltrichlorosilane to improve device performance. Pentacene was deposited by thermal evaporation with a deposition rate near 0.5 \AA/s and with the substrates held at 60 C . Prior to the active-layer deposition, the pentacene was purified by temperature-gradient vacuum sublimation.

Because pentacene, like many organic semiconductors, is degraded by exposure to most common solvents, an aqueous-based photolithographic process was used to pattern the pentacene active layers. A thin layer of polyvinyl alcohol (PVA) photosensitized with chromium was applied to the pentacene active layer by spin casting. The device active area is exposed to UV light through a mask (as in conventional photolithography) and the unexposed PVA is removed by development in water. The patterned PVA is then used as a mask to pattern the pentacene active layer using an oxygen plasma.

3.3 Results

The process described above has a maximum process temperature of 110°C after the pre-shrink step. Using this process we have fabricated pentacene OTFTs on PEN substrates with field-effect mobility as large as about $2 \text{ cm}^2/\text{V-s}$. Typical mobility is $0.5 - 1 \text{ cm}^2/\text{V-s}$ with on/off current ratio, subthreshold slope, and threshold voltage acceptable for display and circuit fabrication. In addition, the available current drive is sufficiently large that these OTFTs can easily serve as the drive transistor for active matrix OLED displays. Fig. 4 shows an OTFT pixel with the TFT electrodes labeled and a section of a pixel array. Fig. 5 shows a completed PEN substrate with pentacene OTFT devices and circuits. The substrate also has several small polymer dispersed liquid crystal (PLDC) test displays (the milky area is the PLDC material sandwiched between the bottom PEN active substrate and an ITO coated mylar top substrate). The PLDC allows a simple reflective display and avoids problems with plastic substrate birefringence.

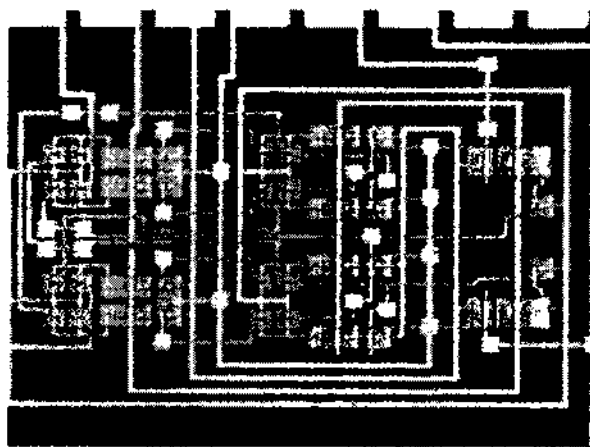


Fig. 6. OTFT divide-by-two circuit.

The flexible substrate pentacene OTFT process has also been used to fabricate analog and digital circuits. Using ring oscillators, a propagation delay as low as 37 \musec per stage was measured for circuit bias voltages of 20 V and $< 50 \text{ \musec}$ per stage for bias voltage as low as 8 V . Fig. 6 shows an optical micrograph of an OTFT divide-by-two frequency divider. The circuit uses 48 transistors and has a maximum clock frequency of 1.1 kHz .

The pentacene transistors used in the circuits described here are slightly depletion mode devices. For digital circuits this requires the use of a level shift stage, which limits the circuit speed. We have also fabricated circuits using OTFTs with naphacene active layers. Naphacene OTFTs are enhancement mode devices, and naphacene OTFT digital circuits do not require level shifting between stages. We have fabricated naphacene OTFTs with field-effect mobility as large as $0.12 \text{ cm}^2/\text{V-sec}$. Although this mobility is about one order of magnitude lower than the pentacene OTFTs described above, propagation delay less than 30 \musec per stage was measured for naphacene OTFT ring oscillators fabricated without level shift stages; significantly less than the delay measured for OTFT circuits with level shift stages. When used as pixel select transistors in active matrix displays, level shifting is not required even for depletion mode devices since the gate drive can be adjusted as needed. This allows much faster device operation, and rise and fall time below 1 \musec have been measured for directly driven pentacene inverters.

Naphacene OTFTs can also be used as phototransistors. Fig. 7(a) shows a plot of the square root of drain current as a function of gate-to-source voltage for a naphacene OTFT with and without illumination (a probe station microscope light source was used for illumination). The OTFT is biased in the saturation region of operation with a drain-to-source voltage of -40 V . With no illumination, the device has an extracted field-effect mobility near $0.12 \text{ cm}^2/\text{V-s}$ and a threshold voltage of -3 V . With illumination, the extracted field-effect mobility is near $0.07 \text{ cm}^2/\text{V-s}$ and

the threshold voltage shifts to a positive value of 14 V. Fig. 7(b) shows a plot of drain current as function of gate-to-source voltage for the OTFT biased in the saturation region of operation with a drain-to-source voltage of -40 V. In the subthreshold region the light induced current modulation ratio is as large as 10^5 . The large photosensitivity may allow naphthacene OTFTs to be used to control display response to ambient illumination, or perhaps even as image sensors.

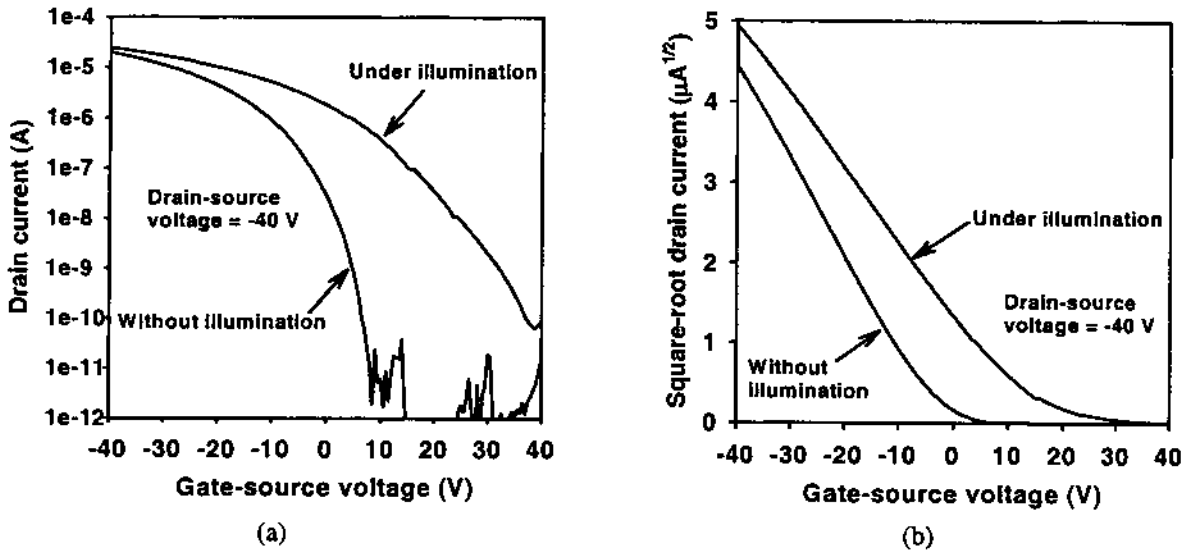
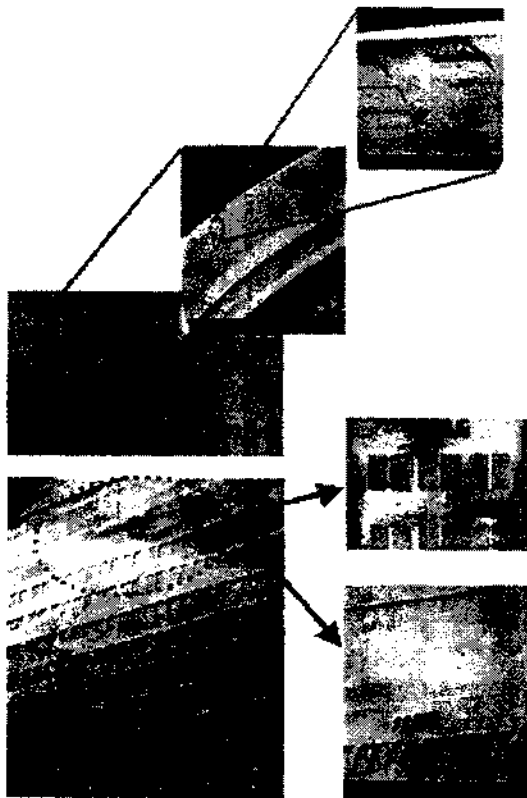


Fig. 7. Characteristics of naphthacene thin film phototransistor with and without illumination: (a) I_D vs. V_{GS} and (b) $\sqrt{I_D}$ vs. V_{GS} .



3.4 Future Directions

The low temperature and simple processing required for OTFT devices and circuits allows display and circuit fabrication on arbitrary substrates, including polymers and perhaps even paper or cloth. Fig. 8 shows simple OTFTs fabricated on a key ring and on a piece of a cotton-polyester bed sheet. These and related results [3-8] point to the possibility of fabricating displays and thin film electronics anywhere.

Fig. 8. Simple OTFTs fabricated on a key ring (top) and on a cotton-polyester bed sheet (bottom).

4. Fundamental Effects of Bending and 3-D Deformation of a-Si TFTs on Plastic Substrates

4.1 The need to understand the performance of a-Si:H TFTs while under strain

Flexible TFT backplanes are needed for large-area curved electronic screens, electronic paper, smart labels, and displays for vehicular applications. Depending on the application, the backplane, and the whole display, will be subjected to some degree of tension or compression due to external bending of the display. Display substrates may be of plastic [9-16] or stainless steel [17].

Even though the amorphous silicon thin-film transistor (a-Si:H TFT) is the common pixel switch in active matrix backplanes, not much is known about its electrical performance during bending (strain). We have shown that the strain in a-Si:H TFTs from bending can be substantially reduced if very thin and/or compliant substrates are used [18-20]. We also have observed that a-Si:H TFTs fabricated on Kapton at 150°C respond differently to tensile and compressive strain. They are found to function properly *after* the application of tensile strain of up to ~ 0.5% (where they fail mechanically) and *after* compressive straining of up to ~ 2% (with no failure observed so far) [21]. In this paper we report changes in the electron field effect mobility in a-Si:H TFTs *during* the application of compressive or tensile strain.

4.2 Transistor structure. Technique for electrical evaluation under mechanical strain

We fabricated arrays of a-Si:H TFTs on 51 μm thick polyimide at the temperature of 150°C. First, the polyimide substrate was coated on both sides with a 0.5 μm thick layer of SiN_x . All TFTs had the following structure: ~ 100 nm thick Ti/Cr layer as gate electrode, ~ 360 nm of gate SiN_x , ~ 100 nm of undoped a-Si:H, 180 nm of passivating SiN_x , ~ 50 nm of (n^+) a-Si:H, and ~ 100 nm thick Al for the source-drain contacts. Fabrication details are given elsewhere [22]. Fig. 9 is a cross-sectional view of this structure. After fabrication, the SiN_x layer on the back of the substrate was etched away and the transistors were annealed in forming gas. Fig. 10 shows typical transfer characteristics for these devices. The off-current is ~ 3×10^{-12} A, the on-off current ratio > 10^6 , the threshold voltage ~ 3 V, and the subthreshold slope ~ 0.5 V/decade. The electron linear mobility, calculated from the transfer characteristic for drain-to-source voltage $V_{ds} = 0.1$ V, is ~ $0.45 \text{ cm}^2/\text{Vs}$.

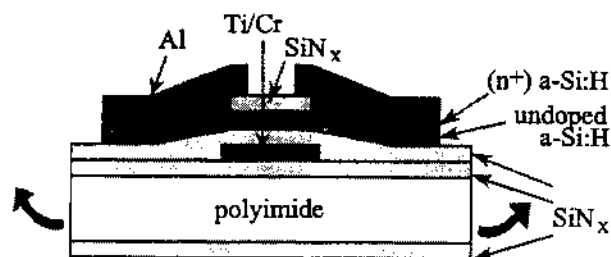


Fig. 9. Cross-section of a-Si:H TFT fabricated on ~ 51 μm thick polyimide foil. The arrows show the parallel bending direction (see text for details).

We strained individual transistors by inward (compression, by definition negative) or outward (tension, positive) cylindrical bending. In most cases the bending direction was parallel to the source-drain current path, as shown by heavy arrows in Fig. 9. A few TFTs were also tested with the bending direction perpendicular to the source-drain current path. In compression, single TFTs were bent to different radii of curvature R , ranging from 70 to 1.6 mm. Transfer characteristics like those of Fig. 10 were measured at each bending radius. Some TFTs were measured at several R , while others were bent permanently to a fixed R , to monitor the change in the transfer characteristics for ~ 40 hours. Several TFTs also were measured in tension by parallel bending.

From each set of transfer characteristics we extracted the off-current I_{off} , on-current I_{on} , gate leakage current I_{leak} , linear mobility μ , threshold voltage V_{th} , and subthreshold slope S . The definition of these currents is as follows: the off-current is the smallest drain-to-source current at $V_{ds} = 10\text{V}$, the on-current is the drain-to-source current for $V_{ds} = 10\text{V}$ and $V_{gs} = V_{th} + 10\text{V}$, and the leakage current is the gate-to-source current for $V_{ds} = 10\text{V}$ and $V_{gs} = 20\text{V}$. V_{th} and μ were calculated from the transfer characteristic for $V_{ds} = 0.1\text{V}$ while S was obtained by fitting an exponential function to the

subthreshold region of the transfer characteristic for $V_{ds} = 10$ V. To obtain reference values for these parameters, each TFT was measured first before any strain was applied. We calculated the strain at the $\text{SiN}_x/\text{a-Si:H}$ interface of the TFTs using Eq. (1) of ref. 21. Young's modulus of our polyimide substrate is 5 GPa and we assumed 183 GPa for all TFT layers [23]. The highest compressive strain, at the smallest bending radius $R = 1.6$ mm, was $\sim -1\%$, the highest tensile strain was 0.2%.

4.3 Electrical performance under strain

First, upon application of compressive strain we observed a slight decrease in the on-current I_{on} , and hence the linear mobility μ . The changes in the off-current I_{off} , leakage current I_{leak} , and the threshold voltage V_{th} remained within experimental error, and we concluded that they did not change. The subthreshold slope S seemed to rise slightly with increasing compressive strain. Next, we applied increasing tensile strain and observed that the linear mobility μ did increase while the subthreshold slope S remained unchanged.

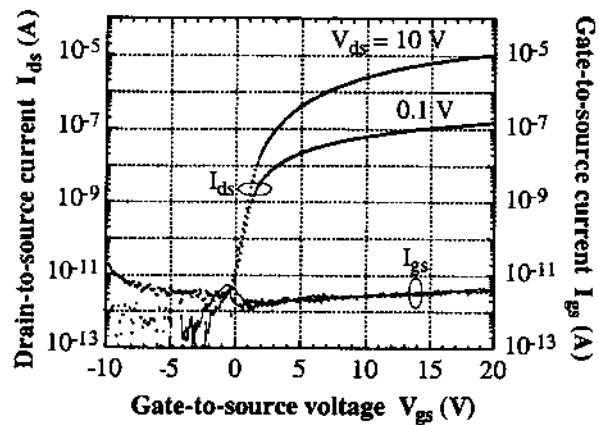


Fig. 10. Transfer characteristics for the TFT of Fig. 9. The source was grounded.

correspond to TFTs with the parallel and perpendicular bending direction, respectively. There is no qualitative difference in the behavior of μ/μ_0 as a function of direction of the strain, but quantitatively the values of μ/μ_0 remain slightly larger in the perpendicular bending direction. A linear fit to all experimentally measured mobilities gives: $\mu/\mu_0 = 1 - \epsilon/4$, when the strain is expressed in percent.

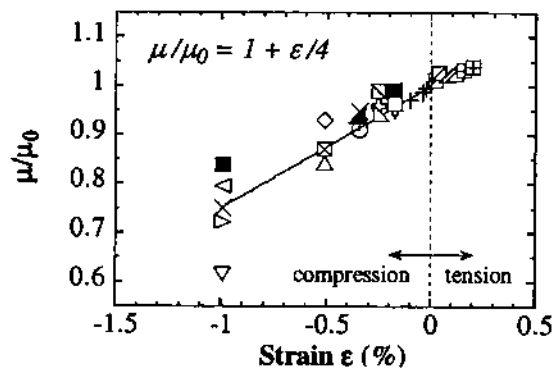


Fig. 11. Relative mobility plotted as a function of strain. Each symbol represents a different TFT. Empty and full symbols correspond to TFTs with the bending direction parallel and perpendicular to the source-drain current path, respectively.

Fig. 12 shows the relative subthreshold slope S/S_0 , where S is the subthreshold slope at a given strain and S_0 is the initial slope. While there is a clear trend in μ/μ_0 as a function of strain ϵ , the spread in S/S_0 is quite large. The solid line in Fig. 12, which is a linear fit to the experimental data, indicates that there is a decrease in S/S_0 with the applied strain, but one should draw this conclusion with some reservation.

For a given strain, the change in the mobility was 'instantaneous' (on the time scale of 5 minutes) and it did not change during the measurement time of ~ 40 hours. Fig. 13

shows the mobility μ/μ_0 , the off-current I_{off}/I_{off0} , and the leakage current I_{leak}/I_{leak0} as functions of time during which -1% compressive strain was applied. As mentioned above, no change in the off-current or leakage current was observed and therefore I_{off}/I_{off0} and I_{leak}/I_{leak0} remain unity.

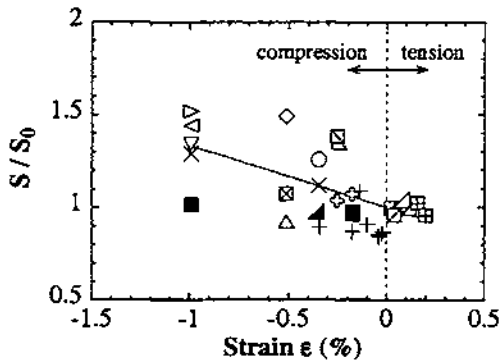


Fig. 12. Relative subthreshold slope plotted as a function of strain. Symbols as in Fig. 11.

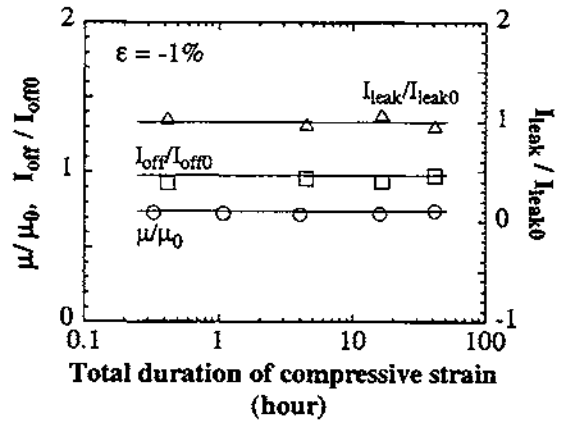


Fig. 13. Relative mobility, off-current, and leakage current as a function of duration of compressive strain of $\sim -1\%$.

4.4 Mechanism of mobility enhancement and reduction

In crystalline silicon the electron and hole mobilities depend on scattering. The most important scattering mechanisms are thermal vibrations of the lattice and ionized impurities. During our bending experiments the amorphous silicon network is squeezed or expanded by no more than 1%, which causes an insignificant change in the scattering length. The measurements are performed at constant temperature. The a-Si:H is of device quality and does not contain phosphorus or boron impurities. However, in amorphous silicon TFTs the free electron mobility, while set by scattering on every silicon atom, is reduced to an effective mobility by frequent trapping in the conduction band tail states. Thus the electron field effect mobility depends on the width of the conduction band tail. For these reasons we considered a change in the slope (width) of the conduction band tail under strain as the cause of mobility change.

In the following discussion, let us consider compressive strain, since the only published data on a-Si:H were measured under hydrostatic compression. We will now trace the link between the width of the conduction band tail of a-Si:H and hydrostatic compression. First, we observed an average decrease in the TFT mobility of only about 25% under the compressive strain of -1%. In a-Si:H the slopes of the conduction and valence band tails are correlated [24] and therefore the electron linear mobility of a-Si:H TFTs depends on the Urbach energy of the a-Si:H channel material [25]. Larger Urbach energy means wider conduction band tail and lower linear mobility in the TFT. If we apply the data of refs. 24 and 25 to our a-Si:H material, a 25% reduction in the linear mobility will be caused by a 1.5-meV increase in the Urbach energy. Next, Cody et al. [26] found that in a-Si:H both the Urbach energy E_0 and the optical gap E_g are controlled by the amount of disorder, structural and thermal, and are correlated as $\Delta E_g \sim -6.2 \times \Delta E_0$. If we assume that strain-induced disorder follows the same dependence, an increase in E_0 of ~ 1.5 meV should be accompanied by ~ 10 -meV reduction in E_g . Lastly, Welber and Brodsky showed experimentally that the optical band gap of a-Si:H decreases with increasing hydrostatic pressure P (absolute value of compressive stress) as $(\partial E_g / \partial P)_T \sim -0.7 \times 10^{-11}$ eV/Pa [27]. Thus a 10-meV reduction in E_g requires a hydrostatic pressure of ~ 1.4 GPa. Taking 60 GPa for the bulk elastic modulus of a-Si:H by hydrostatic compression [28], 1.4 GPa will cause $\sim 2\%$ compression. By thus linking our observed reduction in electron mobility of $\sim 25\%$ to the likely effect of a hydrostatic compression of $\sim 2\%$, we can plausibly explain the mobility reduction in compression as a consequence of increased disorder. Finally, one would intuitively expect that tensile strain will have an opposite effect on the band gap and the valence and conduction

band tails of the a-Si:H channel material and hence the mobility should increase, in agreement with the experimental data of Fig. 11.

A few qualifying comments are in order. In our discussion we neglected piezoresistive changes in the contact resistance of the a-Si:H TFTs. This effect has been observed in microcrystalline silicon [29], but was never studied in a-Si:H. The change in the linear mobility of a-Si:H TFTs and the possible dependence of the a-Si:H band gap on stress imply that a piezoresistive effect does exist. Finally, the channel length of the TFTs does change upon straining but this effect is negligible.

4.5 The 'safe' bending radius of TFT backplanes under cylindrical deformation

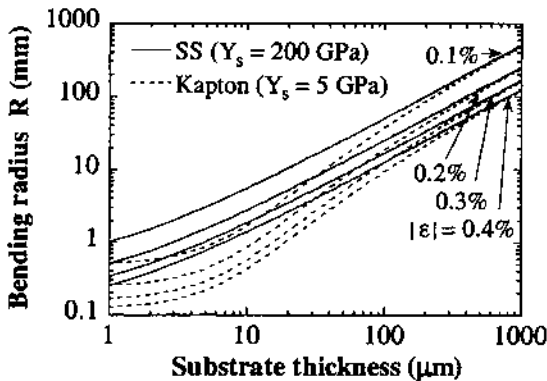


Fig. 14. Bending radius of TFT backplane as a function of substrate thickness for two different substrates (stainless steel and Kapton) and four different values of strain in the TFT circuit.

a function of the substrate thickness for two different substrates (stainless steel ($Y_s = 200$ GPa) and Kapton ($Y_s = 5$ GPa)) and four different values of strain: 0.1%, 0.2%, 0.3%, and 0.4%. We assumed that (i) the substrate is flat before bending, (ii) the TFT circuit is 960 nm thick, and (iii) has Young's modulus of 183 GPa [23].

One can see that regardless of substrate, the thinner the substrate the smaller the bending radius of the backplane, for a given value of strain in the circuit. For substrates thicker than ~ 200 μm the strain in the TFT circuit is almost identical, whether fabricated on a stiff (stainless steel) or on a compliant (plastic) substrate. The advantage of the compliant substrate becomes visible for substrate thickness less than 100 μm . For example, a 10- μm thick plastic wrapping foil substrate and a strain limit of $\pm 0.3\%$ would allow bending to a radius as small as ~ 0.6 mm, while a 10- μm thick steel foil would allow bending to only ~ 2 mm radius. Very small radii of curvature will be made possible by integrating the backplane with the front plane such that the active circuits are placed in the strain-free neutral plane.

4.6 Spherical Deformation of a-Si:H TFTs on plastic substrates

Cylindrical deformation of substrates as described above puts the top and bottom of the substrate foil in opposite strain conditions, with an unstrained neutral plane in between. The strain may be minimized by using a thin substrate. If one desires arbitrary 3-D shapes to be formed from a plane, such as a spherical cap shape, strain is unavoidable, even if thin substrates are used. As a first step towards the achievability of such arbitrary 3-D shapes, polyimide substrates

The 'safe' bending radius of an actual backplane under cylindrical deformation (rolling) will depend on the amount of strain that the backplane circuitry will tolerate. Even though the actual backplane is a multilayer structure that is more complicated than the structure of our TFT and it contains other materials than the ones used in our TFT fabrication, one can use the results from the a-Si:H TFTs as an approximation for the 'safe' bending radius of the TFT backplane. The previously published data suggest that the a-Si:H TFTs are more sensitive to the tension than thin layers of ITO [30]. We assume that the TFT circuit will continue to function at strains between -0.3% and $+0.3\%$ and that the electron mobility will change by less than 10%.

The two main parameters that set the 'safe' bending radius of the backplane are the mechanical properties of the substrate (expressed by Young modulus Y_s) and the thickness of the substrate. Fig. 14 shows the bending radius R as

with finished a-Si:H TFT structures as described above were clamped on a circular boundary and then deformed into a spherical cap shape by applying gas pressure to one side of the clamped substrate, resulting in spherical cap shapes. The shape remained after the pressure was removed because of plastic deformation of the substrate. Geometric arguments make it straightforward to calculate the average radial strain which results from the deformation, which in the limit of thin substrates depends only on the angle subtended (Fig. 15). For example, to subtend an angle of 66 degrees (corresponding to ~ 1 steradian of solid angle), an average tensile strain of 6% results, which will clearly crack the inorganic TFT materials such as silicon or silicon dioxide, making realistic circuits impossible. [31]. Such spherically deformed substrates with active circuitry are not just of academic interest, but are actively desired for their ability to simplify (cost and weight) the optics of focal plane imaging arrays [32].

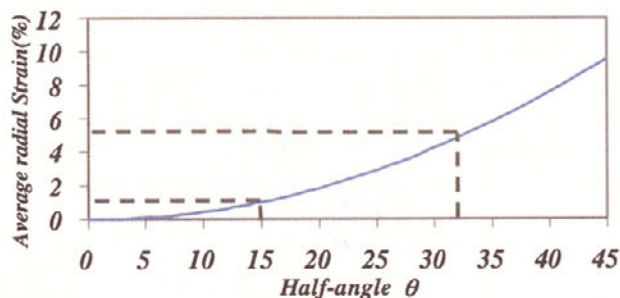


Fig. 15. Average radial strain vs. subtended half-angle (in degrees) for spherical foil clamped on circular edge and deformed into spherical cap shape. 32° corresponds to ~ 1 steradian of solid angle.

The deleterious effect of this large average substrate strain can be avoided, however, by patterning the relatively hard inorganic device materials and silicon nitride passivation into islands [31]. Under deformation, the islands then are relatively rigid, with the substrate deforming under and around them. For proper choice of the island size (under ~ 100 microns in practice), the island strain can be kept under 1%, and cracks in the islands can be avoided (Fig 16). The strain is strong function of the island size, but only a very weak function of the island density because of the large plastic flow which occurs between the islands in the substrate.

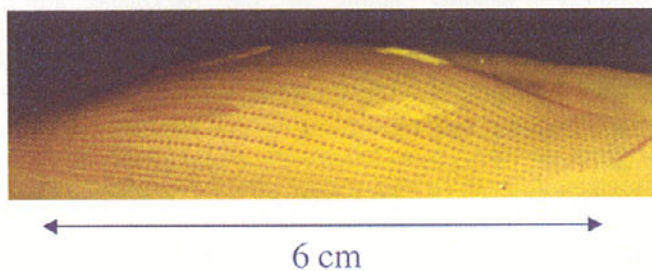


Fig. 16. Deformed polyimide substrate with a-Si:H/silicon nitride device islands deformed to 66 degree field of view.

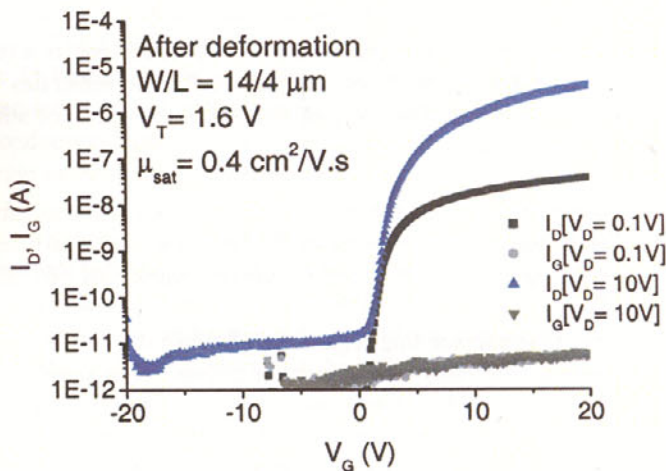


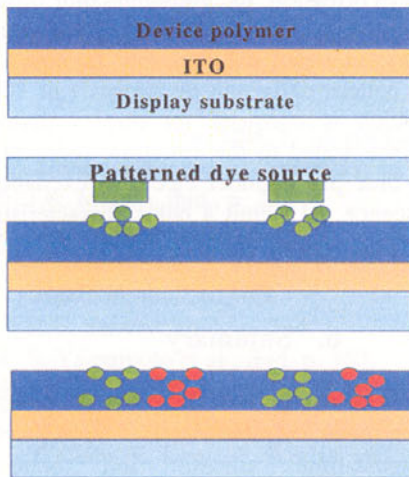
Fig. 17. Well-behaved IV curve of a-Si:H TFT on spherical dome subtending one steradian.

a-Si:H transistors fabricated on such islands which do not crack under deformation exhibit qualitatively well behaved characteristics (Fig. 17) [33], with only minimal changes in threshold voltage and mobility. Ongoing work is relating the change in the transistor characteristics from the biaxial strain which results here to the uniaxial strain of the previous section. The large deformation which results between the island (from the low strain in the islands themselves)

makes it difficult for interconnects between islands to survive the deformation. However, it is possible to deposit interconnect metal on the spherical surface after the deformation, and pattern it using conventional lithography on flat surfaces done before the deformation [34]. With this combination, simple a-Si:H circuits on foils which subtend up to one steradian of solid angle have been achieved [35].

5. Dry-Printing Technologies for Full Color Organic LED Integration

In addition to their attractiveness since they can be deposited on various surfaces at low temperature, organic semiconductors are of great interest for display and other large area technologies because they are amenable to patterning by various printing technologies. In that way, the conventional steps of blanket deposition, photolithography and etching can be avoided.



Step 1: Uniform spin-coat of device polymer with blue-emitting dye

Step 2: Dye Contact Printing: transfer of green dye from pre-patterned dye source to device polymer surface (~70 °C)

Step 3: Repeat printing with patterned red dye

Step 4: Diffusion of dyes vertically throughout the polymer film

In this section, we demonstrate a dry-printing approach for patterning organic polymer semiconductors not for TFTs, but rather for organic LEDs (OLEDs). By sandwiching one or more layers of organic thin films (on the order of 100 nm thick) between an anode and cathode layer with appropriate work function, LEDs can be fabricated on plastic or glass substrates with colors across the visible spectrum. One outstanding challenge for OLEDs is an approach for patterning these materials for full color displays – for pixels which separately emit red, green, or blue light, it is desired that the organic materials be patterned in some way. This is a difficult problem since the conventional means for depositing these materials (spin coating for organic molecules and thermal evaporation for small organic molecules) gives a blanket film, and these organic materials are generally not amenable to conventional photoresist and etch processing as is typically used to pattern inorganic thin films.

Fig. 18. Dye printing process for locally tuning color of organic LEDs. There are two printing steps (green and red) followed by a single diffusion.

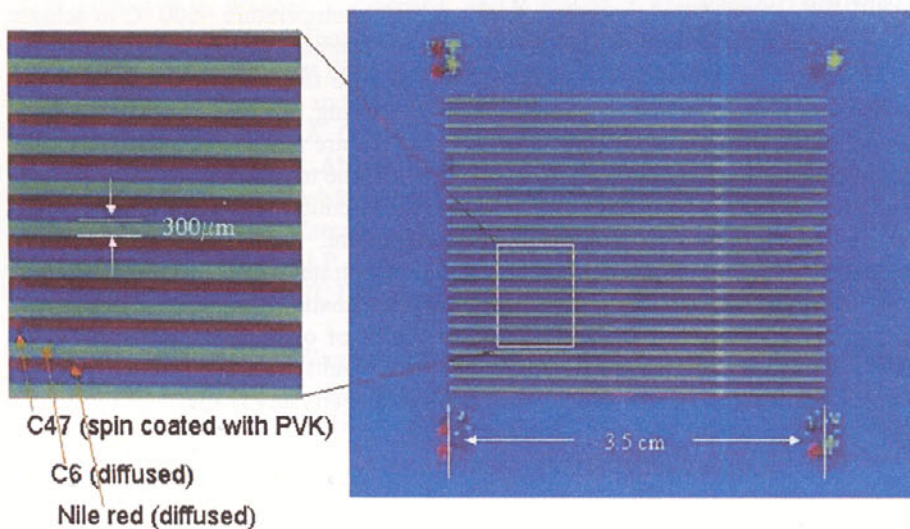


Fig. 19. Photoluminescence image (UV excitation) of a PVK film, uniformly doped with C47 blue dye by spin coating, to which stripes of C6 and Nile red have been added by the printing process of the previous figure [39].

Last year at this meeting, we reviewed work on the

deposition of organic semiconductors and dyes by ink jet printing [36]. However, the practical use of ink jet printing is difficult because of the lateral polymer/dye redistribution which occurs during the droplet drying. Therefore we have developed an alternative all-dry printing process. The emission color of organic LEDs can be tuned by the addition of small (e.g. 1%) levels of dye organic molecules, which capture carriers and/or excitons from the organic semiconductor host. In our work, a 100 nm layer of poly(9-vinylcarbazole) (PVK) is first spin-coated on a substrate with patterned transparent indium tin oxide (ITO) lines, which form the device anode. A blue dye is added to the PVK solution before spin coating, so that after coating the film emits a deep blue light. Printing plates are then made by patterning a dye source, consisting of a green dye (C6) or red dye (Nile Red) in a soft polymer host [37]. The printing plate is brought into contact with the PVK film, and heated to 70 °C. At this elevated temperature, the dye diffuses out of the patterned printing plate polymer to make a pattern on the surface of the PVK, but does not diffuse into the PVK because of its low diffusion coefficient in PVK at this temperature. The dye is then induced to diffuse down through the PVK at room temperature by a brief exposure to a solvent vapor, which increases the diffusion coefficient of the dye in the polymer by over a factor of 10^{10} for several minutes [38].

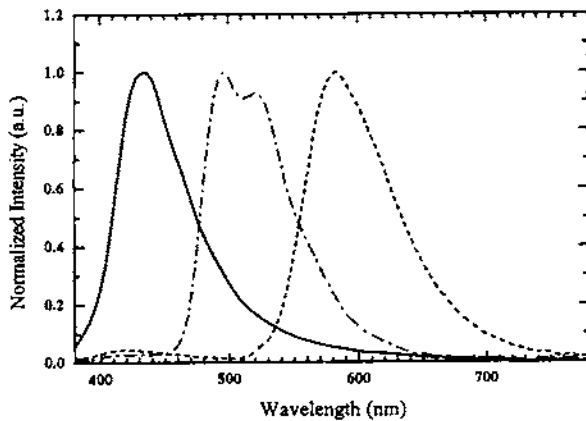


Fig. 20. EL emission in R, G, and B pixels using a device polymer of PVK doped uniformly with C47 (blue, peak at ~430 nm), with patterned Nile Red (~580 nm), patterned C6 (~500 nm), and no added patterned dopant, respectively. [26]

used to fabricate these devices on plastic. All of these technologies are capable of bending, with the most sophisticated structures and analysis having been applied to amorphous silicon. The TFT curves are qualitatively unaffected by strain, and quantitatively the compression produced a small decrease in mobility, while the tension caused an increase in the on-current and hence the linear mobility. We conclude that both the valence and conduction band tails of a-Si:H channel material are affected by strain, and therefore the TFT mobility is strain-dependent. A-Si:H TFTs on plastic can also be deformed into spherical cap shapes, which require a very large average substrate strain, by using patterned device islands. Finally, organic semiconductors are attractive because of their amenability to direct printing and patterning methods. An all-dry printing method was demonstrated to tune the color of organic LEDs, so that RGB light-emitting pixels could be integrated on a common substrate. Altogether, the results point toward the eventual possibility of printing transistors anywhere at low temperatures and bending them into nearly any shape.

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After the dye diffusion, the emission color of the host film is changed, as is shown by the red and green stripes added to the small display plate in Fig. 19. Note the sharp pattern definition on the scale of 10's of microns, which is adequate for display pixels. After cathodes are added to the structure, individual red, green and blue pixels under electrical excitation (electroluminescence, EL) emit a color characteristic of the lowest energy dye in the local region (Fig. 20) [39, 40].

6. Summary

Three different TFT technologies for plastic substrates have been demonstrated: amorphous silicon, polycrystalline silicon, and organic semiconductors. The organic and amorphous silicon technologies have a maximum process temperature of ~150 °C, they can be directly integrated onto most plastic substrates. On the other hand, the polysilicon technology requires a temperature ~500 °C to achieve device performance comparable to that of bulk silicon CMOS technologies, so that a transfer approach was

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* Contact information: sturm@ee.princeton.edu, 609-258-5610