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SCHOTTKY BARRIER HEIGHTS OF Pt SILICIDES ON SiGe

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Abstract

Silicide/SiGe Schottky barriers are of importance for applications in infrared detectors and SiGe contacts, as well as for fundamental studies of metal-semiconductor interfaces. We have fabricated silicide/SiGe Schottky diodes by the reaction of evaporated Pt and Ir films on p-SiGe alloys with a thin Si capping layer. The onset of metal-SiGe reactions was controlled by the deposited metal thickness. The Schottky barrier heights were determined from internal photoemission. Pt-SiGe and Ir-SiGe reacted diodes have barrier heights that are higher than the corresponding silicide/p-Si diodes. PtSi/Si/SiGe diodes, on the other hand, have lower "barrier heights" that decrease with increasing Ge concentration. The smaller barrier heights in such silicide/Si/SiGe diodes are due to tunneling through the unconsumed Si layer. Equations are derived accounting for this tunneling contribution, and lead to an extracted "barrier height" that is the Si barrier height reduced by the Si/SiGe band offset. Highly bias-tunable barrier heights are obtained (e.g. 0.30 eV to 0.12 eV) by allowing the SiGe/Si band offset to extend higher in energy than the Schottky barrier, leading to a cut-off-wavelength-tunable silicide/SiGe/Si Schottky diode infrared detector.

Introduction

Silicide/$Si_{1-x}Ge_x$ diodes may have a lower barrier height than the corresponding silicide/Si diode because of the smaller bandgap of SiGe. This is the motivation for their possible use in extended range silicide infrared detectors[1]. The formation of abrupt, near-ideal silicide/SiGe interfaces, however, is not as simple as the formation of comparable silicide/Si interfaces, because of the more complex chemistry of metal-SiGe reactions. There is at present significant variation in the reported barrier heights of diodes formed by the reaction of metals into SiGe. Kanaya et al.[2] have reported barrier heights (from forward I-V) for Pt and Pd reacted into p-SiGe (of various Ge concentrations) that were lower than the corresponding silicide/Si barrier heights. However, Liou et al.[3] report that the barrier heights (from forward I-V) of Pt and Pd reacted into n-$Si_{0.80}Ge_{0.20}$ were both ~0.68 eV, while Xiao et al.[4] report a barrier height (from photoresponse) for Pd reacted into p-$Si_{0.80}Ge_{0.20}$ of ~0.7 eV, substantially higher than the Pd silicide/Si SBH. This situation calls for better reporting of differing preparation procedures and supplemental information on metal-SiGe reaction products. An approach that bypasses the problems of metal-SiGe reactions, however, is to grow a thin Si capping layer on the SiGe, with which a metal film of suitable thickness would react. Using this method, Xiao et al. have formed Pd and Pt silicides on Si/SiGe with lowered barrier heights.[4] Codeposition of metal and Si in stoichiometric ratio would be another method of avoiding complex metal-SiGe reactions.

In this paper, we report our results on the barrier heights of Schottky diodes formed by the reaction of Pt and Ir layers with a Si cap on SiGe. Diodes were also formed with metal-SiGe reactions by depositing more than enough metal to completely consume the Si cap.

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tal Details

p-type (boron-doped) SiGe structures were grown by rapid-thermal chemical vapor
(RTCVD), in a system that has been described previously.[5] The SiGe layers were
Si, and a layer of graded Ge concentration was grown between the SiGe and the Si.
Ir depositions were done by electron beam evaporation in a load-locked ultra-high
tem. The wafers were RCA-cleaned, which slightly reduces the Si cap thickness and
ted for in selecting the metal layer thickness. Before deposition, the Si surface was
rminated by dipping in aqueous HF solution. The wafers were held at elevated
es during deposition and the silicides were formed by annealing in-situ for one hour.
ere formed at 350 C while Ir diodes were formed at 550 C. For control, silicide/Si
processed and deposited at the same time on boron doped Si substrates (10-15 ohm-
samples were processed with guard ring structures in the Si below the SiGe.
photoresponse measurements were made with a Perkin-Elmer single-pass
ator and a SiC globar at 1000 C as the infrared source. The input radiation was
139 Hz and the photoresponse measured by lock-in amplifier. Measurements were
emperature of 40 K or lower, and at various reverse bias voltages.

tal Results

en the deposited Pt layer is thick enough to react with all the Si cap and some of the
nd that the barrier height is raised, not lowered. We call such diodes Pt-SiGe reacted
SiGe and Ir-SiGe reacted diodes had barrier heights of ~0.27 eV and ~0.31 eV,
, higher than typical values of 0.22 and 0.12 eV for the corresponding silicide/p-Si
eir emission constants are also lower and more voltage dependent than silicide/Si
barrier heights are expected to vary widely depending on the detailed results of the
t-SiGe reactions, for example, have been reported[3,6] to result in Ge segregation and
PtSi formation.

en the deposited Pt layer is not thick
consume the whole Si cap, the
ts extrapolate to a lower barrier
ause some unconsumed Si remains,
e is that of PtSi/Si, and the lower
arrier height is due to tunneling
otential energy barrier formed by the
is reason we refer to such diodes as
e diodes. Figure 1 shows Fowler
tSi/Si/SiGe diodes of varying Ge
ons. The extrapolated barrier heights
vith increasing Ge concentration.
arly extrapolated, or "effective",
ghts, do not really correspond to an
ier height, but rather, are due to an
the yield because of the tunneling
e unconsumed Si layer. In the next
equations for internal photoemission
ed to take this into account.

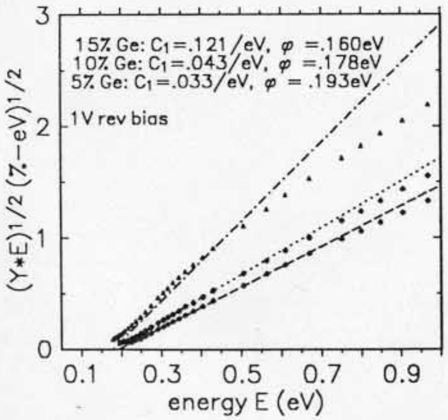

Figure 1: Fowler plots at 1V reverse bias, of PtSi/Si/SiGe diodes of varying Ge content.

Reverse I-V characteristics for the PtSi/Si/SiGe samples show leakage currents that are low for Schottky diodes on epitaxial Si, typically about 10^{-10} A/cm^2 at 1 volt reverse bias. Because the samples have no guard rings, these increase rapidly to about 10^{-2} A/cm^2 at about 10 volts bias. Control diodes made on substrate Si, however, could be biased much higher without breakdown. This may be due to the higher quality of the Si substrates or the higher doping of the epilayers, or a combination of both.

Internal photoemission with a tunneling barrier

Figure 2 is the valence band-edge depth profile of a silicide/Si/SiGe/Si diode, showing the thin potential barrier formed by the unconsumed Si. We briefly outline the derivation of equations for photoresponse in the presence of such a tunneling barrier. The internal quantum efficiency is the probability that a photoexcited carrier will be emitted over the Schottky barrier. The Cohen-Fowler equation for the internal quantum efficiency, $Y=C_1(h\upsilon-\phi)^2/h\upsilon$, is obtained from[7] $Y=V_c/V_s$, where V_s is the k-space volume of states into which carriers can be photoexcited from the Fermi sphere (a shell of width hν above the sphere) and V_c is the k-space volume of states in V_s that satisfy the conditions for emission. In order to model the effects of a tunneling barrier, we therefore divide V_c into two regions, one for perpendicular energies above the Si barrier, and the other for perpendicular energies corresponding to tunneling through Si barrier. We then reduce the volume of this second region by an average tunneling probability τ_{ave}. We get

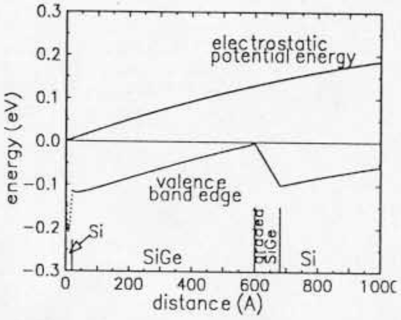

Figure 2: Calculated valence band-edge profile of a PtSi/Si/SiGe/Si diode, showing both Si/SiGe interfaces.

$$Y = C_1(1-\tau_{ave})\frac{(h\nu-\phi_s)^2}{h\nu} + C_1\tau_{ave}\frac{(h\nu-\phi_{sg})^2}{h\nu} \qquad h\nu > \phi_s \qquad (1)$$

$$Y = C_1\tau_{ave}\frac{(h\nu-\phi_{sg})^2}{h\nu} \qquad \phi_s > h\nu > \phi_{sg} \qquad (2)$$

where ϕ_s is the SBH with Si and $\phi_{sg} = \phi_s - \Delta E_v$ where ΔE_v is the valence band offset. Equation (2) holds for photon energies such that *all* the emitted carriers tunnel through the Si barrier, and is of the same form as the modified Fowler equation, with the coefficient reduced by a factor of τ_{ave}. Equations (1) and (2) result in a Fowler plot with a segment of reduced slope below ϕ_s, as shown in Figure 3. Only the slope of this low energy segment, and not its intercept, depends on the value of τ_{ave}. This value can be obtained from the data by first obtaining $C_1\tau_{ave}$ from the slope of the low energy segment, then subtracting the extrapolation of this segment from the high energy part. The slope of the reduced higher energy segment gives $C_1(1-\tau_{ave})$, which is combined with $C_1\tau_{ave}$ to give both C_1 and τ_{ave}. An estimate of the Si barrier thickness d can be obtained from τ_{ave}. If one approximates τ_{ave} by the expression for tunneling through a rectangular barrier of height ϕ_s, $\tau_{ave} = \exp[-2d(2m(E_{ave}-\phi_s))^{1/2}/\hbar]$, then the model predicts essentially a Si-like

rier for Si thicknesses of greater than 40 Å. The fitted values of τ_{ave}, C_1, ϕ_s, and
in Figure 3. For an E_{ave} halfway between ϕ_s and ϕ_{sg}, these values of τ_{ave} correspond
ted Si barrier thickness of ~9-10
consistent with the deposited film
(Pt and Si), within their error
low energy segment extrapolates
eV, which is reasonably consistent
ce band offset of about 0.09 eV
ained SiGe. Incorporating the
ndence of τ would only result in
ure of the low-energy segment,
discernible in the data. More
deling is therefore not warranted.

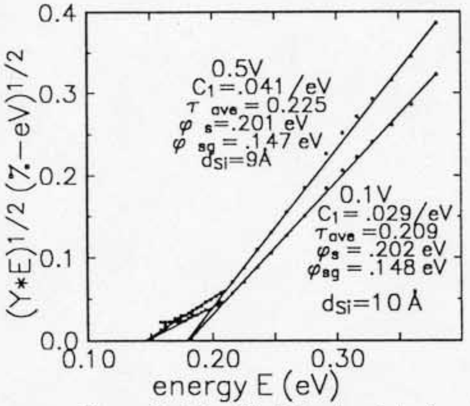

Figure 3: Magnified Fowler plot of a PtSi/Si/SiGe (13% Ge) diode.

rrier-height PtSi/SiGe/Si diodes

icide/SiGe/Si Schottky diodes, the
trate band offset may act as an
arrier to photoemitted carriers,
n the SiGe thickness and grading.
layers are thin enough to lie
ne depletion region, the valence band-edge energy profile is calculated with little
of the standard theory[8]. The electrostatic potential energy due to the space charge
$z,W)=q^2N_a(W(V_{bi})z-z^2/2)/\varepsilon_s$, where the depletion width $W(V_{bi})$ depends on the built
lifference $qV_{bi}=q\phi_b-(E_v-E_F)$. For standard diodes, the valence band-edge energy is
$+q\phi_b$. For silicide/Si/SiGe/Si and silicide/SiGe/Si diodes, however, we have
$+E_v^{(i)}(z)$, where $E_v^{(i)}(z)$ is the initial (non-equilibrium, flat-band) valence band profile
onductor structure, i.e., before any charge redistribution. For a silicide/SiGe/Si
de, the built in potential is given instead by $qV_{bi}=q\phi_{bsg}+\Delta E_v-(E_v-E_F)$, where $q\phi_{bsg}$
e/SiGe barrier height and ΔE_v is the SiGe/Si band offset.

e calculated band-edge profile of Figure 2, the thickness and position of the graded
ch that the "peak" at the SiGe/Si-substrate interface at zero bias does not extend
ϕ_{sg} = ϕ_s-ΔE_v , so that the barrier height measured by photoresponse measurements
hose determined by the silicide/Si/SiGe interface. The SiGe/Si-substrate offset,
n be designed to be extend higher in energy than the Schottky barrier, and then
with reverse bias, forming a tunable barrier height Schottky diode detector. Figure
such a silicide/SiGe/Si tunable-barrier-height detector. The effective barrier height
ucture is much more sensitive to reverse bias than normal Schottky diodes because
peak is much further into the semiconductor. For emission over the SiGe/Si peak
low bias, the quantum efficiency (determined by the emission coefficent C_1) would
h reduced because of scattering in the thicker semiconductor region before the peak
However, the C_1 coefficient should revert to its normal value at higher biases
ng to emission over the Schottky barrier. Because uniformity, and not quantum
is the competitive advantage of silicide infrared detectors, applications may be

possible in spite of the reduced quantum efficiency at low bias.

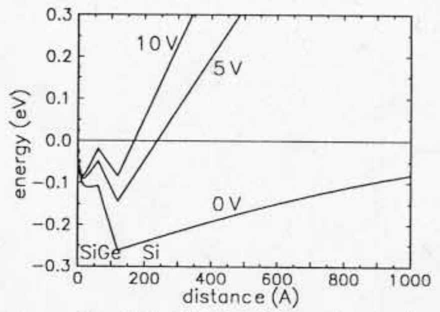

Figure 4: Calculated valence band-edge profile of a tunable silicide/SiGe/Si infrared detector at various bias voltages.

Figure 5 is a plot of the barrier heights of a series of PtSi/Si/SiGe/Si samples, measured by internal photoemission, as a function of reverse bias. The dotted curve is the theoretical reverse bias lowering for a typical PtSi/Si diode. The bias dependence of the barrier heights of the 0% and 10% Ge samples closely follow this curve. For the 15% and 20% samples, however, the barrier heights rapidly decrease with reverse bias, as expected for emission over the SiGe/Si interface. The barrier heights then level off to their normal bias dependence, which is expected at biases such that the SiGe/Si offset is pulled down below the Schottky barrier. The bias-sensitivity of the barrier height in such diode structures is determined by the thickness of the SiGe layer. If we denote the voltage-induced change in the effective barrier height by $\Delta\phi_{eff}(V,z_2)$, where z_2 is the distance from the metal-semiconductor interface to the SiGe/Si interface, then $\Delta\phi_{eff}(V,z_2)=qN_az_2(W(V)-W(V=0))/\varepsilon_s$, until the voltage where normal reverse-bias lowering of the Schottky barrier takes over.

Figure 6 shows the emission coefficents C_1 for the same samples, plotted to linearize the typical Schottky dependence[9] $C_1 \propto \exp(-z_m(V)/L)$, where $z_m(V)$ is the bias-dependent position of the Schottky barrier maximum for 10^{16} cm^{-3} doping, and L is a scattering length in the semiconductor between the metal-semiconductor interface and the Schottky barrier maximum. The 0% and 10% samples have a linear dependence typical of Schottky emission, with slopes

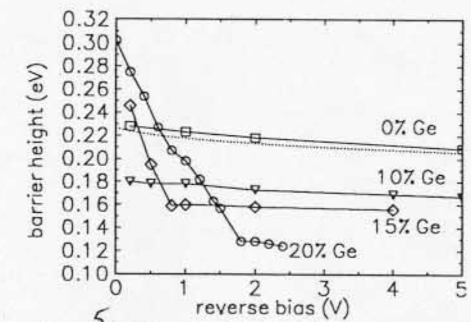

Figure ~~6~~5: Schottky barrier heights at various bias voltages of a series of PtSi/Si/SiGe diodes of varying Ge content.

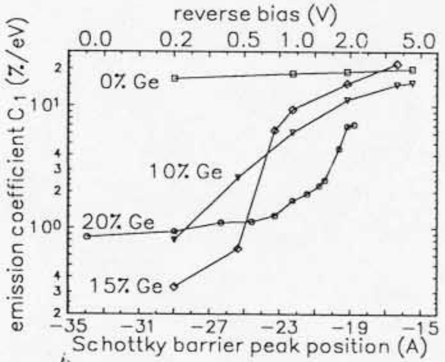

Figure ~~5~~6: Emission coefficients C_1 at various bias voltages of a series of PtSi/Si/SiGe/Si diodes of varying Ge concentration.

rresponding to L = 90 Å and L = 5 Å, respectively. The difference in scattering lengths may due to a combination of alloy scattering and defect scattering in the epitaxial material. The % and 20% samples, however, have nonlinear relationships with low values corresponding to highly bias-variable barrier heights (for emission over the SiGe/Si interface), then a rapid rise higher values corresponding to emission over the Schottky barrier.

nclusions

PtSi/Si/SiGe diodes have effective Schottky barrier heights lower than PtSi/Si. The ective barrier heights decrease with increasing Ge concentration. The lowered barrier height tained from the Fowler plot by standard linear extrapolation does not correspond to an actual rrier height, but is the result of the tunneling through the potential energy barrier formed by unconsumed Si. This tunneling can account for the observed change in the slope of the wler plot at energies below the PtSi barrier height. The barrier height obtained from this low-ergy segment corresponds to the PtSi barrier height reduced by the Si/SiGe band offset. If the Ge layer is thin enough, depending on Ge concentration, the SiGe/Si band offset can extend gher in energy than the Schottky barrier height. Because the potential energy peak formed by s SiGe/Si offset is deeper into the semiconductor than the Schottky barrier, it is more bias pendent, resulting in a Schottky diode with a highly bias-tunable effective barrier height.

knowledgements

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EFFECTS OF RAPID THERMAL ANNEALING ON W/ $Si_{1-x}Ge_x$ CONTACTS.

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ABSTRACT

Thermal reaction of W with $Si_{1-x}Ge_x$ films epitaxially grown by Rapid Therm Chemical Vapor Deposition was investigated in the temperature range 500°C - 1000°C. T samples were annealed either in a Rapid Thermal Annealing (RTA) system or in a convention furnace, both in flowing nitrogen. The reaction products were investigated by Rutherfo Backscattering Spectroscopy (RBS), Energy Dispersive Spectrometry (EDS) and X-r diffraction (XRD). Sheet resistance measurements were also performed to follow the progress the reaction. The reaction of W with $Si_{0.67}Ge_{0.33}$ is similar to that of W with silicon. W reac with silicon to form tetragonal WSi_2. The Ge-content in the silicide is lower than that of the a deposited alloy. It is shown that an oxygen contamination occurs during conventional anneali and leads to the formation of non homogeneous Si_{1-x} Ge_x unreacted alloy below the silicide fil Rapid thermal annealing prevents this parasitic effect and the unreacted film remai homogeneous although a slight decrease in the Ge-content is observed. These results a correlated with Schottky barrier height measurements on p-$Si_{0.83}Ge_{0.17}$ partially strained film We observed an increase of the barrier height with increasing the temperature for annealing fro 500°C to 1000°C. This trend may be explained either by strain relaxation or (and) Ge-conte decrease in the unreacted alloy.

I-INTRODUCTION.

$Si_{1-x}Ge_x$ /Si system is expected to play a major role in Si-based devices and has bee extensively investigated. [1] Astonishingly, little attention has been paid to metal/SiGe contac although the knowledge of metallizations to alloy is required for device applications. Recentl the thermal reactions between transition metals[2], Pd [3-6] and Pt [4-7] have been examined and a fe studies on the electrical properties [3-5] of metal/ $Si_{1-x}Ge_x$ contact have been reported. Refractor metals such as tungsten have several characteristics that make them very attractive candidates fo contact metallizations in VLSI circuits. The electrical properties and the thermal stability o W/ $Si_{1-x}Ge_x$ are consequently of great importance. In a previous work [8], we have reported th electrical properties of W/ p-$Si_{1-x}Ge_x$ Schottky diodes. We clearly evidenced that the compositio and the strain dependence of the Schottky barrier height on p-type follows the same trend than th band gap. The results were explained in terms of a pinning effect of the Fermi level relative to th

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