LIMITED REACTION PROCESSING

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ABSTRACT

Limited reaction processing (LRP), a new technique which provi precise control of thermally driven surface reactions, was used to g multilayer structures composed of semiconductors and insulators. Resu are presented for group IV-based materials including epitaxial Si, S alloys, SiO_2, and polysilicon. III-V materials such as GaAs, AlGa and InGaAs have also been successfully grown. A number of diagnos techniques were used to define the advantages and capabilities of L including TEM, SIMS and AES. In addition, some preliminary device resu are presented.

INTRODUCTION

The fabrication of thin, high quality layers of semiconductor insulator films is critical to the future of semiconductor processi It is also of potentially great importance to be able to fabricate seve films sequentially without removing the substrate from the process chamber. This latter feature is important to minimize chemical particulate contamination. Regarding the layers themselves, we want maintain interfaces between layers that are as abrupt as possible, wh generally argues for a minimum high-temperature exposure; and we w good intra-layer material quality and low defect interfaces, which arg for high temperature processing in many cases. The Limited React Processing (LRP) technique was developed in an attempt to meet th objectives [1-4].

The Basic Process

It is convenient to think of the Limited Reaction Process as technique that uses temperature rather than gas flow as a reaction swit Conceptually, what we have is a CVD reactor of small volume that is dri by a source of high intensity, incoherent radiation that can be switc on and off quickly. The wafer being processed rests on three quartz p and represents most of the thermal mass in the system, similar to conventional RTA apparatus. Details of the chamber and related equipm are given in Ref. [1]. In a typical process sequence we first purge chamber, then establish a carrier flow of inert gas and appropriate fl of reactive gases with the substrate at low temperature (unilluminate We then raise the wafer temperature quickly (>300°C/sec) to the desi processing temperature, normally in the range of 1000°C, leave it th for the time required to achieve the desired layer growth, and then swi the light source off again. After the wafer has cooled, we switch the reactive gases and purge the chamber again to set up the next cyc

The potential of such a system for semiconductor processing can be judged in terms of the quality of the layers that can be grown; the abruptness of the doping gradient between layers; and the interface characteristics that are achieved in a multilayer growth. In what follows we will use these broad criteria to examine results obtained in the growth of both column IV and III-V semiconductor compounds.

Epitaxial Silicon

We report first on our attempts to grow single crystal, epitaxial silicon on a silicon substrate. The substrates used for these experiments were (100) Si. Typically the wafers are chemically cleaned using an RCA process and then baked in H_2 (250 Torr) at 1150-1200°C for 20-60 sec directly before deposition.

The system was operated at a pressure of 1-10 Torr to reduce vertical autodoping, improve thickness uniformity, and allow single crystal deposition at relatively low substrate temperatures. Typical deposition temperatures were 850-1000°C for growth rates from .05-0.2 μ/min. Source gases were SiH_2 or $SiHCl_2$, and AsH_3 and B_2H_6 were used for doping.

Abruptness in the doping concentration was measured by growing an undoped film on an n+ (heavily antimony doped) silicon substrate. Secondary ion mass spectroscopy profiles are shown in Fig. 1 for samples grown by both MBE and LRP processes. In both cases the antimony concentration changes by two orders of magnitude (10^{16}-$10^{18}/cm^3$) over a distance of

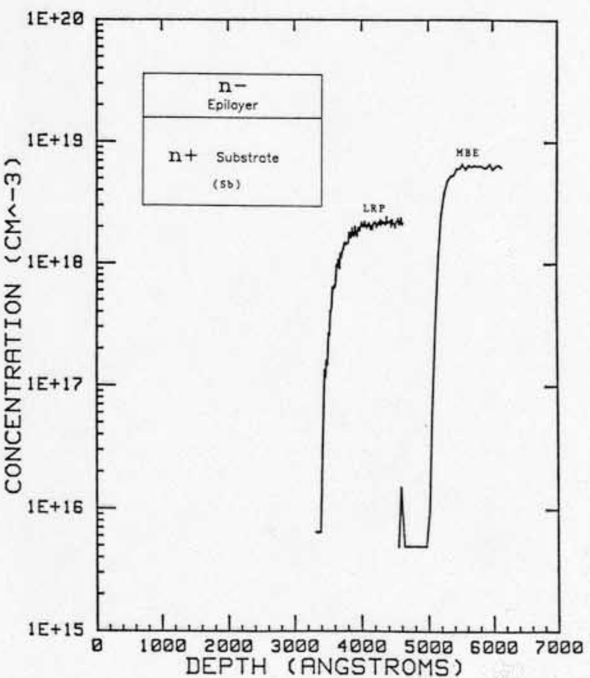


Figure 1. SIMS plots of Sb concentration vs depth for undoped epilayers deposited on an n+ substrate.

less than 30 nm. Hence the LRP process appears to provide an in doping concentration that is comparable to MBE, to within the of SIMS.

The LRP epitaxial films were specular and indistinguish polished substrates when viewed under a Nomarski contrast m Further electronic properties of these films will be described u headings.

Multilayer Growth

A more rigorous test of such a system can be obtained by to grow multi-layer structures consisting of alternating undoped a doped regions. Such structures were deposited in-situ by cha gas composition between high temperature cycles. For these ex silicon was grown from a silane precursor at a pressure of 4. a hydrogen carrier flowing at 3 litres per minute. To introduc the hydrogen carrier was switched off and 5.2 ppm of B_2H_6 in H_2

A SIMS profile of a sample with two p+ regions is shown i The p+ pulses with a full width at half maximum of 10 nm can be re grown [3]. The boron concentration can be observed to change f of magnitude over a distance of less than 40 nm (10 nm/decade).

Figure 3 shows a plot of the measured transition slope vs energy for the sample shown in Fig. 2 and one grown at 1000°C.

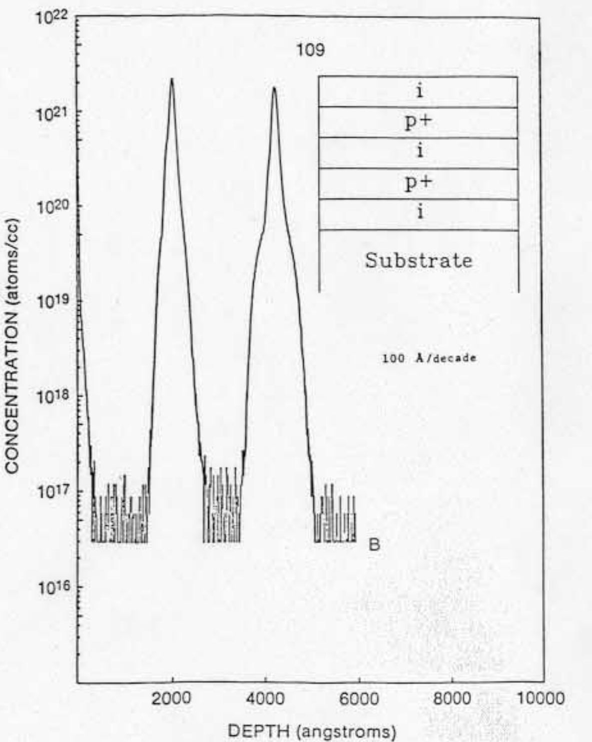


Figure 2. SIMS plot of B concentration vs depth for the LRP p+ structures shown in the inset.

cases the trailing edge is less abrupt because of knock-on by the SIMS oxygen sputtering beam. The lines can be extrapolated back to zero beam energy in order to eliminate the interface smearing caused by the SIMS technique, and thus provide a better estimate of the true transition slope of the doping profile [5]. Note that the trailing edge of the 1000°C sample does not intersect the leading edge at the ordinate, presumably because the trailing edge received a greater thermal exposure as this multilayer test sample was grown.

For electrical measurements, p+ layers having a thickness of .1-.5μ were deposited on n+ substrates. Van der Pauw measurements showed a sheet resistivity of 58 ohms/square and a hole mobility of 42 cm^2/V-sec. This value of mobility is comparable to that of bulk material with the same hole concentration.

By comparing the chemical concentration of dopant determined by SIMS with the hole concentration determined by spreading resistance, the degree of boron activation can be estimated. However, since the SIMS data are considered to be accurate only to about a factor of 2, the level of activation is difficult to determine with precision. The highest hole concentration measured was in the range of $2x10^{20}/cm^3$, whereas SIMS indicated significantly higher boron concentrations. Inactive boron is almost certainly present, the nature of which is currently being investigated.

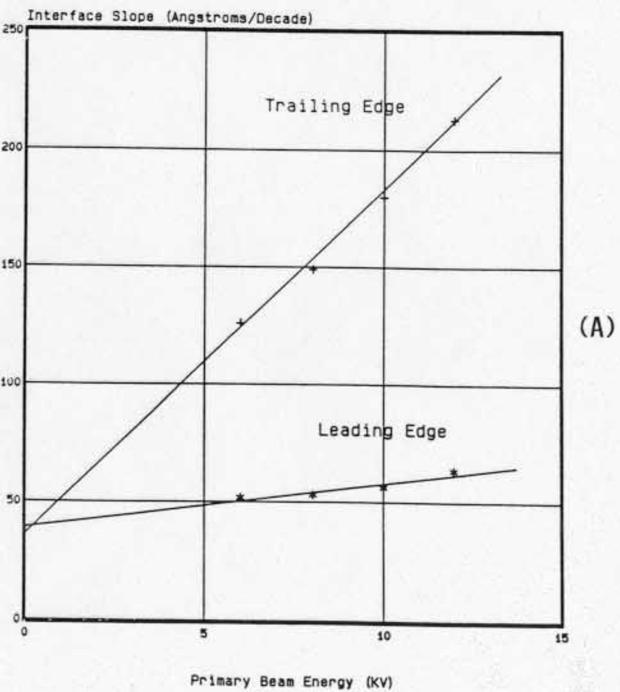
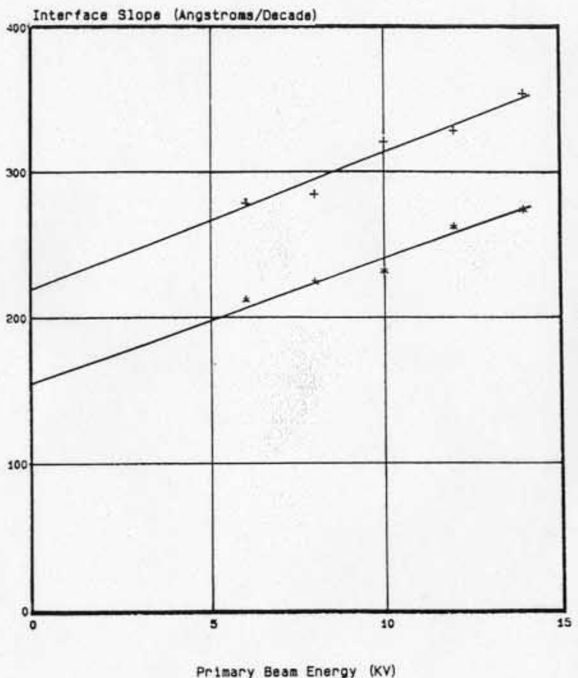


Figure 3. Plots of SIMS B transition slopes vs O_2+ primary beam energy.
(a) LRP i/p+/i sample deposited at 900°C.

(b) LRP i/p+/i sample deposited at 1000°C



Si_xGe_{1-x}/Si superlattices have also been grown using the Reaction Processing technique in which as before each layer multi-layer structure was fabricated in-situ by changing the gas com between high temperature cycles. Commensurate SiGe alloy layers as 15 nm were reproducibly deposited by this technique. Further on such heterostructures are given in the paper by Gronet et

Thermal and Mass Flow Uniformity

Figure 4 is a thickness map of a thin thermal oxide grown on Si wafer in the LRP chamber. This map can be used as a measure of uniformity since the thermal oxidation of silicon is limited by a reaction and not mass flow. Using a 6-inch diameter Si ring place the 4-inch wafer to reduce edge effects, we can achieve an oxide t uniformity of ±3% on the central 3.0-inch diameter portion of th

To determine mass flow uniformity, we performed sheet res measurements on a p-type epilayer deposited on an n-type substrate. 5 is a map of sheet resistivity on a 4-inch wafer in which the ma was aligned upstream in the LRP reactor. The increase in res downstream is caused by both diborane and dichlorosilane depletio measurements indicate that the film near the flat is 1.5 times and has a born concentration 4 times higher than the epilayer on t side of the wafer. We intend to improve this uniformity by in the flow velocity and tilting the water.

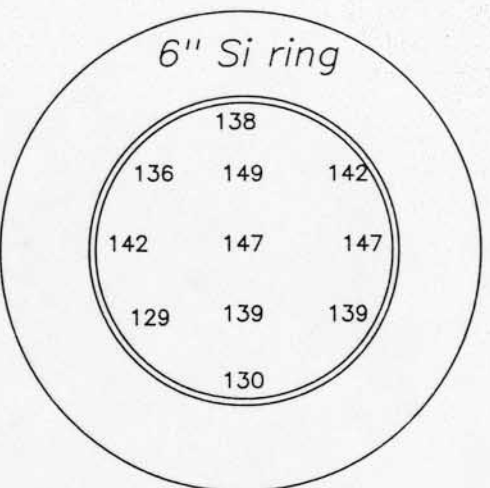


Figure 4. Thermal oxide thickness map of a 4" Si LRP wafer. A 6" diameter Si ring is placed around the wafer to improve temperature uniformity. The oxide was grown at ~1200°C, 500 Torr in dry oxygen. The perimeter values were taken <4mm from the wafer edge.

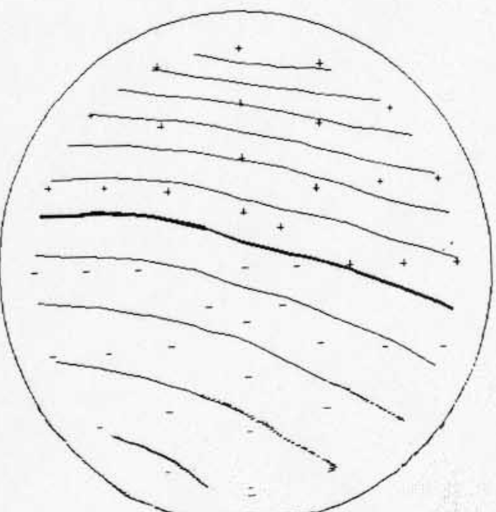


Figure 5. Sheet resistivity map for a p-type LRP Si epilayer deposited on an n-substrate. Each contour line corresponds to a 10% change. The resistivity increases across the wafer because of SiH_2Cl_2 and B_2H_6 depletion in the gas stream.

In Situ MOS Capacitors and MOSFETS

By changing the ambient gases between high temperature cycl silane to oxygen, for example, thin layers of different compositions and polysilicon on a single crystal epitaxial film) can be gro single reactor without removing the sample from the processing Because the system is essentially a cold-wall reactor without a su only the wafer gets heated during a deposition or growth cycle "history" effects from one cycle to the next due to wall and s deposition should be negligible.

A stringent test of such a system for practical application VLSI can be obtained from a study of the properties of MOS ca deposited in situ in an LRP chamber [4]. Oxidation was performe oxygen ambient with 4% HCl at a temperature of 1150°C in a pre 500 Torr. A typical oxidation time of 2 minutes yielded an oxide t of approximately 250Å. This oxide was capped in situ by a laye boron-doped polysilicon using SiH_4 at a substrate temperature of 580

Conventional high and low frequency capacitance-voltage meas were performed to measure the quality of the substrate silicon dioxide interface. From the high frequency curve, the oxide th substrate doping, and interfacial fixed charge can be extracted. determined by this process to be $2x10^{11}/cm^2$, which is comparable current industrial state-of-the-art. The interface state density middle of the gap was determined to be $3x10^9/cm^2$ eV, which comparable to the state-of-the-art.

After the polysilicon deposition, one of the samples proc situ received a further 1150°C, 15 second anneal in an argon It is well known that such anneals improve interface quality. anneal the fixed charge was reduced to $1\text{-}4x10^{10}/cm^2$. The breakdo measured for the oxide by tunneling measurements was determine 10 MV/cm, the value expected for high quality SiO_2 films.

The quality of the MOS capacitors fabricated encouraged us to with the fabrication of MOSFETS [7]. For these experiments epitaxial silicon layer was grown selectively through a previously oxide hole onto a heavily doped silicon substrate. The primar gases for this experiment were 7% SiH_2Cl2 and 2% HCl in an H_2 The HCl flow was chosen to achieve selective growth; i.e., to grow silicon in the oxide holes but to avoid polysilicon depositio of the field oxide. For n-channel MOSFETS, 1.8µ of p-type epi on a p+ substrate. 1.8µ of n-type epi was grown on an n+ subs p channel devices. The pressure during these epitaxial growth 4.2 Torr, the wafer temperature was 925°C, and the growth approximately 1µ/min. The epitaxial layer doping in both c approximately $5x10^{16}/cm^3$. The epitaxial layer grown by this pr roughly 3 times thicker than the field oxide. The detailed the faceting at the edge of the epitaxial silicon surface investigated. Gate oxide and doped polysilicon layers were t and patterned with the gate being used as a self-aligned implantation of source and drain wells. Rapid thermal annealin source drain implants was performed to minimize out-diffusion heavily doped substrates.

The n channel devices were found to have threshold voltage ± .05 V and electron surface mobility of 500 $cm^2/Vsec$. For the devices we obtained a threshold voltage of -0.8 ± .05 V and a hol of 120 $cm^2/Vsec$. In subsequent experiments on non-selective layers we have achieved electron and hole mobilities in exce $cm^2/Vsec$ and 200 $cm^2/Vsec$, respectively. The sub-threshold be both types of devices was well behaved. Both n and p channe showed sub-threshold slopes of approximately 90 mV/decade. T to substrate breakdown voltages for both types of devices ra

12 to 20 volts. Such breakdown voltages are consistent with the measured epitaxial layer doping.

III-V Compounds

In this section we report on the thermally switched growth of epitaxial layers of GaAs and related compounds. Layers of GaAs were grown with trimethylarsenic and trimethylgallium. We have also used the technique with equal success to grow $Al_xGa_{1-x}As$ (0<x<.25) and $In_yGa_{1-y}As$ (0<y<0.1), both on GaAs substrates. Good electrical characteristics and surface morphology, featureless to within the resolution of Nomarski microscopy (1100 X), have been consistently obtained. This technique maintains a growth rate of 10 Å/sec at atmospheric pressure while producing abrupt interfaces. The substrates used for these experiments were undoped and Si-doped Czochralski (100) material. These were degreased and given a 5:1:1 H_2SO_4:H_2O_2:H_2O etch prior to loading. Layers were grown at 670 to 720°C with a 3.5 litre/min flow of H_2 carrier gas and a trimethylarsenic pressure of about 0.5 Torr. Gallium arsenide layers having n-type background doping in the range of $2x10^{16}/cm^3$-$10^{17}/cm^3$ and electron mobilities of 2500-3000 cm^2/Vsec at room temperature were grown. We believe the high background doping is due to impurity incorporation from the trimethylarsenic, as has been reported [8]. Trimethylarsenic was selected on the basis of safety; we believe that superior films could be grown with arsine.

For the growth of III-V compounds, the wafer rests on a thin (20 mil) graphite susceptor which is heated from the underside by a bank of high power tungsten halogen lamps, as in a rapid thermal annealer. Temperature is measured with a thermocouple inserted down a 2mm outer diameter sealed quartz tube in contact with the susceptor (Fig. 6). We believe that supporting this sample on quartz pins alone and measuring temperature with an optical pyrometer would improve this technique by reducing thermal rise and fall times. To date wall deposition prevents this from being a useable strategy.

As was the case for silicon, a critical test of such a system lies in its ability to grow multi-layer compound heterostructures with abrupt interfaces. In Fig. 7, we show a process timing diagram for the growth of a $GaAs/Al_xGa_{1-x}As$ multilayer structure. Figure 8 is an Auger depth

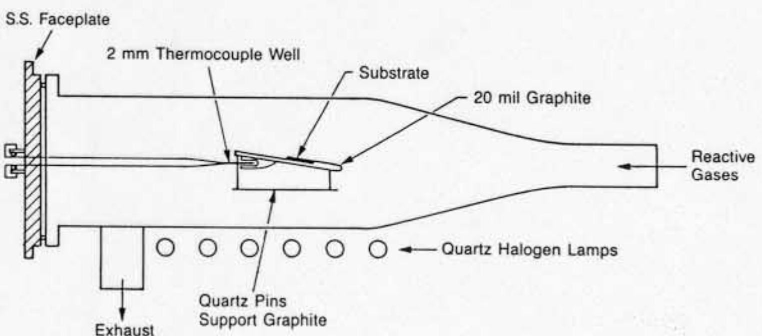


Figure 6. Schematic drawing of the quartz reaction chamber used in our experiments. The wafer sits on a low thermal mass graphite susceptor and temperature is monitored by a thermocouple sheathed in a 2 mm outer diameter quartz tube.

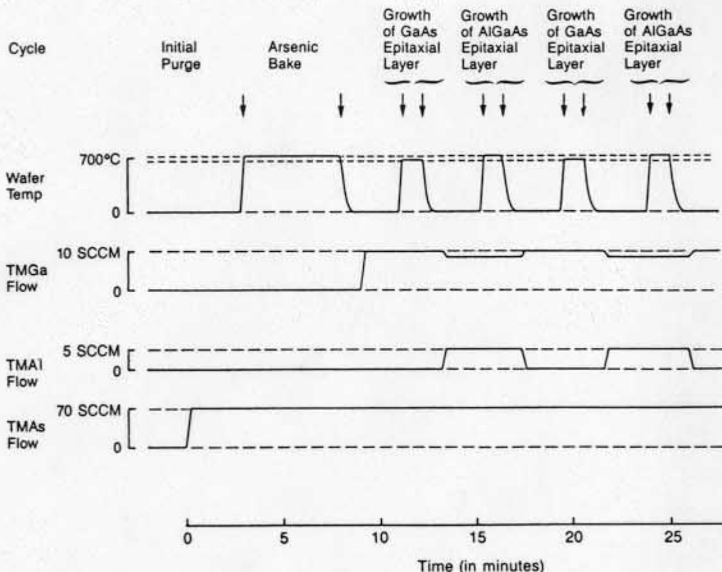


Figure 7. LRP process timing diagram showing how layers are g pulsing the wafer temperature in the presence of the correct gases.

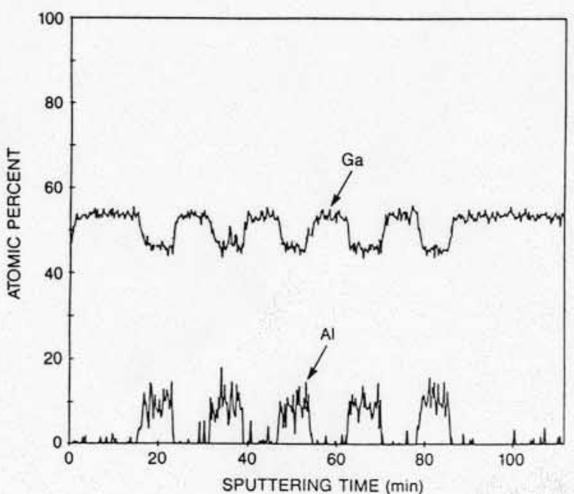


Figure 8. Sputtering Auger profile for sample 135 showing a s of alternating $GaAs/Al_{.12}Ga_{.88}$ As layers. Total thickness 6000 Å. Aluminum scaled by 2 (Charles Evans & Associates, City, CA).

profile of the resulting epitaxial layers. The GaAs was grown at 670°C and the AlGaAs at 720°C, these temperatures giving the best mobility and surface morphology for single layers of each material. We have grown from 3 to 11 layers of this type with layer thicknesses of 300Å to 2500Å by simply repeating a sequence of rapid thermal steps. The structures have excellent surface morphology and electrical characteristics equivalent to single layers grown by conventional MOCVD in our reactor. Rutherford backscattering and ion channeling analysis shows no evidence of crystal defects at the interfaces. Minimum channeling yields are about 4%, the same as bare GaAs wafers.

The microstructure of the $Al_xGa_{1-x}As$ superlattice was investigated with high-resolution transmission electron microscopy (HRTEM). Direct crystal lattice imaging was performed on the <100> zone axis. As may be seen in Fig. 9, the layers are planar with well defined interfaces and no observed defects. The image contrast at layer interfaces is confined to a two monolayer thickness. Lattice continuity is not disrupted. The origin of the image contrast is not known, but it may be due to carbon contamination or slight interfacial stress. Layer thickness calibrated with (100) lattice fringe spacings are 450Å for the $Al_xGa_{1-x}As$ layers and 340Å for the GaAs.

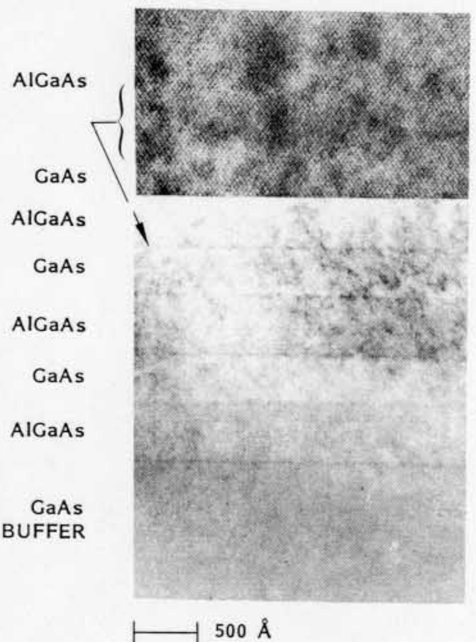


Figure 9. Lattice image Transmission Electron Micrograph of a GaAs/ $Al_{.12}Ga_{.88}As$ multilayer structure. The inset shows that layers are abrupt to within 2-3 atomic planes.

SUMMARY

High quality epitaxial films of Si on a silicon substrate ha grown using the LRP technique. Doping abruptness, defect densi foreign atom precipitation are acceptable for demanding VLSI applic Selective silicon epitaxy has also been achieved using HCl and in the gas stream; and epitaxial growth of Si_xGe_{1-x} alloys has al achieved. MOSFET structures have been fabricated with the critical grown in-situ without removing the substrate from the reaction chambe

GaAs, $Al_xGa_{1-x}As$ and $In_yGa_{1-y}As$ have also been grown on Ga TMAs, TMGa and TMAl precursors. These layers show good crystalline but have reached impurity levels that are somewhat higher than (mid-10^{16} to 10^{17}). This is currently believed to be due to imp introduced from the trimethyl source gases.

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