A Lateral Silicon-on-Insulator Bipolar Transistor with a Self-Aligned Base Contact

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Abstract—**A novel lateral bipolar transistor structure in silicon-on-insulator (SOI) is presented. The structure allows for a minimum geometry base width yet still provides for a metal contact to the entire base region. Fabricated transistors exhibit a base resistance of less than 20 Ω.**

I. Introduction

THE advantages of bipolar transistors over MOSFET's for driving large loads and sensing low currents are well known. Several merged bipolar–CMOS processes have indeed emerged in conventional bulk technology which exploit these advantages [1]–[3]. These merged processes make use of the inherent vertical n-p-n structures present in a bulk CMOS process. In a thin-film silicon-on-insulator (SOI) CMOS technology, such vertical structures do not exist. Lateral bipolar transistors are, however, ideally suited to a thin film, and have the potential for sharing fabrication steps with MOSFET's. Unfortunately, lateral bipolar transistors suffer from an inherent performance limitation related to the base width and the base series resistance. In this letter a lateral bipolar SOI transistor structure is introduced which overcomes this inherent trade-off.

In a conventional lateral bipolar transistor, one can choose to make the base width the lithographic minimum dimension. This narrow base width minimizes the base transist time, but forces the base contact to be placed outside the active region. This leads to a high base resistance which can reduce the speed of the device and lead to severe current crowding. A 0.5-μm-thick film doped 10^{17} cm^{-3} p-type in the base region would have a sheet resistance of 4 k$\Omega/\square$. Hence, in a device with a base width of only 1 μm, current crowding would render all but the first few micrometers of the device useless. Alternatively, one could make the base wide enough such that one could fit a metal contact along the entire base region. Such a device would have a low base resistance, but the wider base width would severely affect the switching speed of the device because of the increased base transit time. Our new structure employs a narrow-base pedestal which can be contacted without any critical lithography. This allows for a minimum-geometry base width yet still provides for a metal contact to the entire base region. The details of the structure are discussed in the next section.

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II. Fabrication

The "starting" materials for the fabrication were 1-μm-thick strip-heater recrystallized silicon films on 2 μm of underlying oxide. The films were recrystallized using a "slow" scan which yielded films which were free of subgrain boundaries [4]. The dominant defect in the films was an array of threading dislocations with a spacing between dislocations of 75 μm perpendicular to the scan direction and a spacing of ~ 1 μm along the scan direction. The films were patterned into individual islands for device isolation and were then implanted to provide a uniform boron doping of 8×10^{16} cm^{-3}. Then 2000 Å of thermal oxide was grown by thermal oxidation, followed by a second boron implant chosen to have its peak at the silicon surface and yield a surface dopant concentration of 10^{20} cm^{-3}. Lithography was then used to define narrow stripes of photoresist which would eventually define the base region. These stripes ranged down to approximately 2 μm in width, the lithographic minimum dimension for the tools we used. (This mask was actually the "gate" mask of a standard MOS test set.)

The photoresist stripes were then used as a mask for the vertical plasma etching of the oxide, followed by vertical etching of the silicon. The silicon etch was adjusted to etch approximately halfway through the silicon film. Arsenic ion implantation and annealing were then used to form the n^+ emitter and collector regions on either side of the silicon pedestal in the base. The photoresist and oxide masked the implant from penetrating into the base region. At this point the structure resembled that diagrammed in Fig. 1(a). Note that the base width corresponds to the lithographic minimum dimension. Structures similar to this have been described previously [5], [6]. However, in these structures the base regions were still contacted outside the active device region, leading to potential base-resistance problems.

Following the collector–emitter implantation, the photoresist and oxide were removed and the implant was annealed. An oxide deposition and planarization were performed. A lithography step then defined holes for the contact to the base region, and a wet oxide etch was done to expose the top of the base pedestal but not to expose the n^+ regions (Fig. 2(b)). Conventional definition and etching of the collector–emitter

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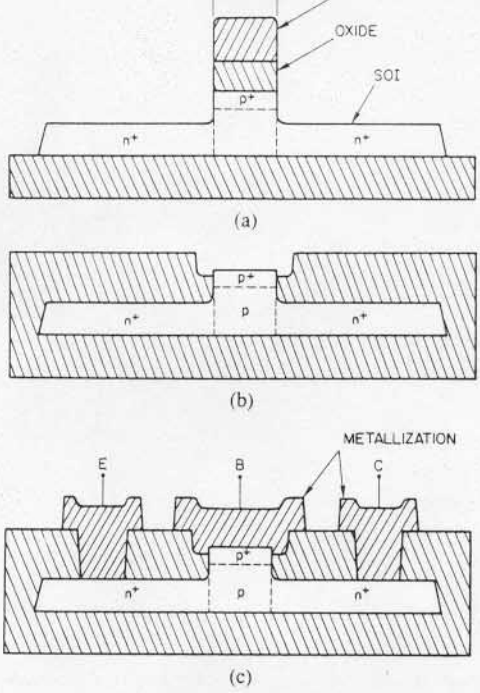

Fig. 1. Cross section of the device structure (a) after the collector–emitter implant, (b) after the base contact etch, and (c) after the completion of processing.

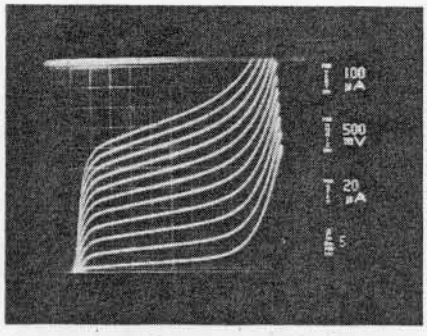

Fig. 2. Common-emitter curve-tracer characteristic of a 2-μm device.

contacts and a multilayer metallization step completed the processing.

Although the base width corresponds to the lithographic minimum dimension, no critical lithography or alignment was required to make a metal contact to the entire base region. The heavy p^+ doping at the top of the base pedestal serves two purposes. First, it provides for a low-resistance ohmic contact. Second, it provides a built-in electric field which repels minority-carrier electrons in the base away from the metal base contact. Electrons reaching the base contact would recombine and give rise to base current, not the collector current desired in normal bipolar transistor operation.

III. Results

Transistors were fabricated having nominal base widths from 2 to 10 μm, and a device length of 50 μm. (This corresponded to the MOS "gate" mask used for the base definition having a series of W/L from 50/2 to 50/10.) Shown in Fig. 2 is a common-emitter curve-tracer characteristic of a breakdown voltage V_{CEO} of 4–7 V, and had a typical current gain of 2.

Considering the doping profiles used in the transistors, the 2-μm device might have been expected to exhibit current gain on the order of 10–50. To identify the cause of the low current gain, measurements were made on transistors of different base widths. It was found that the gain of the transistors was strongly dependent on base width (Fig. 3). The exponential dependence of gain on the base width means that most of the electrons injected into the base at the emitter are recombining before they diffuse across the base to the collector. From the slope in Fig. 3, an effective lateral minority-carrier diffusion length of 1.4 μm can be extracted.

Because the silicon film is thin, the lateral diffusion of minority carriers will be limited by recombination at the film interfaces as well as by recombination within the "bulk" of the film itself. Of special concern in our case is possible recombination at the metal base contact on top of the base region. To test if the vertical built-in base field indeed was successful in repelling electrons away from the base contact, a second series of lateral transistors was fabricated in identically prepared films. This series of transistors had the base contact outside the active device region, and no p^+ surface implant to create a vertical field. The interface on top of the base region in this case was an annealed silicon–silicon dioxide interface, presumably one with a low surface recombination velocity. The collector current of these devices also had an exponential dependence on base width, with a characteristic length of 1.5 μm. Comparing this to the earlier diffusion length of 1.4 μm, we conclude that recombination at the metal base contact was not the site of the dominant recombination in the self-aligned devices. This leaves the "bulk" of the SOI film or the bottom interface as the location of the dominant recombination centers.

A major goal of this device design was to minimize the base resistance. Measurements of the base–emitter and base–collector diodes in forward bias consistently showed a series resistance of 75–100 Ω. Because the mask set used for the devices was based on a standard MOS test set, the collector–emitter contacts were removed ~ 50 μm from the active device. The sheet resistance of the collector and emitter regions was $\sim 50\ \Omega/\square$, and hence largely responsible for the above series resistance. (An optimized device would of course have the emitter and collector contacts very close to the base region.) By connecting the emitter and collector together and repeating the above measurements, it is possible to separate the effects of base resistance and those of emitter (collector) resistance. Although this analysis was limited by a nonzero probing resistance, we were able to establish an upper limit to the base resistance of 20 Ω—an exceptionally low number.

IV. Discussion

The motivation for this work was to develop a bipolar transistor to merge with a thin-film SOI (SOS) CMOS process. One can make a vertical bipolar transistor directly in a thin (0.75 μm) film, but such a structure has too large a collector resistance to be a useful driver [7]. Alternatively, one might

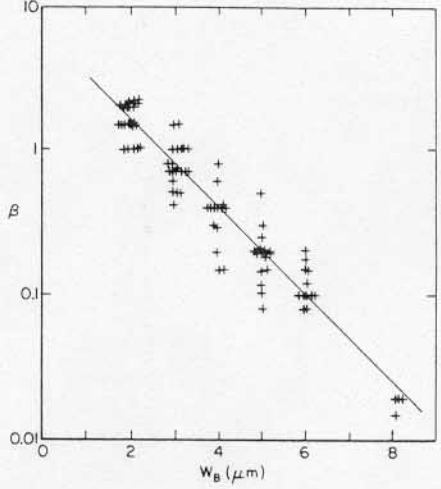

Fig. 3. Gain versus base width for the self-aligned devices.

grow epi on the thin SOI film for vertical bipolar transistors [8], [9]. Such an approach, however, would greatly complicate the fabrication process. Hence we resorted to lateral structures. By providing a body contact to a SOI MOSFET, one can operate the device as a lateral bipolar transistor [10], [11], but, as pointed out earlier, the usefulness of such a structure is inherently limited because of the base resistance. Our structure overcomes the above limitations, and could be merged with an SOI CMOS structure with only one or two extra masks. In addition to using 1-μm-thick films for our fabrication process, we have also used 0.4-μm-thick films coated with a 0.5-μm layer of polysilicon and achieved similar results. These thinner starting films would be more compatible with advanced short-channel CMOS fabrication processes.

Simple calculations show the speed of the device to be dominated by the base transit time down to base widths of less than 0.5 μm. In a one-dimensional approximation, the base transit time τ_B is given by $W_B^2/2D_n$. For example, a 0.5-μm device would have a base transit time of roughly 60 ps. While this is not small compared to the transit time of modern digital bipolar circuitry, it is probably adequate to serve as a driver for merged CMOS–bipolar applications. Because the device is isolated on all sides by oxide, the parasitic capacitances in the device should be small. One drawback, however, is the absence of a lightly doped collector region. Such a lightly doped region is necessary for a minimum base–collector capacitance.

The gain of the devices was shown earlier to be limited by a minority-carrier diffusion length of only 1.4 μm. This occurred despite the fact that the devices were small enough and oriented so that the active regions fit between the dislocation defects mentioned earlier. For a gain of 50, base transit considerations require a diffusion length of 10 W_B (10 μm for a 1-μm device). Recombination diffusion lengths of from 5 to 10 μm have been observed in some strip-heater recrystallized films [10], [11]. Experiments are underway to identify and remove the source of the recombination (film defects, interface states, etc.) in our films.

V. Conclusion

A novel lateral bipolar structure has been developed that allows for both a minimum-geometry base width and a metal contact to the entire base region. Fabricated devices did indeed exhibit an extremely low base resistance, while the current gain of the devices appeared to be limited by recombination in the SOI film. While this device was developed with merged SOI (SOS) CMOS processes in mind, the basic structure should be adaptable to bulk lateral transistors as well.

Acknowledgment

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