

Hole Mobility Enhancement in MOS-gated $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ Heterostructure Inversion Layers

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In this work effective mobility enhancements of 50% at *room temperature* for holes in $\text{Ge}_x\text{Si}_{1-x}$ inversion layers (compared to Si control devices) and over 100% at 90 K are demonstrated. This is important since the mobility of carriers in the inversion layer of a MOSFET is significantly less than that of carriers in the bulk semiconductor. The reduced mobility is due to the increased scattering of carriers closely confined to the Si/SiO₂ interface by the strong transverse electric field of the gate. This fact is particularly troublesome for Si PMOS devices which have an intrinsically lower hole mobility to begin with. Placing a buried epitaxial $\text{Ge}_x\text{Si}_{1-x}$ layer 50 to 100 Å beneath the gate of a PMOS transistor should lead to confinement of holes in the $\text{Ge}_x\text{Si}_{1-x}$ layer (away from the surface scattering sites) and thus to an enhanced (i.e. more bulk-like) mobility. Low frequency capacitance-voltage methods and Hall measurements have shown that an inversion layer does form in the $\text{Ge}_x\text{Si}_{1-x}$ well, but low field mobility enhancement results have yet to be presented. We also will show the devastating impact that misfit dislocations have on mobility, with structures that exceed the $\text{Ge}_x\text{Si}_{1-x}$ critical thickness. The buried $\text{Ge}_x\text{Si}_{1-x}$ layers and Si caps were grown epitaxially on a Si (100) substrate by Rapid Thermal Chemical Vapor Deposition using dichlorosilane and germane at 625°C. The epitaxial films are doped n-type with concentrations of $\approx 1 \times 10^{16} \text{ cm}^{-3}$. Sources and drains were implanted with boron at 25kV and 50kV with a total dose of $5 \times 10^{14} \text{ cm}^{-2}$. A plasma deposited gate oxide of 100 Å was used. This deposition was followed by a 700°C/30 min. N₂ furnace anneal. Contact holes for the source and drain were opened and aluminum was evaporated to form the gate and source/drain contacts. Three variations of the buried channel structure were grown and analyzed, sample 646 which had a $\text{Ge}_{.2}\text{Si}_{.8}$ well and a 75 Å Si spacer, sample 649 which had a $\text{Ge}_{.3}\text{Si}_{.7}$ well and a 105 Å Si spacer and sample 650 which had a $\text{Ge}_{.4}\text{Si}_{.6}$ well and a 75 Å Si spacer. Samples 646 and 649 had $\text{Ge}_x\text{Si}_{1-x}$ layers below critical thickness and 650's $\text{Ge}_x\text{Si}_{1-x}$ layer exceeded critical thickness. A prime Si (100) wafer was also processed as a

control (to account for processing dependent effects). Simulations using a 1-D Poisson solver predict that the structures of both sample 646 and sample 649 will have a hole concentration of $1 \times 10^{12} \text{ cm}^{-2}$ in the $\text{Ge}_x\text{Si}_{1-x}$ well inversion layer before the Si/SiO_2 surface also inverts. The holes added to the inversion layer at the Si/SiO_2 interface should have the same effective mobility as a typical PMOS device so any benefit should be obtained only from the holes in the $\text{Ge}_x\text{Si}_{1-x}$ inversion layer. At room temperature the drain conductance of MOSFETs made from sample 646 had a 25% larger drain current than the Si control devices and the MOSFETs from sample 649 had a 50% larger current. The trend to increased mobility as the holes are confined progressively further from the interface is clear. The effective mobility was also correspondingly higher, sample 649 had a peak mobility of over $200 \text{ cm}^2/\text{V}\cdot\text{s}$ at room temperature and a 50%+ enhancement of the effective mobility across the whole range of effective fields. The $\text{Ge}_x\text{Si}_{1-x}$ MOSFETs in samples below critical thickness had the same subthreshold slope (110 mV/decade) as those of the Si devices, which indicates that the presence of the buried $\text{Ge}_x\text{Si}_{1-x}$ layer did not induce excessive interface states. As the temperature is reduced the mobility enhancement of the $\text{Ge}_x\text{Si}_{1-x}$ devices becomes progressively larger (over 100% enhancement at 90 K). The peak mobility for the $\text{Ge}_x\text{Si}_{1-x}$ devices at 90 K was over $750 \text{ cm}^2/\text{V}\cdot\text{s}$. The upper mobility of our devices may have been limited by the high fixed charge in the plasma deposited oxide, as suggested by the relatively poor performance of our Si control device compared to previously published data. In contrast to the significant improvement in effective mobility seen in samples 646 & 649 the performance of PMOS devices made from sample 650 was markedly worse than that of the Si control. It is strongly suspected that this device had misfit dislocations at the $\text{Si}/\text{Ge}_x\text{Si}_{1-x}$ interface since this device has a $\text{Ge}_x\text{Si}_{1-x}$ well that is well above the equilibrium critical thickness, had very short lifetimes (capacitors would not deep deplete) and subthreshold slopes that were twice those seen in the other devices. This is evidence that dislocations at the heterojunction interface act as scattering sites to reduce mobility. In conclusion it is shown that a significant improvement in the effective mobility of PMOS devices can be achieved by incorporating a buried $\text{Ge}_x\text{Si}_{1-x}$ epitaxial layer. Graduate student support was provided through DOE contract # DE-ACO2-76-CHO3073 and the NSF contract # 8615-7227.

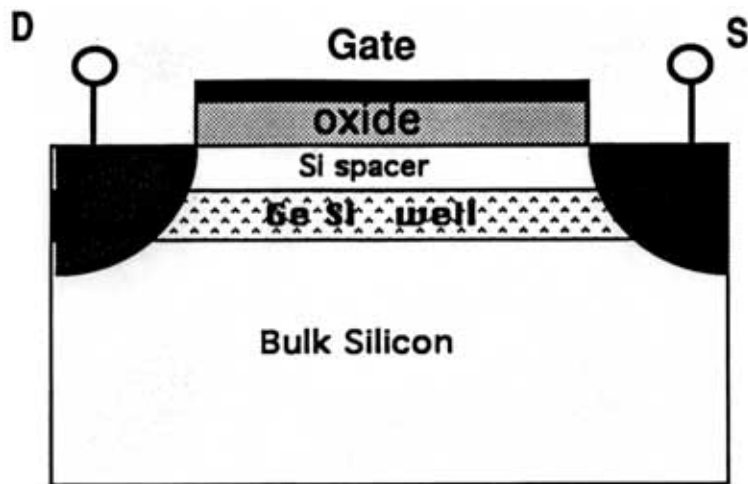


Figure 1: Cross section of a buried channel PMOS device. The GeSi well typically lies 50-100 μm beneath the gate and has a Ge fraction of 0.2-0.4.

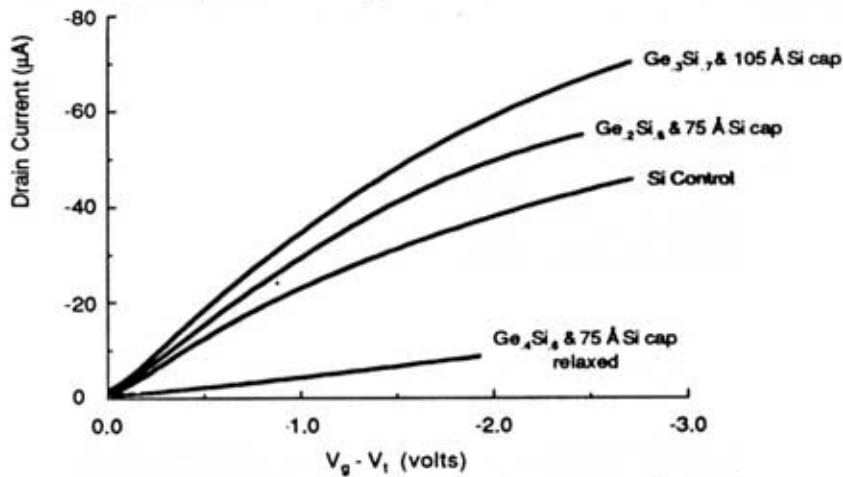


Figure 2: Comparison of the drain conductance curves of several $\text{Ge}_x\text{Si}_{1-x}$ devices to a Si control device. $V_d = -0.2$ volts.

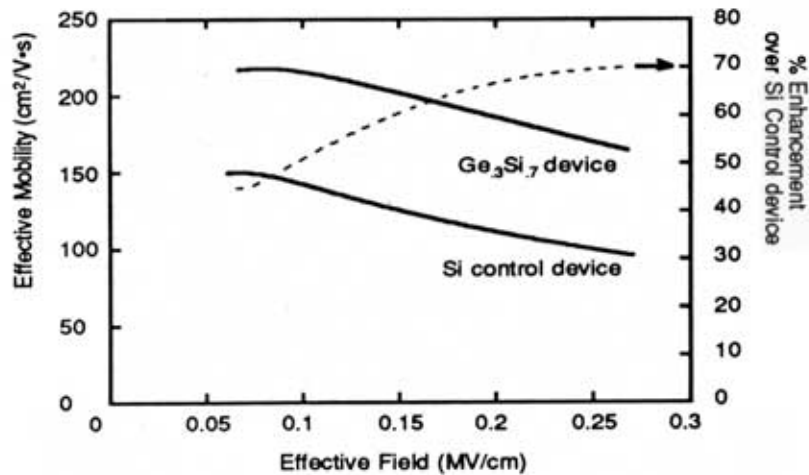


Figure 3: Comparison of effective mobility at 290 K between a device with a Ge_3Si_7 well and a 105 Å Si spacer and the Si control.

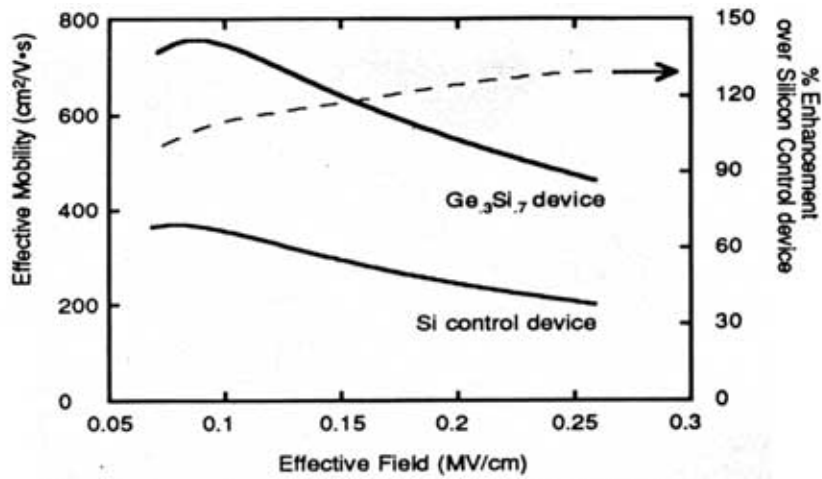


Figure 4: Comparison of effective mobility at 90 K between a device with a Ge_3Si_7 well and a 105 Å Si spacer and the Si control.

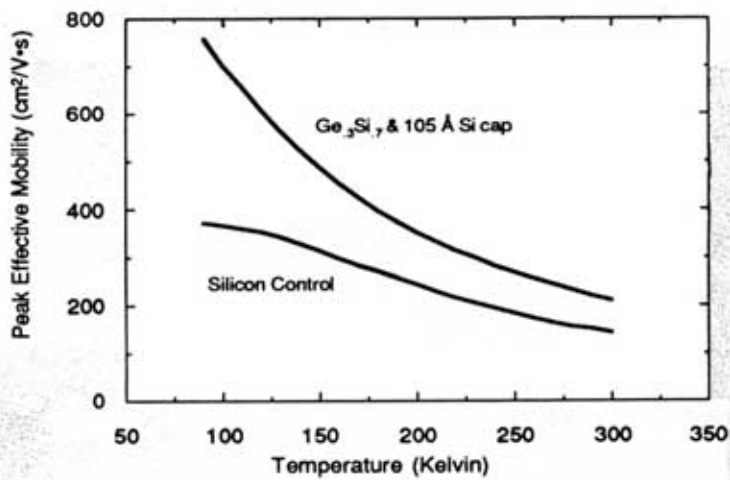


Figure 5: Comparison of peak effective mobility vs. temperature for a Ge_3Si_7 , 105 Å Si spacer device and a silicon control device.

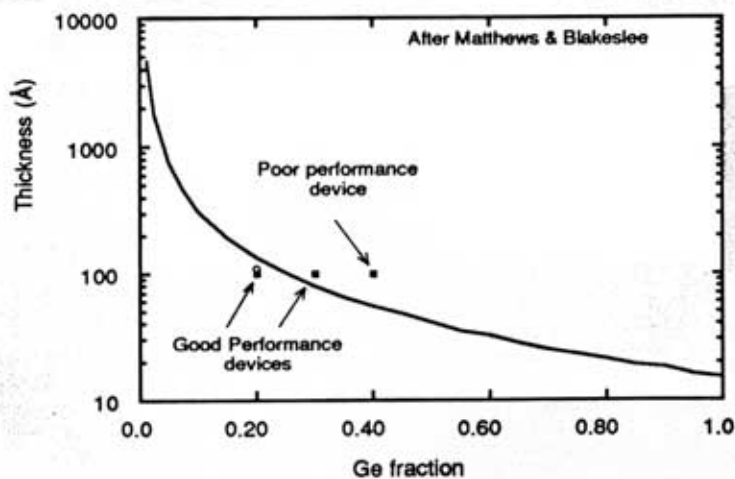


Figure 6: Relation of device structures to equilibrium critical thickness.