

In-Situ Epitaxial Silicon-Oxide-Doped Polysilicon
Structures for MOS Field-Effect Transistors

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Abstract—Limited reaction processing (LRP) has been used to achieve the *in-situ* growth of epitaxial silicon-oxide-doped polysilicon layers. The *in-situ* growth of these multiple layers was combined with the selective epitaxial growth technique to create structures for MOSFET fabrication. The results of n- and p-channel transistor fabrication utilizing these structures are presented.

I. INTRODUCTION

THE silicon substrate-oxide-doped polysilicon structure forms the heart of the modern MOSFET. For some CMOS isolation techniques, a silicon epitaxial layer is added to create a substrate-epi-oxide-polysilicon sandwich [1]–[4]. Conventionally, these layers are each fabricated in a separate step in a separate reactor, and the wafers must be physically transported from one reactor to another. In this letter we report the *in-situ* fabrication of epi-oxide-polysilicon structures and present the performance of n- and p-channel MOSFET's fabricated using these structures.

The multiple-layer structures were fabricated using the limited reaction processing (LRP) technique [5]. This method uses rapid changes in sample temperature to control the growth or deposition of thin high-quality semiconductor or insulator layers. The LRP system has been described previously [5]. It consists of a quartz reaction tube surrounded by microprocessor-controlled tungsten lamps. One end of the reaction tube is connected to a gas control system which can supply several conventional processing gases such as Ar, O₂, SiH₄, etc. The other end is connected to a low-pressure pumping apparatus. Silicon samples in the reaction tube can be brought to typical processing temperatures (e.g., 1000°C from room temperature) in a matter of seconds. By changing the process gases in the reaction tube between high-temperature cycles, multiple semiconductor and insulator layers may be sequentially grown or deposited *in situ*, i.e., without removing the wafer from the reaction chamber.

We have previously used this technique for the sequential *in-situ* growth of a thin oxide and then the deposition of doped polysilicon for the fabrication of MOS capacitors [6]. How-

ever, that work did not include an epitaxial silicon layer and was not extended to a fabrication process for MOSFET's.

II. FABRICATION

The starting materials for the experiments were (100) Sb-doped n-type silicon wafers for p-channel FET's and (100) B-doped p-type wafers for n-channel devices. Both types of substrates had a resistivity of $\sim 0.01 \Omega \cdot \text{cm}$. Two-inch squares were cut from larger wafers to fit into the limited reaction processing tube. Initially, a uniform field oxide of thickness 6000 Å was grown by wet oxidation at 1100°C in a conventional furnace. Holes in the field oxide for subsequent selective epitaxial growth were then opened using a conventional "diffusion" mask and wet chemical etching. After a chemical cleaning, the wafers were loaded into the LRP chamber and baked in H₂ for 30 s at 1150°C and 1.0 torr. Three successive high-temperature steps were then carried out to create the structure in Fig. 1(a). These steps were: 1) selective epitaxial silicon growth; 2) gate oxidation; and 3) doped polysilicon deposition. The process gases were changed and purge cycles were performed between the high-temperature steps, but the vacuum seal to the chamber was not broken.

The primary source gases used for the epitaxial growth were 7-percent SiH₂Cl₂ and 2-percent HCl in an H₂ carrier. The HCl flow was chosen to achieve selective growth, i.e., to grow epi in the oxide holes but to avoid polysilicon deposition on top of the field oxide. For n-channel MOSFET's, 1.8 μm of p-type epi was grown on a p⁺ substrate (sample LRP 169), and 1.8 μm of n-epi was grown on an n⁺ substrate for p-channel devices (sample LRP 171). The pressure during the epitaxial growth was 4.2 torr, the wafer temperature was 925°C, and the growth rate was $\sim 1 \mu\text{m}/\text{min}$. The epitaxial layer doping in both cases was $5 \times 10^{16} \text{ cm}^{-3}$. Note that the epitaxial layer was some three times thicker than the field oxide. The detailed nature of the faceting that occurs at the edge of the epitaxial silicon surface [7] was not investigated.

The gate oxidation was performed at 1150°C in an oxygen ambient at a pressure of 500 torr for a period of 60 s. The gate oxide thickness was 140 Å. After the oxidation, heavily doped p-type polysilicon was deposited using silane and diborane at 580°C and 1.5 torr. The polysilicon layer thickness was 0.3 μm.

After the LRP steps, conventional processing (beginning with gate lithography and etching) was carried out to create the MOSFET structures shown schematically in Fig. 1(b). Rapid thermal annealing of the source-drain implants was performed to minimize outdiffusion from the heavily doped substrate.

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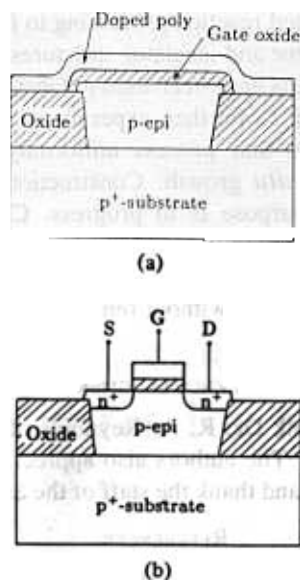


Fig. 1. (a) Multiple-level epi-oxide-poly structure grown *in-situ* by LRP, and (b) the schematic cross section of MOSFET's made from this structure. Note that the actual epitaxial layer in our experiments was three times thicker than the field oxide.

During the back-end processing, the wafers were subjected to a total of 15 min at 900°C. A titanium-aluminum metallization and a 400°C forming gas anneal completed the processing.

III. RESULTS

On-chip capacitor test structures confirmed the gate oxide thickness of 140 Å and showed an epitaxial layer doping of $4-5 \times 10^{16} \text{ cm}^{-3}$ for both the p and n epitaxial layers. Both the n- and p-channel MOSFET's exhibited qualitatively well-behaved characteristics. A curve-tracer photograph of a typical short-channel n-MOS device is shown in Fig. 2. (The effective channel length of 0.8 μm was determined by measuring the transistor conductance for many different gate lengths at several different gate biases.) The typical performance of a p-channel device (with $L_{\text{eff}} = 1.0 \text{ μm}$) is shown in Fig. 3.

Threshold voltages and channel mobilities were extracted from long-channel (50-μm) devices in the triode regime. The n-channel transistors had a threshold voltage of $1.25 \pm 0.05 \text{ V}$ and an electron surface mobility of $490 \pm 10\text{-percent cm}^2/\text{V}\cdot\text{s}$. Given the epi doping concentration of $5 \times 10^{16} \text{ cm}^{-3}$, a surface mobility of $600 \text{ cm}^2/\text{V}\cdot\text{s}$ might have been expected [8]. However, the CV measurements indicated a surprisingly high fixed charge at the epi Si-SiO₂ interface ($N_f \sim 5 \times 10^{11} \text{ cm}^{-2}$). Excess scattering caused by these charge centers can reduce surface mobilities [8]. The reason for this large interface charge is not known. The p-channel devices had a threshold voltage of $-0.80 \pm 0.05 \text{ V}$ and a hole mobility of $120 \text{ cm}^2/\text{V}\cdot\text{s}$. The subthreshold behavior of the devices was also well behaved. Both the n- and p-channel devices showed subthreshold slopes of approximately 90 mV/decade. The source (drain)-to-substrate breakdown voltages for both types of devices ranged from 12 to 20 V. Such breakdown voltages are consistent with the measured epitaxial layer doping.

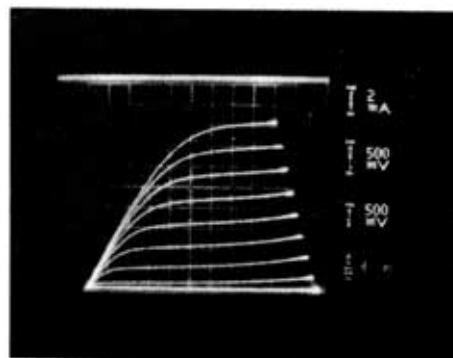


Fig. 2. Curve-tracer characteristics of a typical n-channel device with $L_{\text{eff}} = 0.8 \text{ μm}$ and $W = 50 \text{ μm}$.

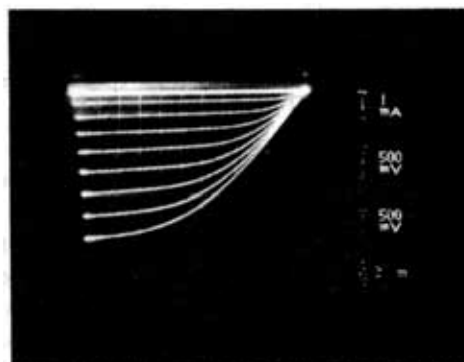


Fig. 3. Curve-tracer characteristics of a typical p-channel device with $L_{\text{eff}} = 1.0 \text{ μm}$ and $W = 50 \text{ μm}$.

The low carrier mobilities and the high interfacial charge indicate some material problems at the epitaxial layer-thin oxide interface. Although it is conceivable that the high fixed charge is related to the *in-situ* processing, it is more likely that the selective epitaxial growth step was not properly optimized. Uniform nonselective epitaxial silicon layers grown by LRP have been shown to exhibit excellent material and electrical properties [5], [9]. These include minority-carrier lifetimes in the range of tens of microseconds and electron and hole surface mobilities (for conventionally processed FET's) of 830 and 200 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively. It should be noted that two-step *in-situ* processing (oxidation plus polysilicon deposition) has been found to yield excellent interface quality [6].

IV. DISCUSSION

Multiple-level *in-situ* processing could reduce the inevitable contamination (particulate and chemical) that occurs when wafers are transported from one reactor to another. Cleaner interfaces between layers could lead to greater process uniformity and higher yields. Such considerations could be important for ULSI. However, the scale of the processing in these experiments (2-in wafers and discrete devices) was not sufficient to allow realistic testing of parameters such as threshold uniformity and yield.

Because limited reaction processing minimizes the high-temperature exposure of the wafer, the substrate-epitaxial layer interface remained sharp. A SIMS profile of the B

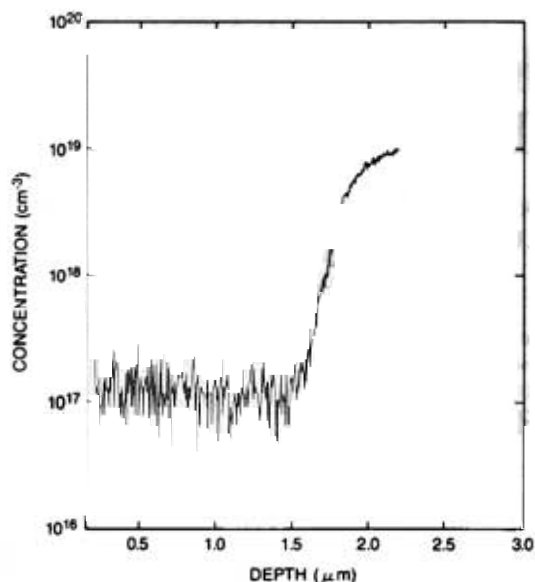


Fig. 4. SIMS profile of the boron doping in the epitaxial layer after the completion of MOSFET processing (sample LRP 169).

doping profile in sample LRP 169 after the completion of the processing shows the B concentration at the interface changes by nearly two orders of magnitude in only $0.3 \mu\text{m}$ (Fig. 4). Hence the epitaxial layer thickness could have been much thinner than the $\sim 2 \mu\text{m}$ used in these experiments without adversely affecting the transistors. Note that depositing the polysilicon *in-situ* implies that any implants for threshold shifting would have to be done through the gate polysilicon. As an alternative to such implants, the tight control of dopant profiles offered by LRP may make it possible to tailor the doping of the epitaxial layer during the layer growth. Such a technique would depend on very precise control of the dopant level in the epitaxial material, however.

In this work, n- and p-channel devices were fabricated on separate substrates. Further work is underway to combine both types of transistors onto a common substrate for complementary structures. Such a process will probably require two separate selective epitaxial steps. Because of the oxide isolation and the heavily doped substrates, the complementary structure should be rather immune to latch-up.

V. SUMMARY

The use of limited reaction processing to fabricate multiple-layer semiconductor and insulator structures has been demonstrated. These layers have been used to fabricate both n- and p-channel MOSFET's. Further experiments are necessary to evaluate the yield and process uniformity implications of multiple layer *in-situ* growth. Construction of a large-scale reactor for this purpose is in progress. Combining limited reaction processing with *in-situ* patterning (such as laser beam assisted deposition [10]) may make it possible to someday build a complete circuit without removing the wafer from the processing chamber!

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