Silicon And Silicon-germanium Epitaxy For Quantum Dot Device Fabrications Towards An Electron Spin-Based Quantum Computer

Kun Yao

A Dissertation
Presented to the Faculty
of Princeton University
in Candidacy for the Degree
of Doctor of Philosophy

Recommended for Acceptance
by the Department of
Electrical Engineering
Adviser: James C. Sturm

September 2009

Abstract

Semiconductor quantum dots are promising candidates as qubits for spin-based quantum computation as they provide highly tunable structures for trapping and manipulating individual electrons. It is the objective of this doctorate thesis to study on the development of silicon and silicon-germanium epitaxy and nanofabrication techniques for quantum dot devices, and the performance level achieved in the silicon/silicon-germanium material heterosystem.

We describe the growth of two-dimensional electron gas structures in strained Si on high-quality SiGe relaxed buffers with low temperature mobility exceeding 10,000 cm^2/Vs, currently limited by the background impurities in our RTCVD system. The modulation of the electron gases using atomic layer deposited Al_2O_3 is also demonstrated. We have developed a wide range of fabrication methods of the electron gases for quantum dot applications including nanolithography and etching techniques optimized for etch selectivity and anisotropy. Feature sizes well under 100 nm can be reliably obtained.

To achieve precise control of exchange coupling of qubits, we present a new concept of parallel 2-D electron gases in a double quantum wells as interaction dimers. A typical value of 0.1 meV for symmetric-anti-symmetric splitting of subbands is predicted by modeling. The signature of inter-well scattering is proved by a negative transconductance effect measured in such structures. The physical realization of such qubit dimers can also enable a novel "flying qubit" scalable architecture for semiconductor-based quantum computers.

The robustness of quantum dot devices is often strongly affected by defect states on the surface arising from the Si/SiO_2 interface. We demonstrate the use of epitaxial regrowth of SiGe for surface passivation, done with thermal cleaning temperatures less than 800 °C and negligible degradation of device performance. Side-gated multiple quantum point contacts are fabricated. They can be used to completely deplete

electrons on a quantum dot with gate leakage less than a few nA. We have also observed periodic single electron tunneling conductance peaks in a single quantum dot transistor with a side-gate-to-dot capacitance of 4.4 aF.

Acknowledgements

First of all, I want to thank Princeton University and the Department of Electrical Engineering for giving me this wonderful opportunity to carry out my research work in the first instance.

I am deeply indebted to my advisor Professor James C. Sturm, whose perpetual enthusiasm, stimulating insight, and constant encouragement that have shaped me throughout the years. I always feel extremely lucky to have had worked with him inside and outside the laboratory. I also wish to thank Professors Jason R. Petta and Antoine Kahn for reviewing this thesis. Furthermore, Professors Sigurd Wagner, Mansour Shayegan, Stephen A. Lyon, Daniel C. Tsui, and Stephen Y. Chou are always willing to help me whenever I need their guide. They have set a role model of a great teacher and mentor.

This thesis could not have been achieved without all the collaborators. I would like to express my gratitude to Professor Leonid P. Rokhinson and his post-doc Dr. Alexander Chernyshov at Purdue University for their low-temperature measurement, Dr. Anthony Lochtefeld and his team at AmberWave Systems for their preparation of SiGe relaxed buffers, and Professor Ya-Hong Xie at UCLA for providing MBE samples. At Princeton, I would like to thank e-beam nanolithography expert Dr. Mikhail Gaevski, TEM imaging and analysis expert Dr. Nan Yao, and Shyam Shankar from Lyon group for his help with ESR measurement. I treasured all the cooperative work experiences that made the research more rewarding for me.

A special thanks goes to all members in Sturm group. Malcolm S. Carroll, Haizhou Yin, Xiang-Zheng Bo, Eric J. Stewart, Rebecca L. Peterson, Keith H. Chung, Weiwei Zheng, Sushobhan Avasthi, and Jiun-Yun Li are all among our RTCVD hall of fame. In particular, I am obliged to Keith for his friendship and loyal support to carry the reactor upon our shoulders for nearly half decade. All other folks, including Iris Hsu, Richard Huang, Ke Long, Troy G. Abe, John A. Davis, David Inglis, Hongzheng

Jin, Bahman Hekmatshoar, Yifei Huang, Noah Jafferis, and Kevin Loutherback, contributed to make the lab a fun place to work. I would also like to thank my colleagues in Tsui group, Gabor Csathy, Yong Chen, Zhihai Wang, Keji Lai, Tzu-Ming Lu, and Dwight Luhman. They are great physicists and have offered me broad perspectives during countless discussions.

My doctoral research would be very painful if I did not have the kind support from PRISM and EE staffs. I am thankful to Dr. Helena Gleskova (now on the faculty of the University of Strathclyde in Scotland), Dr. George Watson, Dr. Conrad L. Silvestre, and Joe E. Palmer for their conscientious maintenance of the cleanroom. I truly appreciate Cathy A. Wertz, Sarah M. Braude, Carolyn M. Arnesen and Sheila R. Gunning for their generous help.

Finally, my deepest gratitude goes to my family for their love and care throughout my life; I am simply impossible without them. I grew up in a typical south China small town and have come a long way. I have no suitable words that can describe the evergreen support from my parents and brother from oversea in the past eight years. Last but not least, to my fiancée Lan, I remember all the moments with your accompanying me during the hard times. Your love enabled me to accomplish this work.

Thank you! Thank You!! Thank YOU!!!

To the victims and heroes of September 11, 2001

On that day I was sitting 50 miles away at Princeton university graduate school orientation in Richardson auditorium in Alexander Hall.

Contents

List of Tables

List of Figures

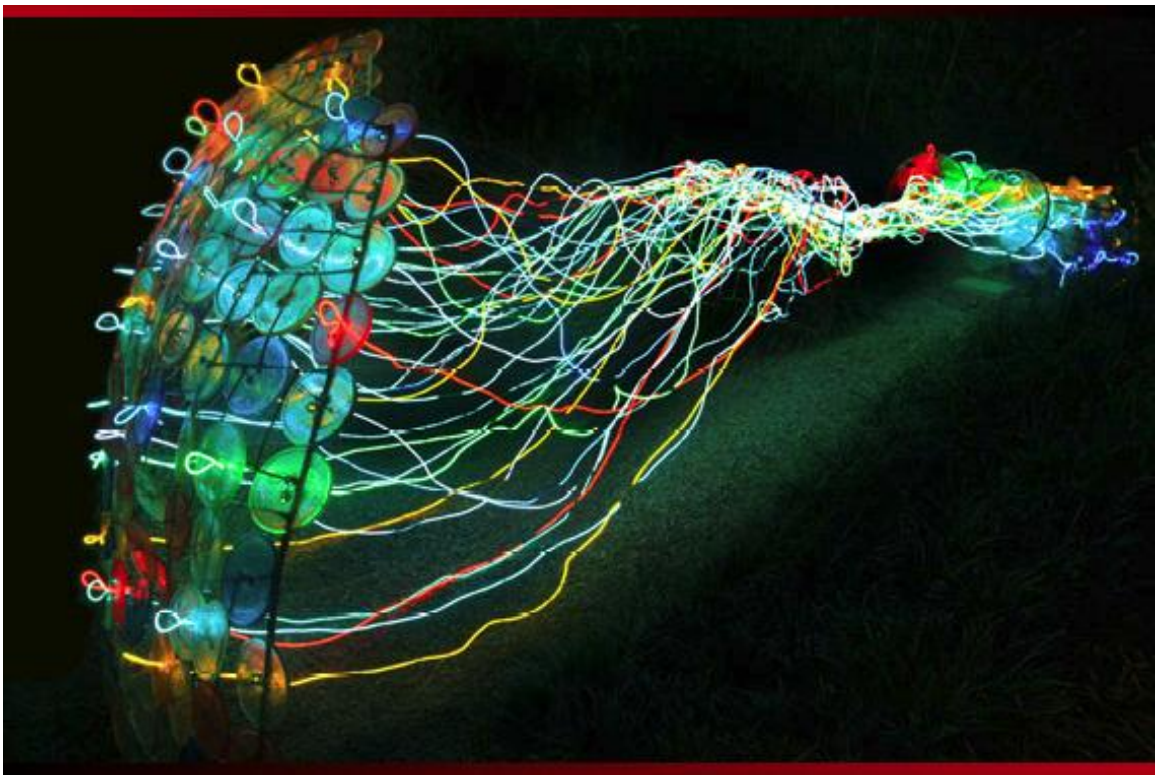


Figure 1: Sensation: Interior View (2006) is an abstract sculpture by Jersey City artist Nancy Cohen that was inspired by discussions with Princeton University President Shirley Tilghman. Tilghman, a leader in the field of molecular biology, collaborated with Cohen and Princeton University Electrical Engineering Professor James Sturm on the artwork, which is an abstraction about the sense of smell and how odors are recognized and remembered. Multi-colored cast resin discs are affixed to a steel armature forming a wall that connects to bulb-shaped structures by vibrant wires. The different colors of discs represent the sensor neurons in the nose that detect different odorant molecules; the wires represent the axonal connections that pass through the skull to the olfactory bulb in the brain, with the neurons from each type of sensor going to their own specific region in the olfactory bulb. (Image courtesy of NSF, from NSF IPAMM final report, 2007)

Chapter 1

Introduction

1.1 Motivation

As the raw material of the information age, silicon has changed the world in a revolutionary fashion over the past 50 years. Interestingly, since silicon is similar to carbon, particularly in its valency, some people have proposed the possibility of silicon-based life. Life itself as we know it could not have developed based on a silicon biochemistry. However, the impact of silicon-based microelectronics on our life is apparent all around us. And the microelectronics universe itself is still expanding dramatically.

Moore's law has been the most important and most famous benchmark for developments in silicon technology. It describes that the number of transistors on a chip will double about every two years. The integrated circuit industry has kept that pace for nearly 40 years. As of today, Intel's next-generation Itanium processors will have 2-billion transistors [1]. CMOS scaling aggressively approximates the molecular scale in less than 10 years, transistors would eventually reach the limit of miniaturization at nearly atomic levels. Then the physical laws that govern the behavior and properties of the circuit will be inherently quantum mechanical in nature, not classical any more. On April 13, 2005, Gordon Moore himself stated in an interview that the law

cannot be sustained indefinitely [2]:

> In terms of size [of transistor] you can see that we're approaching the size of atoms which is a fundamental barrier, but it'll be two or three generations before we get that far - but that's as far out as we've ever been able to see. We have another 10 to 20 years before we reach a fundamental limit. By then they'll be able to make bigger chips and have transistor budgets in the billions.

This is why we begin our journey at the level of atoms and electrons. Quantum computing, as its name suggests, may eventually allow computing to surpass the atomic level size restrictions. It represents the most promising possible final destination beyond the microelectronics roadmap. A quantum computer makes direct use of distinctively quantum mechanical phenomena to realize a fundamentally new mode of information processing. There are a number of quantum computing candidates, including those based on superconductors, Bose-Einstein condensates, quantum optics, and many others. Our work will focus on the "spintronic" quantum dot in silicon concept. This technology exploits the intrinsic spin of electrons and its associated magnetic moment, which is also the origin of the term "spintronics". A clear advantage of this route is that our experimental technique is compatible with existing complementary metal oxide semiconductor (CMOS) technology, making integration of quantum dots in silicon chips feasible.

1.2 A Brief History of Quantum Computing

The idea of a computational device based on quantum mechanics was first explored in the 1970's and early 1980's by a small number of visionaries, such as Charles H. Bennett of the IBM Thomas J. Watson Research Center, Paul A. Benioff of Argonne National Laboratory in Illinois, David Deutsch of the University of Oxford, and

Richard P. Feynman of the California Institute of Technology. The idea of a quantum gate was introduced, the basic possibilities of quantum algorithms were set forth, quantum communication (in the form of quantum cryptography) was well developed, and some rudimentary ideas of how quantum computing could be implemented were considered.

In 1994, Peter Shor, a research and computer scientist at AT&T's Bell Laboratories in New Jersey, devised the first quantum algorithm [3]. Shor's algorithm harnesses the power of quantum superposition to rapidly factor very large numbers (on the order $\sim 10^{200}$ digits and greater) in a matter of seconds, much faster than is possible on conventional computers. With this breakthrough, quantum computing was transformed from a mere academic curiosity into a world interest. There is now a fast growing list of potential quantum tasks such as cryptography, error correcting schemes, quantum teleportation, etc. that show even more desirability of experimental implementations of quantum computing [4]. There is a remarkably long list of physical systems that have been proposed for potential realizations. Several significant experimental examples include: trapped ions [5], cavity QED [6], nuclear magnetic resonance [7], superconducting devices [8, 9, 10, 11, 12]. The Loss-DiVicenzo proposal that would use coupled quantum dot arrays as qubits [13] for a semiconductor-based quantum computer has attracted many researchers in solid-state physics field.

To consider how a practical quantum computer can be built, David DiVincenzo of the IBM Thomas J. Watson Research Center gave a simple list of five requirements: [14]

1. The machine should have a collection of qubits.

2. It should be possible to set all the memory bits to 0 before the start of each computation.

3. The error rate should be sufficiently low.

4. It must be possible to perform elementary logic operations between pairs of bits.

5. Reliable output of the final result should be possible.

To summarize the challenges from the perspective of an engineer, one needs to be able to build a physical system with a collection of well-characterized quantum two-level systems (qubits). Furthermore, the decoherence time of these qubits should be long (compared to the "clock time"), so that the qubits are to a high degree isolated from coupling to the environment so as to not decohere while performing operations on them. Electron spins in silicon are promising because of their long decoherence times, but electrical gating schemes for doable logic operations and measurements of individual qubits still seem challenging.

The Loss-DiVincenzo proposal uses the intrinsic spin of the electrons in coupled quantum dots as the basic carrier of information. Desired operations are effected by the gating of the tunneling barrier between neighboring dots. At this point, devices capable of quantum computing must be constructed so that theory can be put to test. This relies on simultaneous further advances in the experimental techniques of semiconductor nanofabrication, magnetic semiconductor synthesis, single electron electronics, and scanning probe techniques.

At present, quantum computing and quantum communication technology remains in its infancy, especially on the hardware side. However there is a vast amount of versatility as well. Eventually time will tell whether any of these efforts will actually provide a successful route to a quantum computer. Its future undoubtedly lies in the profound effect it will have on the lives of all mankind.

1.3 Thesis Outline

Chapter 2 gives a brief review of the properties of the strained Si/SiGe heterostructures and the means to exploit the strain status in the layers for band engineering.

This chapter also contains details of Si and SiGe epitaxy at Princeton by rapid-thermal CVD (RTCVD).

Chapter 3 is dedicated to two-dimensional electron gas (2DEG) in modulation-doped Si/SiGe heterostructures, which is the physical embodiment of single electrons in quantum dots. Transport properties of electrons and modulation of heterojunction potentials are discussed. A theoretical model is studied to understand the limits on low-temperature electron mobilities.

In chapter 4 we extend our study to parallel 2DEGs in double quantum wells. Such a structure can serve as interaction dimer between two adjacent qubits in a "flying qubit" architecture for quantum computing. For this purpose, we investigate the band structures and the epitaxial growth of double quantum wells.

Chapter 5 presents a thorough review of quantum dot fabrication methods. Various nanolithography and etching methods are critically studied and compared. Examples of successful device applications are given. The expected limitations and benefits of different fabrication options are assessed.

Chapter 6 is focused on Si/SiGe epitaxial regrowth, a novel concept and technique for silicon-based quantum dot surface passivation with ideally zero defects and interface states. A low-temperature cleaning and growth sequence is developed to achieve conformal crystalline passivation over nanopatterned device surface on a wafer scale. This chapter also demonstrates the electrical compatibility of the regrowth technique with the existing 2DEG structures.

The growth, fabrication and epitaxial passivation techniques of Si/SiGe structures are the key to the realization of silicon-based quantum computer architectures. Chapter 7 covers the device aspects of these achievements. Simple quantum device applications including quantum point contact (QPC) and a single quantum dot are presented. We also discuss the possible role of such quantum devices in future quantum computers.

Finally in chapter 8 a summary of the contributions of this thesis is combined with a brief discussion of some possible future directions of research towards quantum computers.

Chapter 2

Si/SiGe Epitaxy

2.1 Introduction

Silicon-based heterostructures have come a long way from the discovery of strain as a new and essential parameter for band structure engineering, to the present state of electron and hole mobilities enhancement which surpass those achieved in the traditional Si/SiO_2 structures. Germanium can be considered as a kind of 'natural' choice for silicon-based heterostructures: the two group-IV elements silicon and germanium crystallize in the same diamond lattice, and form random $Si_{1-x}Ge_x$ alloys of arbitrary composition. By means of these heterostructures, the band structure can be tuned within a wide margin. Table 2.1 lists the most important physical properties of silicon and germanium. In addition, their structural and chemical properties are very similar, which eases epitaxial growth and the application of standard Si CMOS technologies.

The obvious advantages of Si/SiGe heterostructures were recognized at an early stage of research, with the first report on a Si/SiGe superlattice appearing already back in 1975 [15]. After more than 30 years of research and development in this field, SiGe is commonly used as a strain-inducing layer for CMOS transistors in modern

Table 2.1: Selected physical properties of unstrained bulk silicon and germanium at room temperature.

		Silicon	Germanium
Crystal structure		diamond	diamond
Lattice constant (Å)		5.431	5.657
Dielectric constant		11.9	16.2
Direct bandgap (eV)		3.40	0.80
Indirect bandgap (eV)		1.12(Δ)	0.66(L)
Electron mass (m_0)	m_t	0.19	0.08
	m_l	0.91	1.59
Bulk mobility ($cm^2V^{-1}s^{-1}$)	Electrons	1450	3900
(T = 300 K)	Holes	505	1800

technology. Since its introduction at the 90-nm node, strain has become a central performance enhancement element for the standard CMOS flow. With the scaling of the thickness of gate dielectric in silicon CMOS devices, channel mobility in MOSFETs is trending towards lower values due to higher vertical fields [16]. Embedded SiGe source/drain (S/D) was first used in production for 65-nm PMOS. In the 45-nm method, the combined impact of higher Ge fraction in the embedded S/D and the strain enhancement from poly gate removal allow for a 1.5× higher hole mobility compared to 65-nm, despite the scaling of the transistor pitch (contact-poly-contact spacing) from 220 nm to 160 nm.

A key benefit of using SiGe in quantum computing applications comes from the Si/SiGe modulation-doped heterostructures. Modulation-doped structures were first conceived by Dingle in 1978 [17]. In such structures, the active layers consist of an undoped channel for the mobile carriers, an undoped spacer layer that separates the ionized dopants from the channel, and a doping layer. The carriers are confined at the heterojunctions to form a two-dimensional electron/hole gas (2DEG/2DHG). High mobilities are realized in the 2-D gas because the thick spacer layers significantly reduce Coulomb scattering at the ionized impurities of the doping layer. In the spin-qubit scheme for quantum computing we have considered, we are particu-

larly interested in quantum dots created by lateral confinement in a 2DEG. Because individual quantum states are accessible in such quantum dot, we can trap single electrons. The precise control of the electron number is accomplished using the well-documented Coulomb blockade effect.

2.2 The Strained Si/SiGe Heterostructures

2.2.1 Structural Properties

As the lattice constant of germanium is about 4.2% larger than that of silicon, the lattice constant of a bulk SiGe alloy can be estimated by Vegard's rule which uses a linear interpolation of the parameters of the end-point elements of Si and Ge:

$$a(Si_{1-x}Ge_x) = a(Si) + [a(Ge) - a(Si)]x, \tag{2.1}$$

where x represents the fraction of germanium atoms.

Let's first consider the case that a layer of pure silicon is deposited on top of bulk SiGe alloys. When the silicon film is thin, the in-plane silicon lattice tries to stretch and line up with the SiGe. The thin pseudomorphic (meaning that lattice mismatch is accommodated by strain in the thin film on a lattice-mismatched substrate) silicon becomes tensilely "strained". Fig. 2.1 illustrates the formation of such strained thin films.

The thin films cannot relax, because the elastic energy stored in such a homogeneously strained layer is lower than the elastic energy associated with the local distortion around a misfit dislocation. Also as a result of the strain, the perpendicular lattice constant of the silicon, $a_{i\perp}$, will decrease:

$$a_{i\perp} = a_i \left[1 - D^i \left(\frac{a_{i\parallel}}{a_i} - 1\right)\right], \tag{2.2}$$

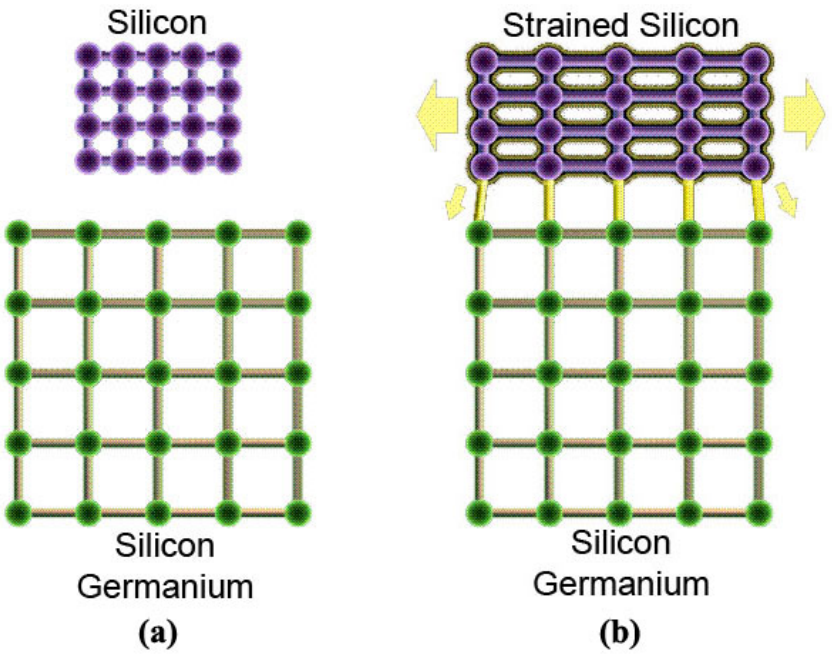


Figure 2.1: Schematic lattice structure of thin silicon deposited on silicon germanium substrate: (a) the SiGe lattice constant is larger compared to that of bulk Si; (b) the pure Si lattice attempts to line up with the SiGe lattice, which causes the Si to become tensilely strained. (Image courtesy of IBM, www.ibm.com)

where a_i denotes the cubic (unstrained) lattice constant of the film, and D^i is a constant that depends only on the elastic constant c^i_{11} and c^i_{12} of the respective material (in the above case, silicon):

$$D^i_{(001)} = 2\left(\frac{c_{12}}{c_{11}}\right). \tag{2.3}$$

So far we have discussed in detail the heterostructures of stained Si on SiGe. The argument for thin pseudomorphic SiGe layers deposited on Si bulk is very similar, except for that SiGe layers are under compressive strained to maintain pseudomorphic bonding with the Si substrate.

It has been shown in Fig. 2.1 that in order to exploit strained silicon, the strain-defining SiGe substrate has to be realized. Bulk SiGe can be ruled out, both because of the growth problems of pulling homogeneous SiGe crystals, and because such substrates would jeopardize the Si/SiGe system's compatibility with existing silicon tech-

nologies. It is necessary to employ silicon substrates and grow a relaxed, intermediate SiGe buffer layer.

For relaxed buffers as well as for pseudomorphic layers the most relevant material parameter is the critical thickness t_c [18], an equilibrium parameter at which strain relaxation by the generation of misfit dislocations can commence. When the strained film thickness exceeds t_c, misfit dislocations become energetically favorable, and provide partial strain relaxation of the film. By using low-temperature epitaxy techniques, such as molecular beam epitaxy (MBE) or chemical vapor deposition (CVD), one can also grow pseudomorphic SiGe films above the equilibrium critical thickness on bulk Si. This is because a metastable range exists in which the nucleation and propagation of misfit dislocations is kinetically suppressed. Fig. 2.2 shows the three regimes labeled 'stable', 'metastable' and 'relaxed' as a function of Ge fraction x [19].

However, as there are many nucleation sites from the threading dislocations in a relaxed "virtual" substrate, in practice there is little metastable critical thickness for heterostructures grown on such substrates, such as tensilely strained silicon on relaxed SiGe buffers on a silicon substrate.

2.2.2 Band Alignment

For the very large-scale integration (VLSI) community, the whole point of growing heterostructures is the opportunity to manipulate the behavior of carriers through band engineering. The bands of Si and SiGe alloys are strongly affected by strain, and experimental data are available both for unstrained bulk SiGe alloys and for pseudomorphic compressively strained SiGe films on Si(100) substrates. The strain-induced heavy-hole/light-hole splitting also leads to a splitting of the valence band in strained SiGe. Fig. 2.3 shows the bandgap values against Ge fraction x [20].

This thesis is focused on strained Si on SiGe relaxed buffer heterostructures. The

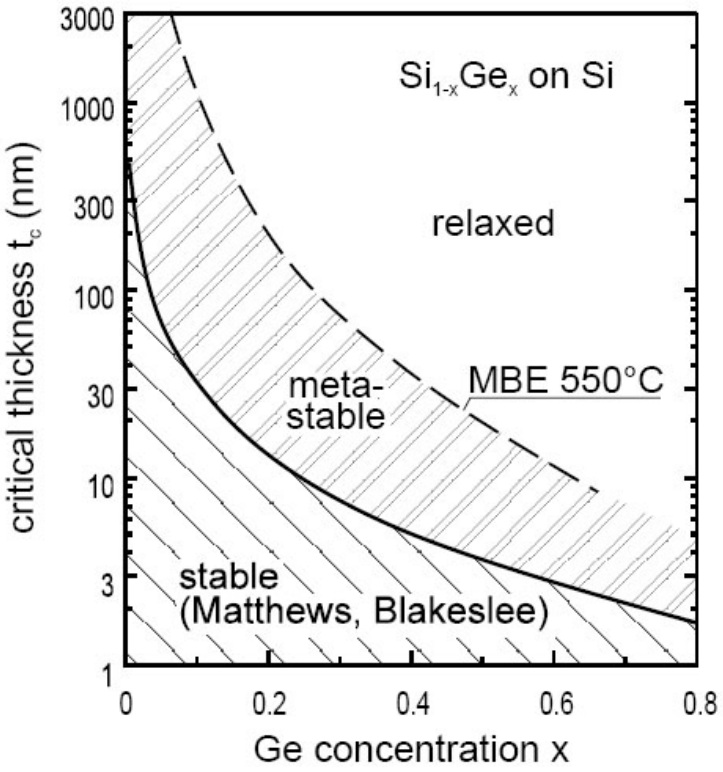


Figure 2.2: [19] Critical thickness against fraction for $Si_1 - xGe_x$ on Si. The lowest curve gives the theoretical limit in thermal equilibrium, whereas the experimental curve is for a metastable layer grown at 550 °C by MBE.

pseudomorphic Si/SiGe interface is commonly used as a quantum well to confine electrons. Such $Si/Si_{1-xs}Ge_{xs}$ heterojunctions are of type II for all value of x_s. Fig. 2.4 illustrates the valley splitting and allows predictions for arbitrary Si/SiGe heterojunctions with respect to band ordering and band offsets [19]. Throughout this thesis we will discuss the $Si/Si_{0.7}Ge_{0.3}$ system unless a different x_s is specified. A complete description of the band alignment can be calculated based on the local density functional and *ab initio* pseudopotentials [22]. In summary, the hydrostatic strain component leads to an overall downward shift of the average valence band and lowers the Δ and L band energies. The uniaxial strain component only splits the Δ conduction bands and the degenerate light/heavy hole valence band edges and leaves the weighted average positions of these bands unaffected. For the conduction band,

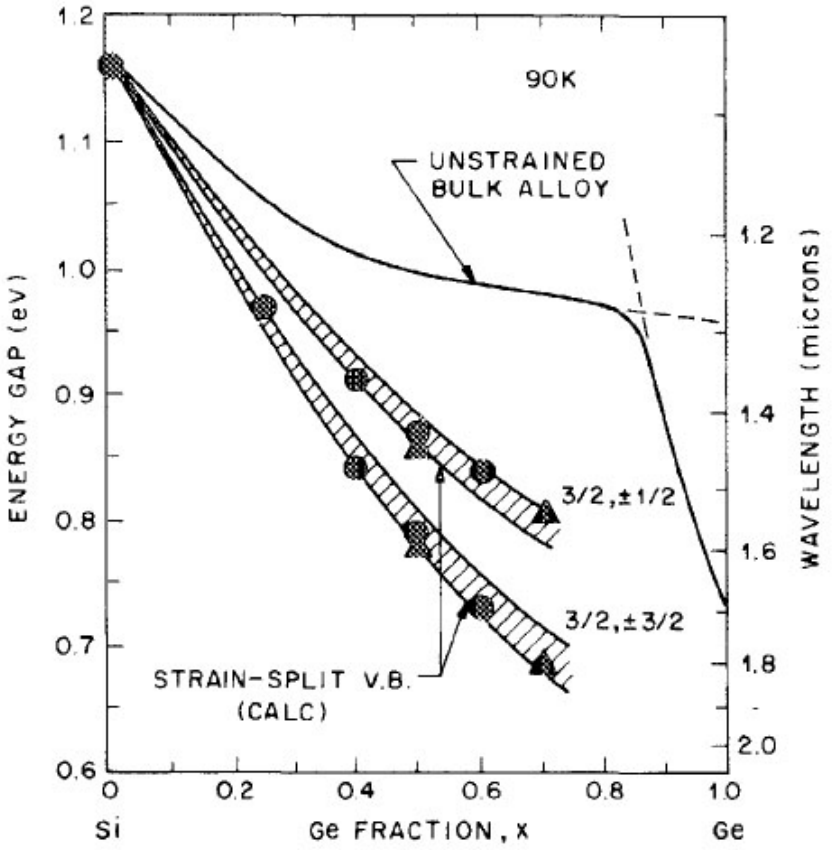


Figure 2.3: [20] Summary of energy-gap values of SiGe alloys, both unstrained bulk and strained SiGe on Si(100) substrate, at 90 K after correcting for quantum well shifts (circles = 75Å wells; triangles = 33Å wells). The double points at the same values of x correspond to a splitting of the valence band. The unstrained bulk alloy data are from optical absorption measurement by Braunstein [21].

the six-fold valley degeneracy in bulk silicon is lifted. The overall lowest conduction band is always the Δ_2 level in the active Si layer. Analytical fittings for the band offsets that will be used for numerical simulations can be expressed as [23]

$$\Delta E_v(x_s) = -0.238x_s + 0.03x_s^2, \tag{2.4}$$

$$\Delta E_c(x_s) = -0.35x_s - 0.35x_s^2 + 0.12x_s^3, \tag{2.5}$$

where $x_s < 0.85$, the negative signs indicate that the conduction and valence bands of strained Si are lower than those of the relaxed $Si_{1-x_s}Ge_{x_s}$ substrate.

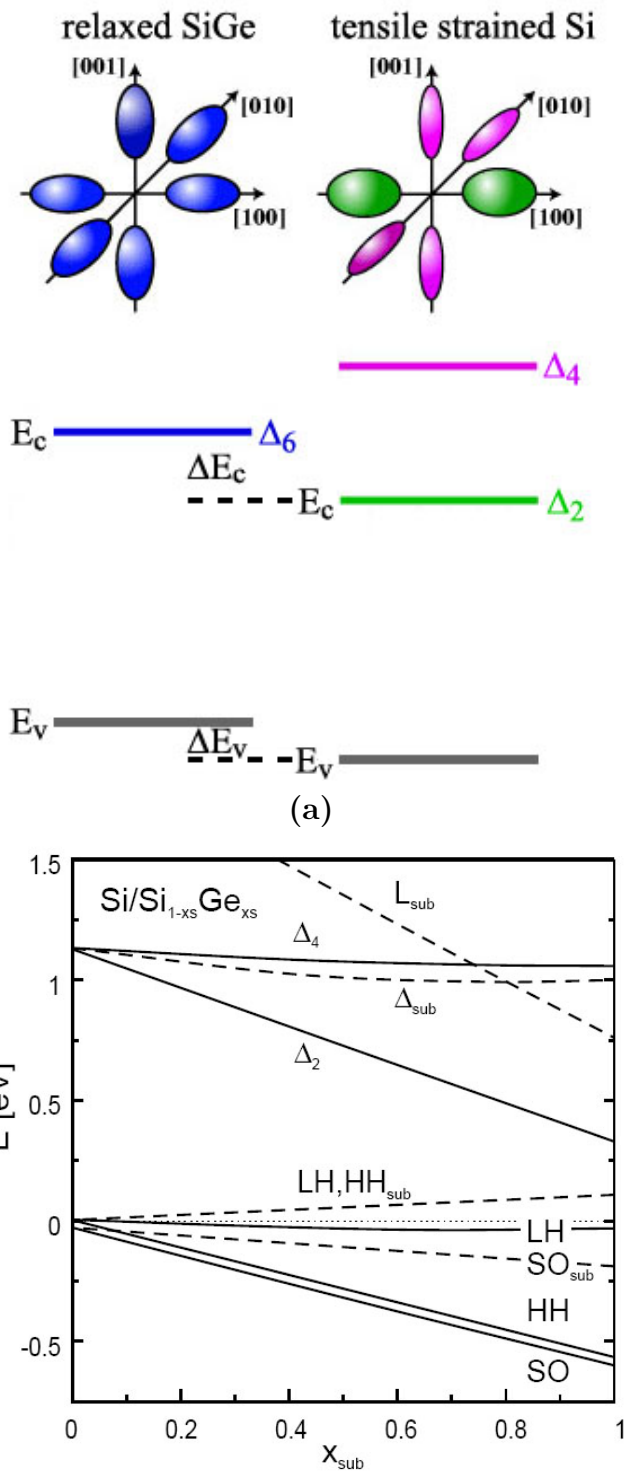


Figure 2.4: (a) The splitting of Si conduction bands in tensilely strained Si/SiGe heterostructures. (b) [19] Variation of the relevant silicon conduction and valence bands of a tensilely strained Si/SiGe heterostructure as a function of relaxed SiGe substrate composition x_{sub}.

The strain-induced band alignment also has strong effects on electron transport in strained silicon. The high electron mobilities realized in Si/SiGe heterostructures are of great interest for application in high performance CMOS as well as for quantum computation. The mechanism of mobility enhancement is well understood. For tensilely strained Si on SiGe substrate, the conduction band minimum lies in the silicon Δ_2. At low temperatures, the electrons only populate in the lower minima. The in-plane effective mass is now reduced to the transverse effective mass, which is only

$$m^* = m_T = 0.19\ m_0. \tag{2.6}$$

Besides the lower in-plane effective mass, the lifting of degeneracy also helps suppression of intervalley scattering. The enhanced electron mobilities and as a result, enhanced mean free paths in these structures have made a variety of transport physics experiments possible. One prominent example is the observation of the fractional quantum hall effect (FQHE) in an n-type Si/SiGe heterostructure [24]. To date, the highest low-temperature electron Hall mobility ever reported in strained Si is around 8.0×10^5 cm^2/Vs [25]. This has approached those in the GaAs/AlGaAs system to within a factor of 50. At room temperature, however, phonon scattering dominates and generally muffles the mobility. Still a 2DEG enhances the mobility by almost a factor of two over that of pure bulk silicon (2600 vs. 1450 cm^2/Vs) [26].

2.3 Si and SiGe Epitaxy at Princeton

2.3.1 Overview of the RTCVD Epitaxy

The Si/SiGe epitaxy for this thesis was performed in a custom-built rapid thermal chemical vapor deposition (RTCVD) apparatus at Princeton [27]. The reactor includes a load-locked, cold-wall quartz tube. A 100-mm silicon wafer is loaded and

supported by a quartz stand. It is heated from underneath by a bank of twelve 6-kW tungsten-halogen lamps. The process gas flows are adjusted by mass flow controllers. Three silicon precursors are available: dichlorosilane (or DCS, SiH_2Cl_2), silane (SiH_4, 10% in argon mixture), disilane (Si_2H_6, 10% in hygrogen mixture). Germane (GeH_4, 0.8% in hydrogen mixture) is used as the germanium precursor. Diborane (B_2H_6, 20 ppm diluted in hydrogen) and phosphine (PH_3, 100 ppm diluted in hydrogen) are added for *in situ* doping in both Si and SiGe growth. Unreacted exhaust gases are handled by a burnbox/scrubber equipment. The burnbox operates at around 850 °C to assure a thorough oxidation of the effluent. The hot treated gases are passed through a water recirculation tank for cooling and removal of residual reactor gases and particles.

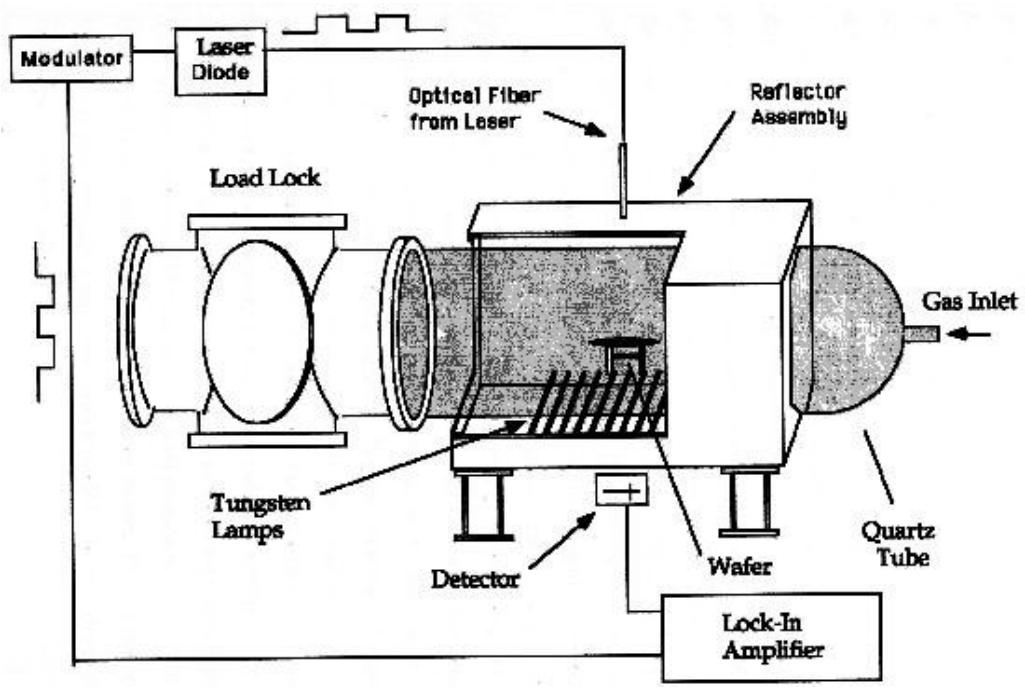


Figure 2.5: Schematic of Princeton RTCVD system used in this thesis. (Image courtesy of P. V. Schwartz [28])

Typical epitaxial growth conditions are at a pressure of 6 Torr with 3 standard liters per minute (slpm) hydrogen carrier flow. Under these conditions the growth surface is hydrogen-terminated. In this susceptor-free reactor, the silicon temperature

is measured by infrared absorption [29]. Two semiconductor lasers at 1.30 and 1.55 μm are coupled into a common fiber. The transmission is measured using lock-in amplifier techniques. A feedback loop controls the lamp power for accurate temperature control. The RTCVD system has been shown capable of growing high quality Si/SiGe layers on a 100 Å scale with an interface abruptness on the order of 10 Å, which is essential for quantum computing applications. Next we will discuss the Si/SiGe epitaxial RTCVD growth in more details, as well as to learn the prospects and limitations of this system.

2.3.2 The Use of Commercially-available SiGe Relaxed Buffers

We obtained our SiGe relaxed buffer from AmberWave Systems (see also www. amberwave.com), one of the semiconductor industry's leading suppliers of strained silicon technology. From the perspective of epitaxial growth, the growth conditions of relaxed buffers of a few microns thick and the thin modulation-doped layers can be quite different. High temperatures typically above 1000 °C are desirable for relaxed buffer growth to enable simultaneous improvements in both dislocation density and growth rate. The growth optimization is focused on high throughput on a large wafer scale. In contrast, optimization for the growth of high-mobility heterostrucures often leads to a contrary requirement. The layers are usually grown at low temperatures ($\sim$ 550 - 750 °C) for precise control of the thin layer thickness and interface abruptness. The typical sample dimension is around 1 cm for magneto-transport experiments at liquid helium temperatures. Therefore, it is difficult for a single system to grow both SiGe relaxed buffers and the modulation-doped heterostructures. We are among the first to use commercially available SiGe relaxed buffers for Si/SiGe modulation-doped heterostructures in academic research. The suitability of such applications is demonstrated.

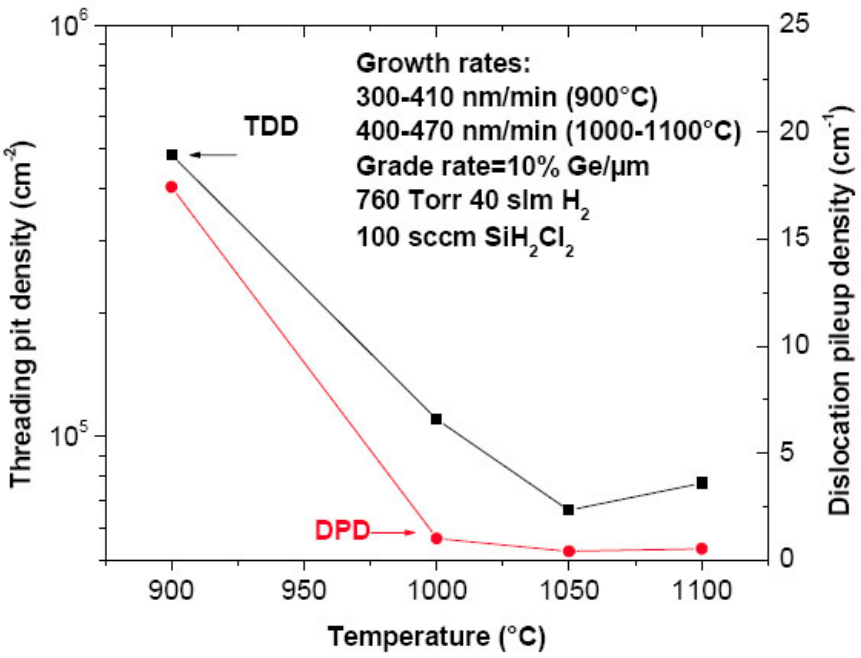


Figure 2.6: [30] Effect of temperature on AmberWave graded buffer threading dislocation density (TDD) and dislocation pileup density (DPD), determined by etch pit density and plan view TEM, respectively.

AmberWave Systems has developed a novel, high quality SiGe graded buffer growth process using $GeCl_4$ [30]. The use of the new germanium precursor enabled previously unattainable growth temperatures and growth rates. The chlorine component also can reduce parasitic deposition on the reactor chamber walls. Fig. 2.6 shows the effect of temperature in their system while maintaining high growth rates. Normally their growth procedure is as follows:

1. Start with 200-mm silicon substrates, either heavily or lightly doped depending on the applications;

2. Grow an undoped linearly-graded SiGe buffer at 10% germanium per micron;

3. Grow an undoped SiGe cap layer at the final Ge content, approximately 2 μm thick;

4. (optional) Chemical mechanical polishing (CMP) of the surface, to remove cross-

hatch roughness.

In this work three kinds of SiGe relaxed buffers from AmberWave Systems were used. Table 2.2 summarizes the parameters of these buffers. The use of CMP to eliminate cross-hatch patterns on relaxed SiGe buffers is illustrated in Fig. 2.7. The polished surface has a roughness RMS of 5.7 Å which is about ten times smoother than the as-grown surface. However the surface roughness has nearly no measurable effect on the quality of quantum wells growth on top, the electrical quality of quantum well samples grown on polished and unpolished buffers from the same growth were identical.

Table 2.2: Summary of AmberWave Systems SiGe relaxed buffers.

Label	AW2L	AW3H	AW3L
Substrate doping	(p-type) lightly	(n-type) heavily	(p-type) lightly
Ge content	20%	30%	30%
Total buffer thickness (μm)	4	5	5
Surface polishing	CMP	CMP	none

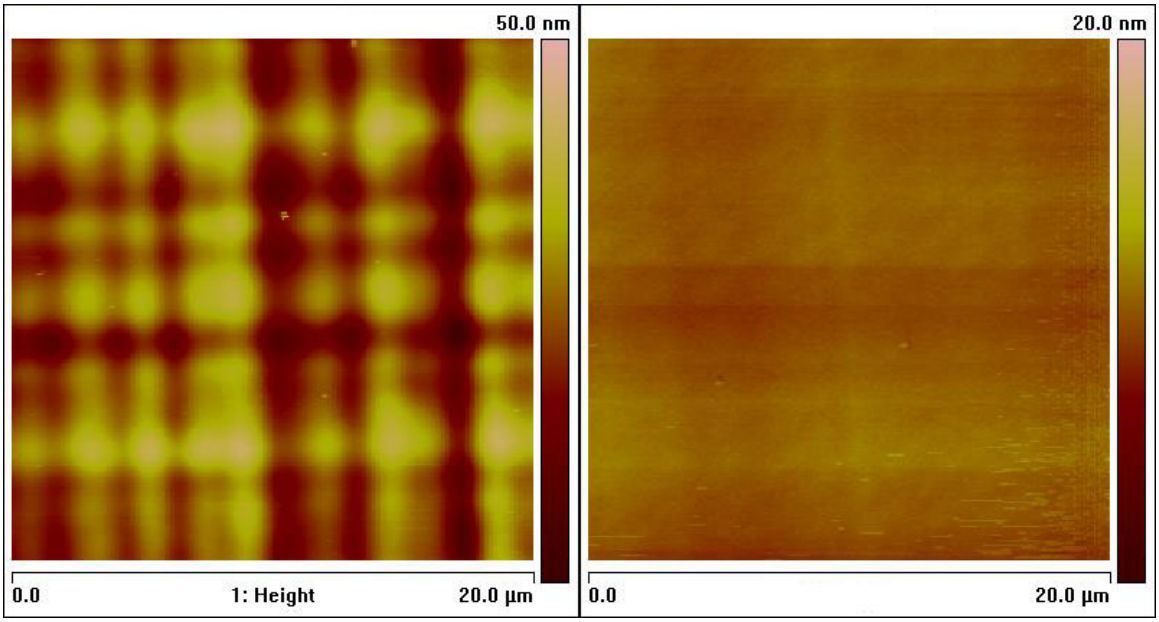


Figure 2.7: Top-view AFM images of: (left) AW3L SiGe relaxed buffers with cross-hatch patterns, surface RMS = 7.05 nm; (right) AW3H SiGe relaxed buffers after polishing, surface RMS = 0.57nm.

Since the Princeton RTCVD system is designed for 100-mm wafers, the 200-mm wafers were first diced into 1×1 cm squares using a Kulicke & Soffa wafer dicing saw (model 982-6) so they can be loaded with support of a 100-mm carrier wafer. The special carrier wafer has 5 etch-defined recessed holes to fit the small samples, as shown in Fig. 2.8.

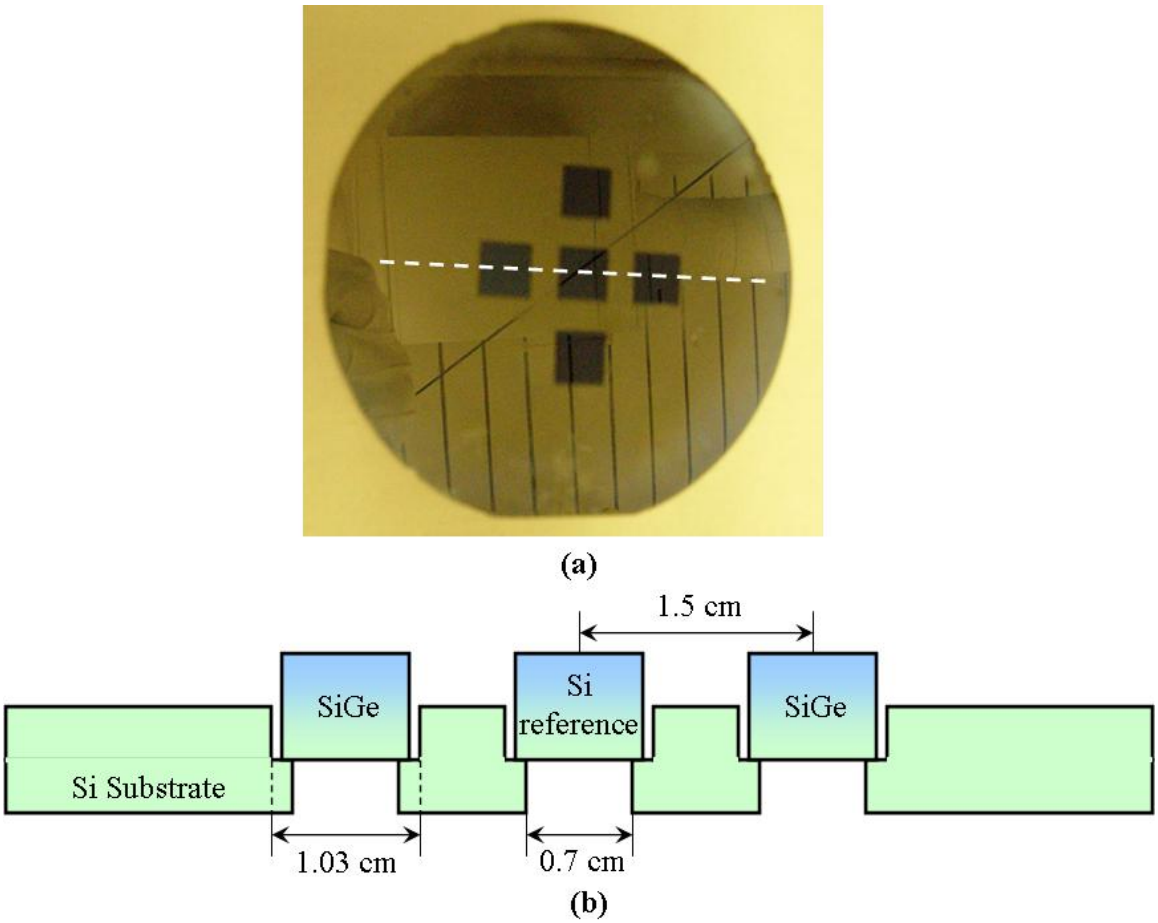


Figure 2.8: (a) A picture of 5 1×1 cm square pieces loaded on a 100-mm carrier wafer used for RTCVD growth. (b) A schematic view of cross section along the dashed line in (a) showing the dimensions of recessed holes.

2.3.3 Infrared Absorption of Si and SiGe

Since in our CVD the growth temperature is inferred by measuring the transmission of infrared through the center of a 100-mm wafer, the effects of the heavily doped

substrate as well as SiGe buffers have to be evaluated first.

For any silicon wafer with known thickness d and doping level n (or p), the system utilizes a single variable, normalized transmission (denoted by $t(T)$), to measure the temperature. Ignoring any change with temperature in the fractional power transmitted at the air-silicon interface [31], the normalized transmission will depend on the wafer thickness and material absorption coefficient:

$$t(T) = e^{-(\alpha(T)-\alpha(NT))d}, \tag{2.7}$$

where NT stands for normalization temperature, which is taken as room temperature. Sturm et al. presented analytical expressions for near-infrared absorption in silicon [29]. The absorption proceeds predominantly by two process: valence band to conduction band transitions and by free carrier absorption.

$$\alpha(T) = \alpha_{BG}(T) + \alpha_{FC}(T). \tag{2.8}$$

Here we only give the final results for the sake of simplicity. For the bandgap absorption

$$\alpha_{BG}(h\nu, T) = \sum_{i=1}^{2}\sum_{j=1}^{2}(-1)^j \frac{\alpha_i \left[h\nu - E_g(T) + (-1)^j k\theta_i\right]}{exp\left[(-1)^j\theta_i/T\right] - 1}\ cm^{-1}, \tag{2.9}$$

$\alpha_1(E)$ and $\alpha_2(E)$ represent absorption from the transverse acoustic and optical phonons, respectively.

$$\begin{aligned}
\alpha_1(E) &= 0.504\sqrt{E} + 392(E-0.0055)^2, E \geq 0.0055 \\
&= 0.504\sqrt{E}, 0 \leq E < 0.0055 \\
&= 0, E < 0, \\
\alpha_2(E) &= 18.08\sqrt{E} + 5760(E-0.0055)^2, E \geq 0.0055
\end{aligned} \tag{2.10}$$

$$= 18.08\sqrt{E}, 0 \leq E < 0.0055$$
$$= 0, E < 0, \tag{2.11}$$

where α is in units of cm^{-1} and E is in electronvolts. The temperature dependence of the silicon bandgap is

$$E_g(T) = E_g^0 - \frac{4.73 \times 10^{-4} T^2}{635 + T} \ eV. \tag{2.12}$$

The second mode, free carrier absorption coefficient can be calculated as

$$\alpha_{FC}(T) = n(T)\sigma_n(T) + p(T)\sigma_p(T), \tag{2.13}$$

where the two cross sections are given by

$$\sigma_n(T) = 1.01 \times 10^{-12} T\lambda^2 \ K^{-1}, \tag{2.14}$$
$$\sigma_p(T) = 0.51 \times 10^{-12} T\lambda^2 \ K^{-1}. \tag{2.15}$$

The electron and hole concentrations n and p depend on n_i in silicon according to the relationship

$$\sqrt{np} = n_i = 3.87 \times 10^{16} T^{3/2} exp\left(-(0.605 - 7.1 \times 10^{-10}\sqrt{n_i/T})/kT\right) \ cm^{-3}. \tag{2.16}$$

Two lasers with wavelengths of 1.30 and 1.55 μm are used in temperature range from 500 to 800 °C. It has been found that in lightly doped silicon, nearly all of the absorption at 1.30 μm proceeds by a band-to-band process due to bandgap narrowing at these temperatures ($\alpha_{BG}(T) \gg \alpha_{FC}(T)$), while at 1.55 μm free carrier absorption dominates ($\alpha_{BG}(T) \ll \alpha_{FC}(T)$). In practice, for standard 100-mm silicon wafers with

light substrate doping, we monitor 1.30 μm transmission for temperatures up to 650 °C then switch to 1.55 μm for up to 800 °C. Fig. 2.9 shows the original published data of normalized transmission over the temperature range. The slopes of the curves in their useful range (for example, 1.30 μm at 600 °C and 1.55 μm at 700 °C) are both around 3%/°C. This means if we assume a conservative estimate of error in transmission measurement to be $\sim \pm 10\%$, the temperature error will be $\sim \pm 3$ °C.

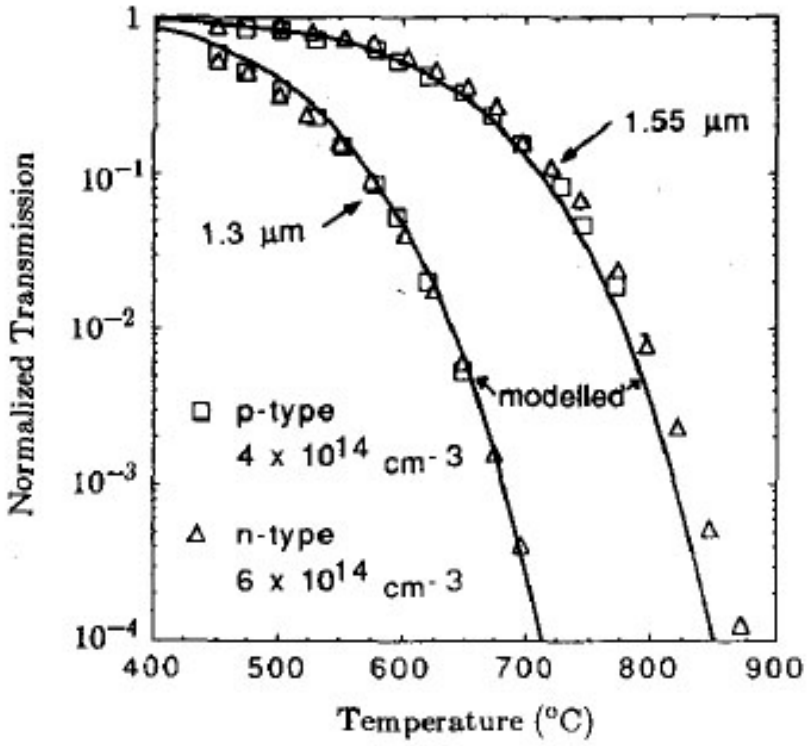


Figure 2.9: [29] Data of normalized transmission vs. temperature for 1.30 and 1.55 μm, for lightly doped <100> n-type (7.5 Ω·cm, thickness = 513 μm) and p-type (37 Ω·cm, thickness = 493 μm). The data have been adjusted to reflect a 500-μm thickness. For comparison, also presented are the model results for the n-type wafer.

There are least two potential problems caused by the use of AmberWave Systems substrates in our temperature measurement. First, the 200-mm starting silicon wafers are 725 μm thick, 50% more than the standard 100-mm wafers. Also the SiGe relaxed buffers cause extra absorption. To extend the usefulness of our existing normalized transmission models, we modify it to reflect the above changes. In particular, the

following rather simplified assumptions are made to incorporate the effect of SiGe layers:

1. The only different parameter when applying the above calculations of infrared transmission to SiGe is the reduced bandgap. All other effects such as the band splitting and change in the phonon-assisted bandgap transitions due to a random alloy are ignored. The reduction of $Si_{1-x}Ge_x$ bulk alloy bandgap is obtained as [32]

$$\Delta E_g = E_{Si} - E_{SiGe} = 0.43x - 0.206x^2 \ eV. \tag{2.17}$$

2. The linear graded SiGe buffer is treated approximately as a single-step relaxed layer with its final Ge content and half of its real thickness. As a result, a SiGe relaxed buffer consisting of a linear graded buffer of thickness d_{graded} and a uniform cap layer of thickness d_{cap} will have an "effective" thickness of

$$d_{SiGe} = d_{graded}/2 + d_{cap}. \tag{2.18}$$

3. We also ignore the power reflected at the Si/SiGe interface, since the two materials are very close to each other in nature and the Ge content change is gradual. In other words, the absorptions in Si and in SiGe are additive, the total normalized transmission is:

$$t(T) = e^{-(\alpha_{Si}(T) - \alpha(NT)_{Si})d_{Si}} e^{-(\alpha_{SiGe}(T) - \alpha_{SiGe}(NT))d_{SiGe}}. \tag{2.19}$$

Under these assumptions the normalized transmission of AmberWave Systems buffers is calculated. As an example, Fig. 2.10 shows the model for a 725 μm Si substrate plus a total of 3 (graded) + 2 (cap) μm $Si_{0.7}Ge_{0.3}$ buffer, so the effective SiGe

layer thickness used is 3.5 μm. The dotted line shows the model for the starting Si substrate only. The substrate doping was chosen to be 1×10^{15} cm^{-3} p-type. One finds out that overall the effect of the SiGe buffer is about 10% reduction in transmission at 1.30 μm and 5% reduction at 1.55 μm. The difference can be explained by noting that the reduced bandgap will have a stronger impact on band-to-band absorption, which is a more dominant mechanism at 1.30 μm.

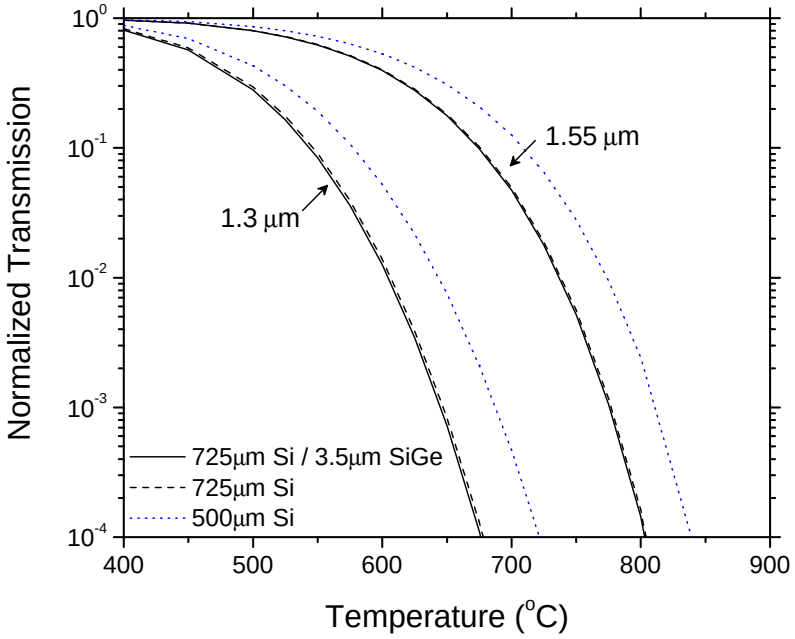


Figure 2.10: Model of normalized transmission vs. temperature for 1.30 and 1.55 μm, for lightly doped <100> p-type (1×10^{15} cm^{-3}, thickness=725 μm) plus a $Si_{0.7}Ge_{0.3}$ buffer (thickness = 3.5 μm). Also presented are the model results for a 500-μm thick silicon.

The slope of the 1.30 μm curve at 600 °C is now steeper, $\sim$ 4.5%/°C. This is better for our temperature control, as now we can achieve $\pm$2°C accuracy with 10% measured signal variation. However, this change in slope comes at a cost: the actual received signal is also about 75% weaker than that previously from the 100-mm Si wafer. The upper temperature limit with the 1.30 μm is around 650 °C. Measuring higher

temperature is difficult due to the weak transmission, which is subject to large error bars caused by electrical noise. Alternatively, we can switch to 1.55 μm transmission at these temperatures. The slope is about 1.5%/°C indicating an estimate of ±6°C error. For the 1.55 μm in the temperature range 700 - 750 °C, both the slope and the actual signal strength remain at a reasonable level. We can still achieve $\sim$ 3%/°C accurary with strong received signals.

So far we have only considered substrates with light doping (10^{15} cm^{-3}). In such cases Fig. 2.10 can be referred to find the desired normalized transmission set points. Physically, the moderate and heavily doped cases are expected to be very different because of the significant free-carrier absorption even at room temperature. The calculation shows that a heavily doped substrate indeed does have a very low normalized transmission at elevated temperatures. We decide the best practice to circumvent such difficulties is to load a regular lightly-doped Si reference piece in the center of a carrier wafer, while placing other samples around the outside of the carrier wafer. Empirical data shows that the temperature nonuniformity within 2 inches from the center of the carrier wafer is less than 5 °C.

For all growth on AW relaxed buffers described in this thesis, the thick Si/SiGe heterostructure samples were placed on a recess hole that is 1.5 cm away from the center, while a 500-μm thick silicon sample was placed in the center for temperature control, as previously shown in Fig. 2.8. The growth on four outside pieces on the perimeter is uniform. This method gives a repeatable temperature so that certain growth conditions may be reproduced.

2.3.4 Growth Rates and Doping Profiles

The successful epitaxy of Si/SiGe heterostructures, especially the structures designed for quantum computing applications, rely on precise knowledge of growth rates and doping profiles. Various historical data are available for our RTCVD reactor, yet

none are based on SiGe relaxed buffers. We performed calibrations with a series of carefully designed growth sequences and their secondary ion mass spectroscopy (SIMS) analysis. All SIMS analysis presented in this thesis were prepared by Evans Analytical Group at Hightstown, New Jersey.

The Si/SiGe epitaxy is performed at temperatures between 550 and 700 °C. A hydrogen background (3 slpm flow at 6 Torr) is used. DCS is the preferred silicon precursor, as the deposition is more selective and hence reduces the parasitic coating of reactant byproducts on the reactor walls. However, we also find that disilane growth at lower temperature can achieve similar growth rates with lower phosphorus background impurities. So data using disilane as precursor are also measured. Fig. 2.11 summarizes the calibration results for SiGe layers growth using various combinations of gas mixtures. From the growth calibration data, for example, one should use a gas mixture of 26 sccm DCS / 1.8 sccm GeH_4 at 625 °C or 25 sccm Si_2H_6 / 4 sccm GeH_4 at 575 °C to grow $Si_{0.7}Ge_{0.3}$ films.

Another critical control parameter for successful heterostructure growth is the doping level in doped layers. For n-type modulation-doped Si/SiGe heterostructures, we are particularly interested in phosphorus doping profiles in SiGe layers, either as intentional dopants or background impurities.

Fig. 2.12 shows the phosphorus doping levels obtained in $Si_{0.7}Ge_{0.3}$ films by *in situ* PH_3 doping. By comparing the two silicon precursors, we find that the phosphorus incorporation is in general higher for a given phosphine flow in SiGe layers grown with DCS than with disilane. This might also contribute to the higher background impurity level seen in DCS growth. With a DCS precursor it is very difficult to achieve *in situ* doping levels below 10^{19} cm^{-3}. Note however the phosphorus doping level does not attain its steady state value immediately when the phosphine is switched on, a typical transient region of a few nanometers was observed in historical SIMS profiles. Thus in the thin supply layer of a few nanometers SiGe, the doping level may be

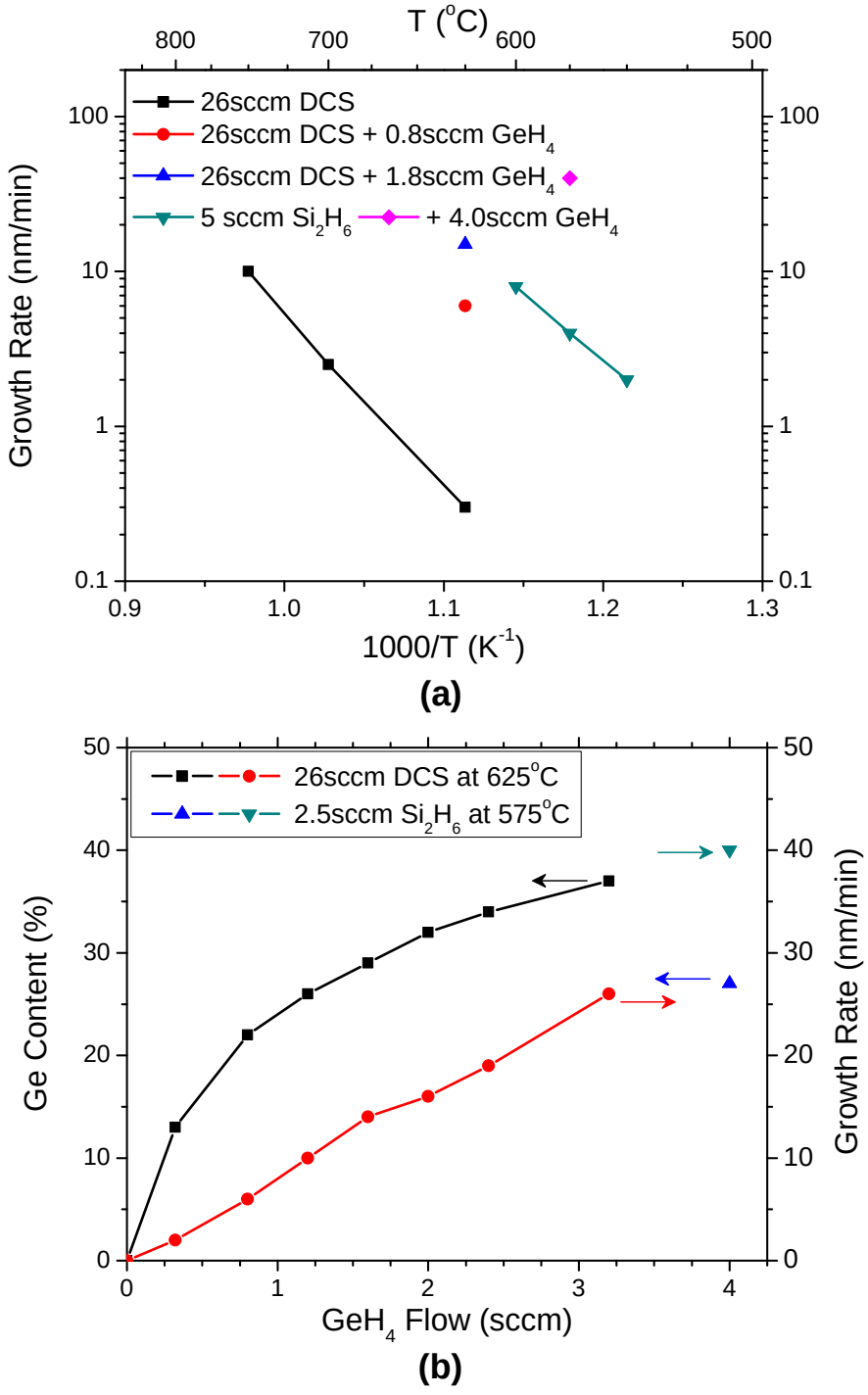


Figure 2.11: Growth rate and Ge content of SiGe layers using DCS and disilane at different temperatures and gas flow rates.

lower than the steady state value from the figure.

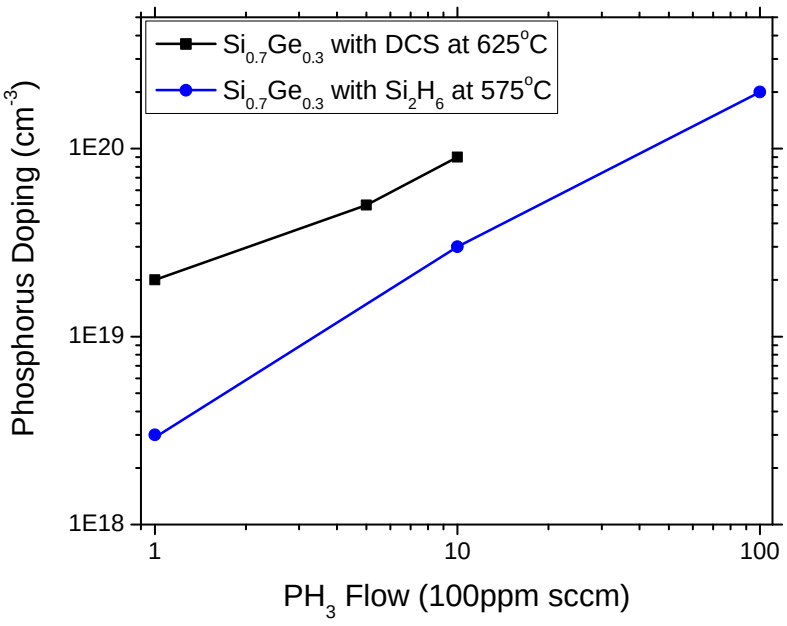


Figure 2.12: N-type doping level in $Si_{0.7}Ge_{0.3}$ vs. phosphine flow (100 ppm in hydrogen) layer grown at two different conditions.

2.4 Summary

Lattice-mismatched Si/SiGe heterostructures can form pseudomorphic layers under a certain temperature-dependent critical thickness. The effects of strain on both the band structure and the band offsets have been reviewed. Band engineering through the strain adjustment has spearheaded both silicon device applications and understanding in mesoscopic physics. In particlar, we are concerned with the tensilely strained silicon on SiGe relaxed buffers for their usefulness in confining electrons. To explore these opportunities, epitaxial silicon and silicon-germanium layers are grown by RTCVD at Princeton. High quality commercially available SiGe relaxed buffers are integrated in our experiments for the growth of thin heterostructure layers. General

growth issues such as infrared absorption for accurate temperature control, calibration of growth rates and doping profiles have been addressed. The rest of this thesis will be dedicated to the growth and applications of Si/SiGe heterostructures.

Chapter 3

The Two-dimensional Electron Gas in Strained Silicon

3.1 Introduction

The two-dimensional electron gas (2DEG), formed by employing modulation-doped Si/SiGe heterostructures, is a very important low-dimensional system for electronic transport. It is the core of a field-effect transistor, which goes by many acronyms including modulation-doped field-effect transistor (MODFET) and high electron mobility transistor (HEMT). The silicon metal-oxide-semiconductor field-effect transistor (MOSFET) is perhaps the most common electronic device, with holes or electrons trapped in an inversion layer at the Si/SiO_2 interface. Since the first observation of the modulation doping effect in Si/SiGe grown by MBE [33], considerable research involving 2DEG has been done, and much continues to this day. The 2DEG offers a mature system of potentially high mobility electrons, especially at low temperatures. These enormous mobilities offer a test bed for exploring fundamental physics, as well as a single figure of merit for the overall growth quality.

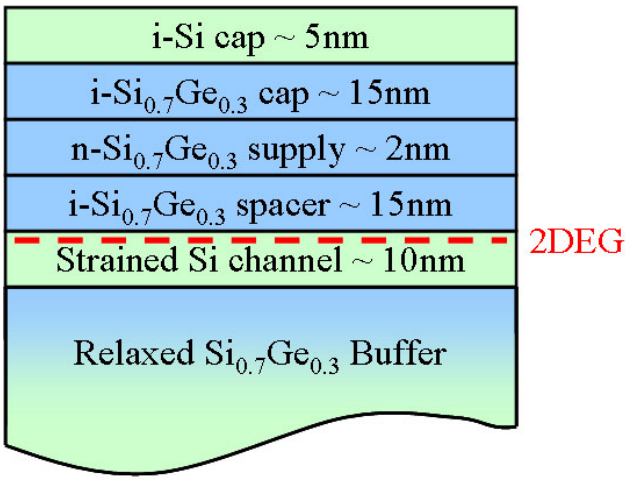
Fig. 3.1 shows the structure for a typical 2DEG in strained Si/SiGe and the

associated band diagram. It has the following layers, starting from the substrate and going up as the direction of growth:

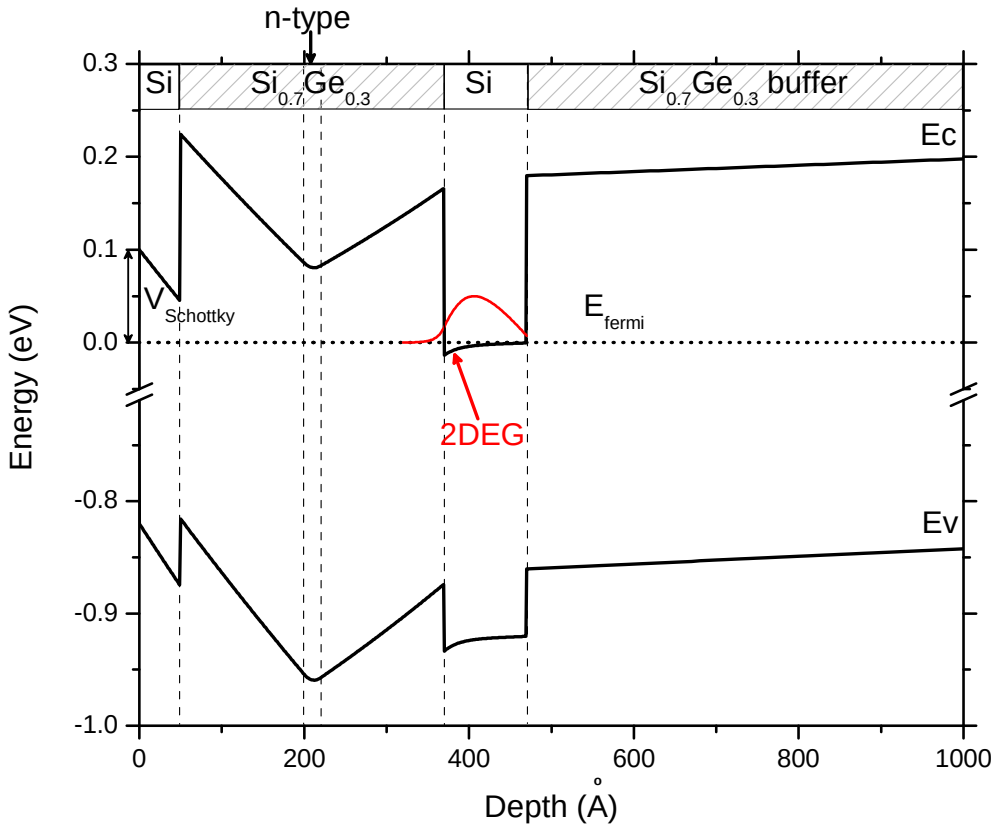
1. Relaxed SiGe buffer layer, to induce tensile strain in silicon;
2. Strained Si channel for the electrons, undoped;
3. SiGe spacer of thickness s, undoped, to separate the ionized dopants from the channel;
4. SiGe doped layer of thickness d and doping N_D (heavily n-type), possibly a monolayer in δ-doped material;
5. SiGe and a very thin Si cap. A metal gate may be deposited on top, which is used to tune the potential of the quantum well.

In the band diagram, we assumed a doping level of 5×10^{18} cm^{-3} in the supply layer. Other materials parameters and calculation procedures can be found in Appendix B and in [23]. Ideally the doping level and surface potential were designed such that the lowest subband in the doping level is located above the Fermi level. Therefore at low temperature, free electrons exist only in the channel, and occupy only the lowest subband lying above the Δ_2 level. For reasons of clarity, only the Δ_2 bands in silicon are plotted. Another important parameter in the band structure is the surface potential $V_{Schottky}$, which will be sensitive to the top surface states/defects. This is not a problem in top-gated structures, in which the surface potential can be tuned continuously.

The one hurdle that has been severely impeding the enhancement of mobilities in strained silicon 2DEG's is the availability of high quality buffer layers. Fig. 3.2 shows the evolution of published Hall mobilities from various publications [25]. Relaxed SiGe buffer layers on Si substrates (also referred to as *virtual substrates*) are relatively thick, since a high degree of relaxation and low defect densities are required.



(a)



(b)

Figure 3.1: (a) A typical structure of modulation-doped layers on a relaxed SiGe buffer layer. (b) The band diagram shows a type-II band alignment with the electrons confined in the tensilely strained Si channel. The surface potential is assumed so that $V_{Schottky} = -0.1$ V. The electron wave function is plotted in red (in arbitrary units).

In the first few years of SiGe buffer layers growth people used a single-step technique, which consists of growing a constant-composition SiGe layer with a thickness far exceeding the critical thickness [41]. Such buffer layers are associated with very high threading dislocations penetrating throughout the growth. The graded buffer technique has been developed to overcome the problems. It employs a linear Ge gradient throughout initial buffers, followed by a final layer with constant Ge composition. The graded buffers have led to a significant enhancement of the mobilities. Further improvements of the relaxed buffer layers aiming towards device applications have been made over time. In the past few years, with progress in chemical mechanical polishing (CMP) [42] and high temperature growth process, atomically flat relaxed buffers with 10^5 cm^{-2} threading dislocations became commercially available [30]. Efforts will continue for optimization of graded buffers both with respect to relaxation and surface morphology.

Before we move to the experimental results, I would like to emphasize the important role of 2DEG in quantum computing. In the Loss-DiVicenzo proposal [14], free electrons are used as a vehicle for information. The Si/SiGe 2DEG appears to be a particularly promising host. Electrons are confined in quantum dots created by lateral confinement of a 2DEG. The mobility is also essential, as it directly defines the mean free path which affects quantum point contacts (QPC) and other single electron phenomena, which may be used as part of quantum dot devices.

3.2 Characterization of the 2DEG's

3.2.1 Sample Structures

Two samples will be discussed as examples of 2DEG's in modulation-doped heterostructures. Sample #3996 was grown on 20% Ge relaxed buffers AW2L, and #4736 was grown on 30% Ge relaxed buffers AW3L. The AW3L susbstrates were not

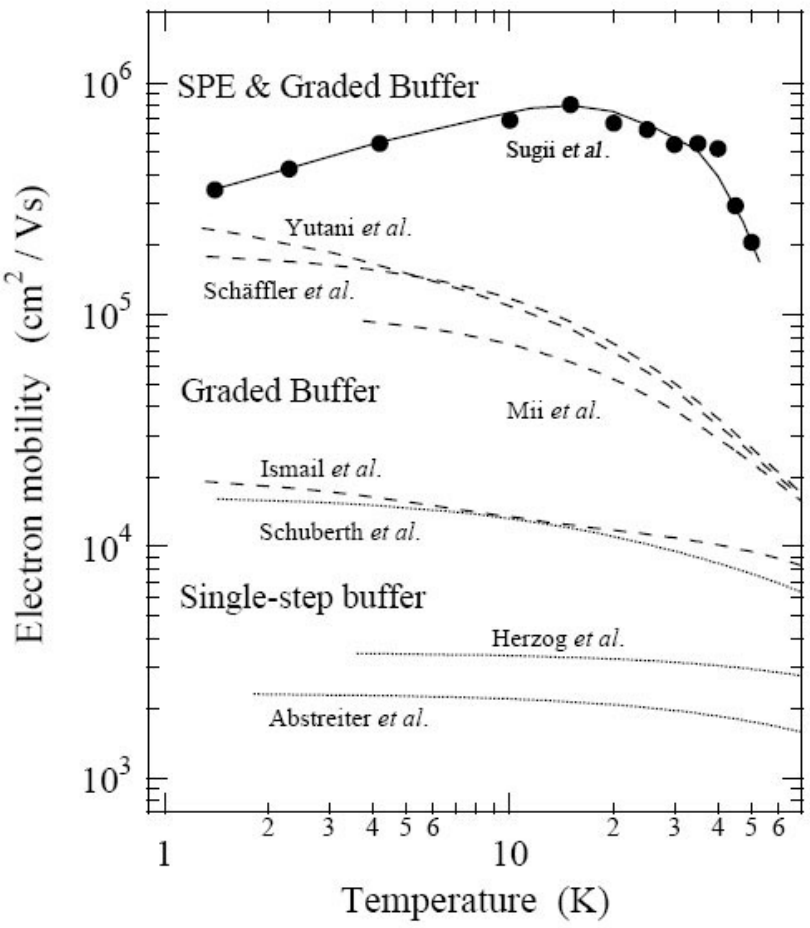


Figure 3.2: [25] Temperature dependences of electron mobility for a Si/SiGe heterostructure with a graded buffer layer ($0 \leq x_s \leq 0.2$) from literature [34, 35, 36, 37, 38, 39, 40]. Dotted lines are samples with a single-step buffer layer; dashed lines are samples with a graded buffer layer; solid line uses MBE combined with solid-phase epitaxy (SPE).

polished therefore have cross hatch patterns on the surface. The AW3H buffers with smooth surface were grown on heavily-doped starting Si. This has caused the diffusion of dopants into the SiGe buffers leading to excessive substrate leakages, which will be discussed in the next Section 3.2.2.

The samples used in growth are 1×1 cm squares resting on a 100-mm silicon carrier wafer. Prior to the loading, the surface is cleaned by a standard wet clean at room temperature in a H_2SO_4/H_2O_2 (7:3) solution for 15 minutes followed by a highly diluted HF (1:1000) dip for 2 minutes. After the wafer is transferred to the

chamber through the nitrogen-purged load lock, the chamber undergoes an *in situ* hot bake process with 5 slpm H_2 at 6 Torr at 900 °C for two minutes. The H_2 flow is then reduced to 3 slpm at the same pressure for growth. 26 sccm SiH_2Cl_2 is used for Si growth at either 700 or 750°C. GeH_4 is added for SiGe growth at 625 °C. The GeH_4 (0.8% in hydrogen) flow rates for $Si_{0.8}Ge_{0.2}$ and $Si_{0.7}Ge_{0.3}$ are 100 and 225 sccm, respectively. The PH_3 flow rate for doping in the supply layer is 2 sccm (100 ppm in hydrogen). Fig. 3.3 shows the nominal layer structures for both samples.

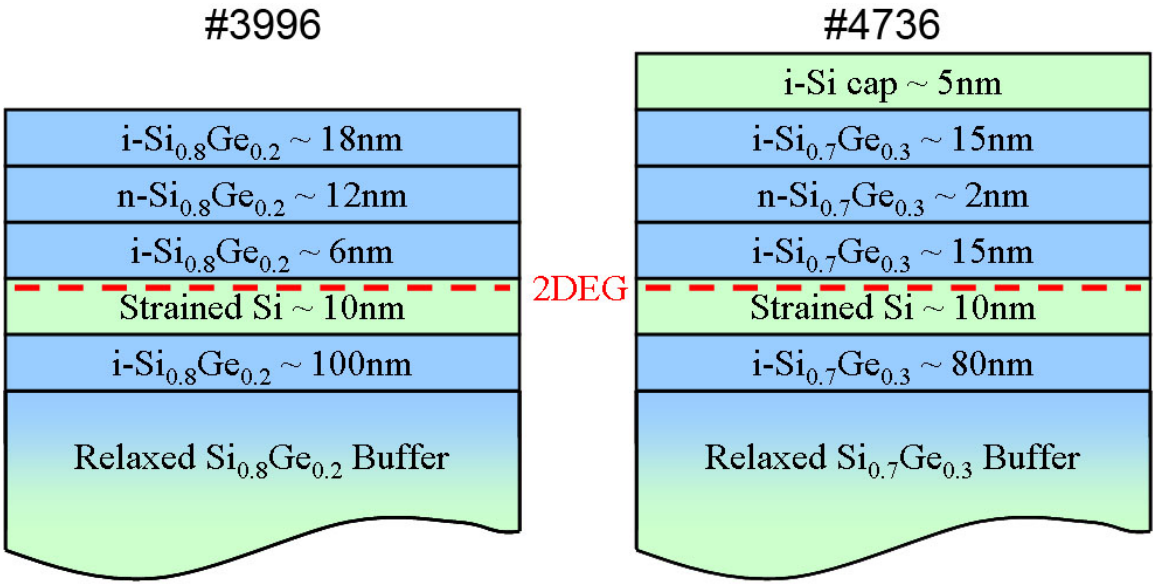


Figure 3.3: Layer sequences for the two 2DEG samples #3996 and #4736. The n-type doping level is $\sim 10^{19}$ cm^{-3} in both samples; grown with DCS as in Fig. 2.12

For processing, Hall bars are defined by optical lithography and etched by reactive ion etching (RIE) using a gas mixture of CF_4/O_2 in a PlasmaTherm 720 SLR Series system. Ohmic contacts are made to the channel by Au:Sb (1% antimony) evaporation, lift-off, and subsequent annealing at 430 °C for 10 minutes. For sample mouting, gold wires were bonded by soldering indium to the contact pads for external electrical measurements. Both samples show low-temperature Hall mobilities of around 10,000 cm^2/Vs at liquid helium temperatures 4.2 K and below. Sample #3996 has a 2-D electron density of 2.2×10^{12} cm^{-2} and #4736 has 0.96×10^{12} cm^{-2}. At present, the

mobility in these samples is limited by the high background phosphorus doping in the silicon ($\sim 10^{17}$ cm^{-3}), which also contributes to the high 2-D density. The background doping effect will be discussed in more details in Section 3.3.

3.2.2 Effect of Substrate Doping in Relaxed SiGe Buffers on Leakage

We have demonstrated the successful use of commercially available relaxed SiGe buffers in Princeton RTCVD system for strained Si/SiGe 2DEG. However, all samples grown on one particular batch of buffers, AW3H, have shown large substrate leakage even at liquid helium temperatures. We suggest that the substrate doping (arsenic) contributes to leakage current in relaxed buffers if the starting Si substrate is heavily doped.

In our measurement the substrate leakage is defined as current from the top 2DEG Hall bar metal contacts to the substrate. The substrate contact is a gold wire bonded to the backside of the sample. Fig. 3.4 shows a strong dependence of leakage current on the substrate doping at T = 4.2 K. Samples grown on both AW3H and AW3L were compared. For the heavily-doped Si substrate, the leakage current is in the μA range even with only a few hundred mV applied. Such substrate shorting makes not only side gating of nanostructures in the 2DEG impossible, but also prevents back gating of the 2DEG by applying a substrate voltage. However if a lightly-doped Si substrate is used, the leakage is only in the pA range, up to applied voltages of $\pm$30 V before breakdown. These two otherwise identical 2DEG structures were grown at less than 800 °C as described before, a thermal budget that does not cause significant dopant diffusion in silicon. The only other high temperature step was the growth of relaxed SiGe buffers at AmberWave systems, which was above 1000 °C.

To understand the origin of the substrate leakage, the doping profiles of the arsenic-doped substrates and SiGe relaxed buffers were analyzed by SIMS, as shown

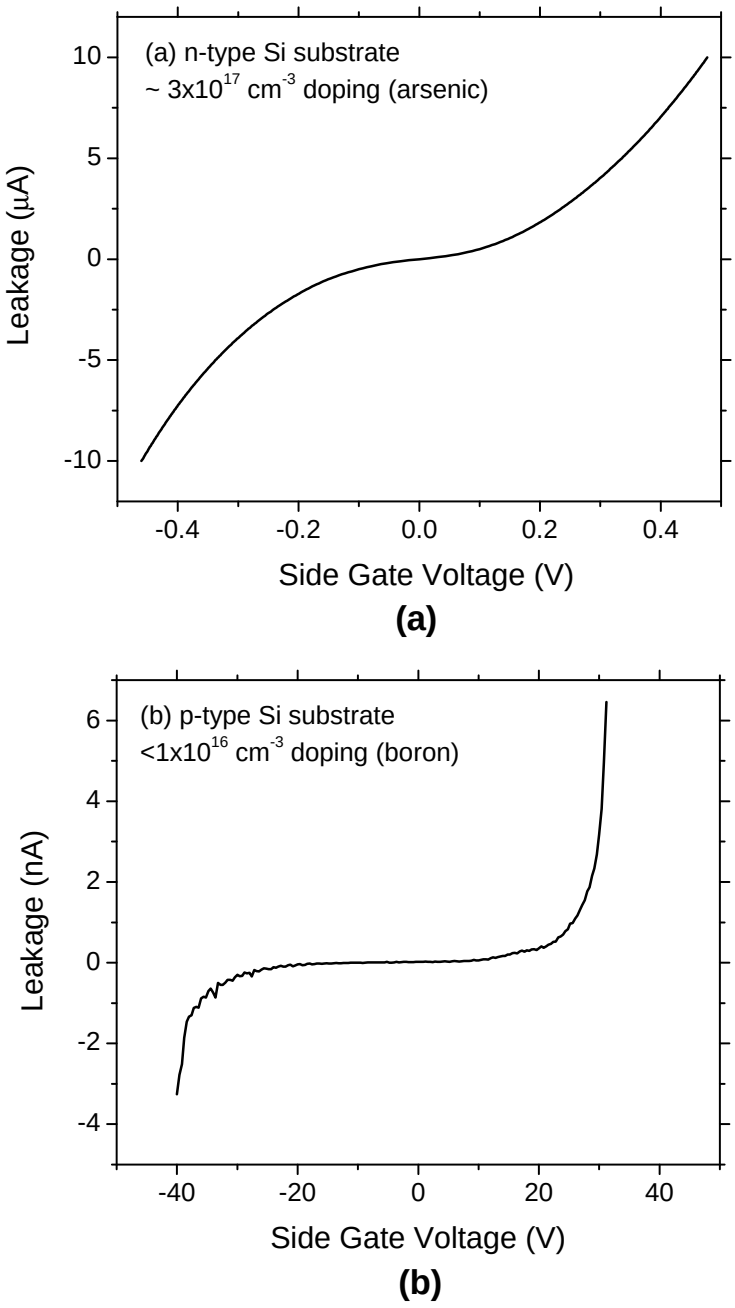


Figure 3.4: I-V curves from the 2DEG Hall bar mesa through the SiGe buffers to a back substrate contact for samples starting on (a) AW3H, a heavily n-type doped (arsenic) and (b) AW3L, a lightly p-type doped (boron) silicon substrates. Note the μA scale in (a) and nA scale in (b).

in Fig. 3.5. We found that during the high-temperature relaxed buffer growth, As diffused through the whole SiGe buffers. Assuming a diffusion length of $\sim$ 5 μm, we can extrapolate the As diffusivity in $Si_{0.7}Ge_{0.3}$ to be about 6×10^{-11} cm^2/s at T = 1000 - 1100 °C, more than three orders magnitude higher than the intrinsic As diffusivity in Si. As diffusion in relaxed SiGe has been studied in the past using ion-implantation method [43, 44], and typical diffusivity for As in $Si_{0.7}Ge_{0.3}$ at T = 1000 °C was reported to be in the mid 10^{-13} cm^2/s range. However, in these previous works As was implanted into the top SiGe surfaces where the dislocation density is low. Our result suggests that when As diffused from the starting Si substrate through the graded buffers with higher threading dislocation densities, the diffusion was further enhanced and penetrated the SiGe relaxed buffers. Similar leakage mechanism caused by enhanced dopant diffusion near misfit dislocations was also reported in the strained Si MOSFET on a SiGe relaxed buffer substrate [45]. Even in pure silicon, since the early days of bipolar transistor technology, the very fast dopant diffusion through threading dislocations in epitaxy was well known to form emitter-collector shorts or "pipes" [46, 47]. Two main mechanisms have been suggested, the fast diffusion of impurities down the dislocation cores and the enhanced diffusion of impurities to an enhanced vacancy concentration caused by climbing or interacting dislocations.

In addition to the enhanced As diffusion in the relaxed SiGe buffers, we suggest that arsenic segregates to the dislocations. Since the average As doping level in our buffers was $\sim 3 \times 10^{17}$ cm^{-3}, lower than the Mott metal-insulator transition level, for the dopants in the buffers to conduct at low temperatures (T < 4.2 K) there must be regions with an effective doping level that exceeds the Mott level. We suggest that a possible explanation is localized As segregation, which has also been studied in silicon by several groups [48, 49].

To avoid substrate leakage, we use only AW3L SiGe relaxed buffers grown on lightly-doped Si substrates ($< 1 \times 10^{16}$ cm^{-3}) for strained Si 2DEG and quantum dot

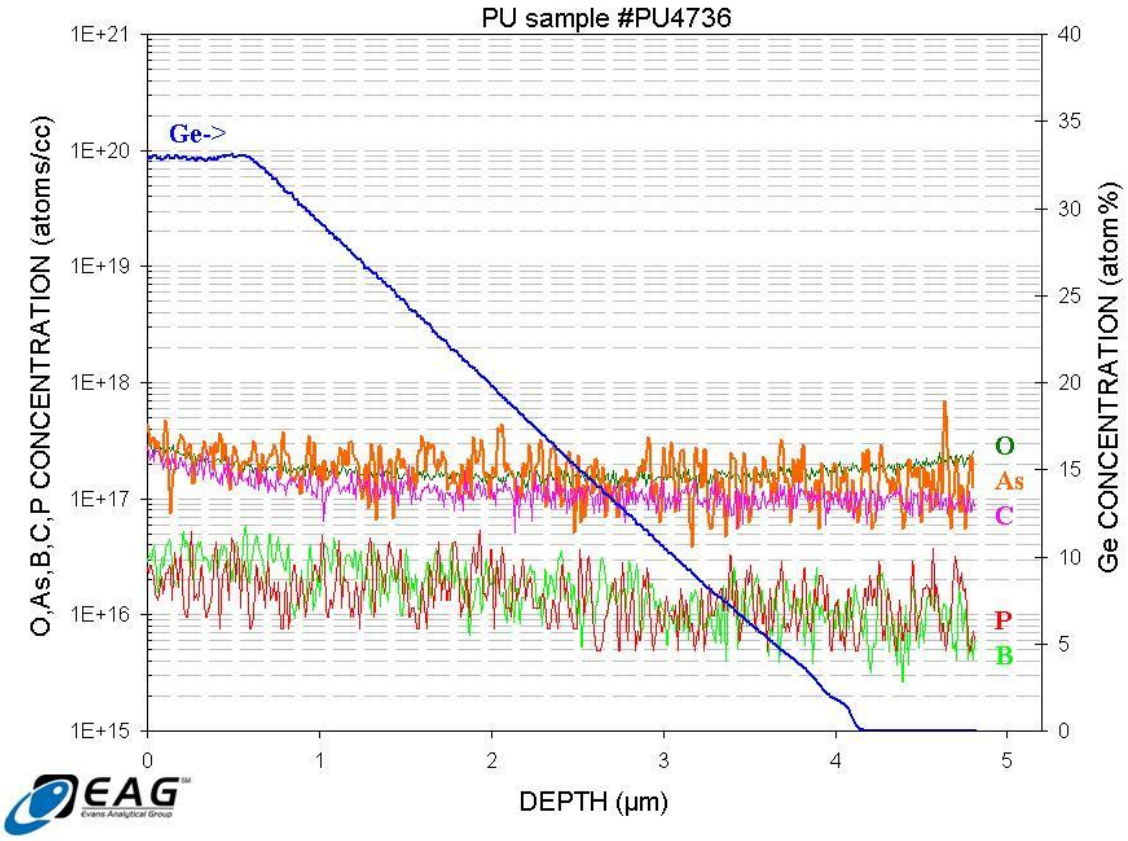


Figure 3.5: SIMS analysis of AW3H substrate showing the starting Si substrate, the linearly graded SiGe buffer, and the uniform $Si_{0.7}Ge_{0.3}$ buffer. The growth temperature of the relaxed SiGe buffer is over 1000 °C.

applications. With low substrate doping, we achieved successful gating and surface passivation, which will be covered in later chapters of this thesis.

3.2.3 Magneto-transport Properties

To further study the transport properties of the electron gases, magneto-transport measurements are taken in a closed-cycle He-3 refrigerator with superconducting magnet. These measurements were performed through collaboration with Professor Leonid Rokhinson's laboratory at Purdue University. As an example, Fig. 3.6 shows the results of sample #4736 in a magnetic field up to 8 Tesla. Well-defined Shubnikov-deHaas (SdH) oscillations and quantized Hall plateaus are observed. Also

from the Fourier transform of the oscillations in reciprocal field, we see only a single oscillation period. This confirms that only the lowest subband is occupied.

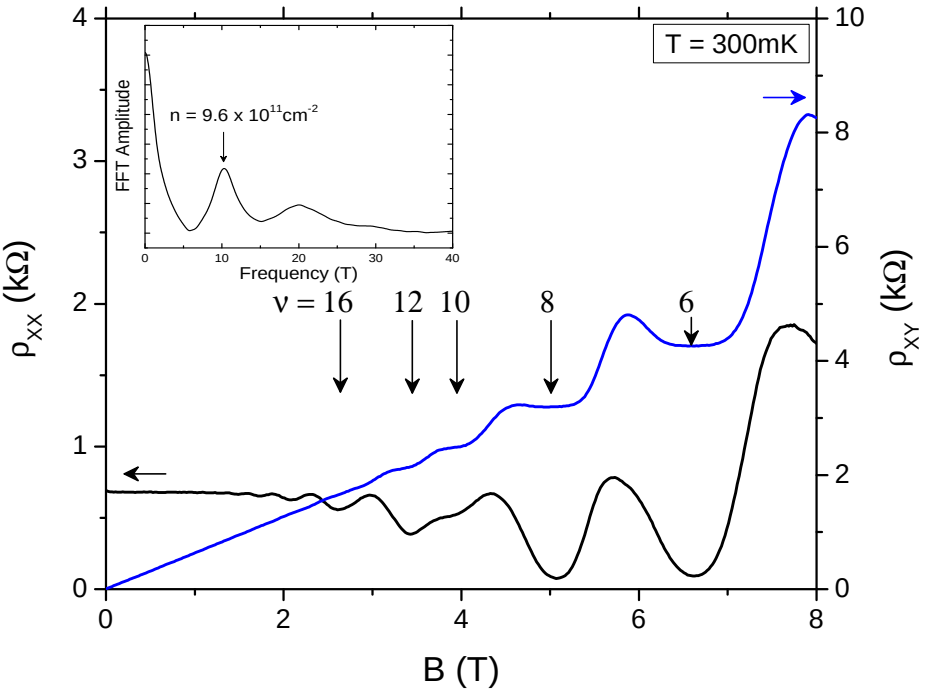


Figure 3.6: Longitudinal resistance ρ_{XX} and Hall resistance ρ_{XY} vs. magnetic field B at T = 300 mK, showing the integer quantum Hall effect. The filling factor ν is marked by arrows. The inset shows the Fourier spectrum of the longitudinal resistance.

In high fields we also observed a clear integer quantum Hall effect. At integral filling factors of ν, where $\rho_{XY}^{-1} = (e^2/h)\nu$, there are broad plateaus at the corresponding values of the Hall resistance that coincide with the minima in the longitudinal resistance. This occurs whenever the Fermi level lies between Landau levels. The change of these filling factors also indicates the system's degeneracy. At low fields, the total degeneracy is 4, resulting from the two-fold valley degeneracy (Δ_2) and the spin degeneracy,

$$g_{low} = g_v g_s = 4. \tag{3.1}$$

Beyond 4 T the Zeeman splitting lifted the spin degeneracy, as a result we observed filling factor of 10 and its changing by consecutive even integers, which indicates that

$$g_{high} = g_v = 2. \tag{3.2}$$

From the onset field of Zeeman spin splitting, we can also estimate the Landau level broadening in the 2DEG. Since the bulk Si has an effective g-factor of 1.99, if we ignore the small enhancement of g-factor in strained Si due to exchange interactions, the Landau level broadening

$$\Gamma = g\mu_B B \approx 0.46\ meV, \tag{3.3}$$

where $\mu_B = e\hbar/2m_0$ is the Bohr magneton.

Magneto-transport measurements on the 20% Ge 2DEG sample #3996 yielded very similar results. The filling factors are larger due to the higher electron density, and also the Landau level broadening is smaller.

3.2.4 Electron Spin Resonance of Electrons in Si and SiGe

In recent years, considerable efforts have been put towards spin manipulation in modulation-doped Si/SiGe heterostructures, due to its important role in quantum computing. To study the possibility of g-factor tuning in our 2DEG, we investigated the anisotropy of g-factor and electron spin resonance (ESR) linewidth in these quantum wells.

There are two popular mechanisms to manipulate spins in semiconductors. One is the Bychkov-Rashba (BR) effect [50]. The BR effect is caused by broken mirror symmetry induced by structure and/or an applied electric field (structure induced asymmetry, SIA). As an alternative mechanism, g-factor tuning has been proposed. In such a scheme spins are assumed to be selectively manipulated by a resonant radio

frequency field.

We first grew a 30% Ge 2DEG sample #4754, which is very similar to #4736. The ESR spectrum is measured through collaboration with Professor Stephen A. Lyon's group at Princeton University. Fig. 3.7 shows the spectrum, a shift in g-factor ($\Delta g = 0.0002$) with respect to the direction of external field is clearly present. To interpret this anisotropy, we need to consider the BR effect, which accounts for the lowest order of spin-orbit interaction (SOI). The SOI causes zero-field spin splitting and can be decribed by an effective magnatic field term:

$$\mathbf{H}_{BR} = \frac{2\alpha_{BR}k_F}{g_0\mu_B}\mathbf{e}_k \times \mathbf{e}_z, \tag{3.4}$$

where k_F is the electron momentum at Fermi level, $\mathbf{e}_k$ is the direction of electron velocity, and $\mathbf{e}_z$ refers to the growth direction (001). The BR parameter α_{BR} is a material constant dependent on structure that reflects the strength of SOI.

In thermal equilibrium, all velocity directions are isotropically distributed. Averaging the resulting total field yields an anisotropy of the resonance field. In an external magnetic field H_0, the effective BR field will cause the measured g-factor depending on the field orientation (angle θ, with respect to $\mathbf{e}_z$):

$$g = g_0\left[1 + \frac{H_{BR}^2}{4H_0^2}(1 + cos^2\theta)\right]. \tag{3.5}$$

This leads the g-anisotropy shown in the spectrum:

$$\Delta g = |g(0^\circ) - g(90^\circ)| = g_0\frac{H_{BR}^2}{4H_0^2}. \tag{3.6}$$

Our measured g-anisotropy is similar to numbers reported by other groups [51], which is about 0.0002 for a pure silicon channel. We also evaluated that $\alpha_{BR} = 1.58 \times 10^{-13}$ eV·cm from g-factor using equation (3.6), while the the reported value is about $5{\times}10^{-13}$ eV·cm in silicon.

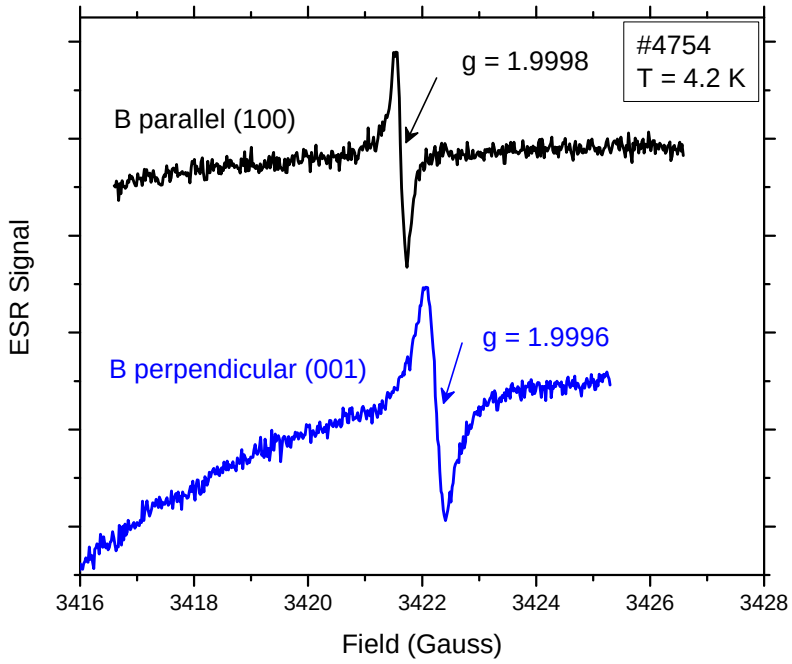


Figure 3.7: The electron spin resonance spectrum of the Si 2DEG sample #4754 in both perpendicular and in-plane magnetic field.

In their work an increase in both g-anisotropy and ESR linewidth with Ge content in the channel was observed. It can be explained by an increase of SOI with more Ge. To confirm this, we also grew a 2DEG sample #4759 with a $Si_{0.95}Ge_{0.05}$ channel and otherwise identical structure to #4754 and measured the ESR spectrum. Fig. 3.8 is the result. With the added 5% Ge in channel, one clearly finds that the g-factor shift becomes larger ($\Delta g = 0.0022$), and the ESR peak lindwidth is broadened.

The ESR signal linewidth ΔH for in-plane field is influenced by the BR effect and can be calculated as below:

$$\Delta H \approx \frac{\pi \alpha_{BR}^2 n_s}{\hbar g_v g \mu_B} \tau_k, \tag{3.7}$$

where τ_k is the momentum relaxation time. To the first order, both Δ_g and Δ_H

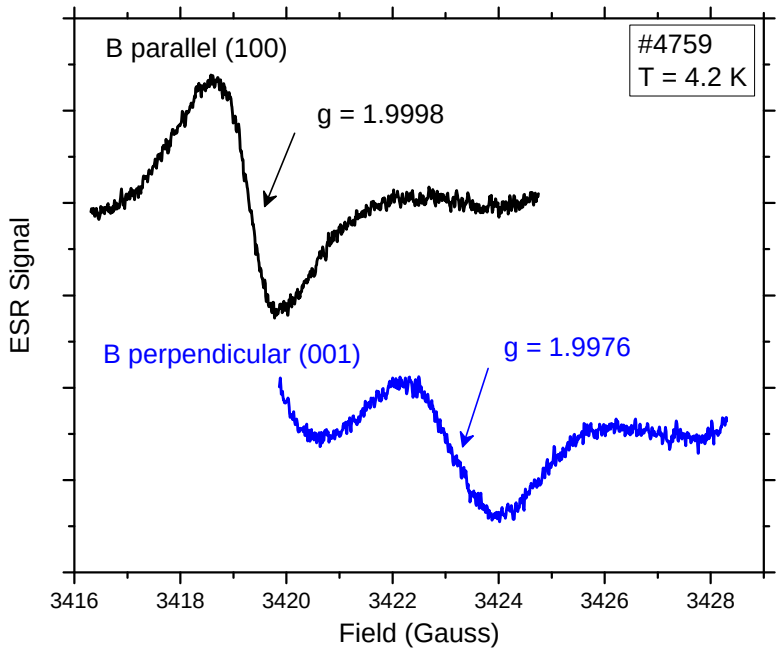


Figure 3.8: The electron spin resonance spectrum of the $Si_{0.95}Ge_{0.05}$ 2DEG sample #4759 in both perpendicular and in-plane magnetic field.

increase proportionally to the square of the BR parameter α_{BR}. Therefore, adding a small amount of Ge to the Si quantum well channel shifts the ESR to smaller g-factors because of the stronger SOI in SiGe. This effort can provide an alternative way for g-factor tuning in quantum dots. The growth of such germanium added channel is also compatible with our existing RTCVD growth routines.

3.3 Theoretical Mobility Models

3.3.1 Calculation of Mobility Limited by Coulomb Scattering Mechanisms

To better understand and estimate the ultimate mobilities that can be achieved in n-type modulation-doped Si/SiGe heterostructures, many theoretical studies were

performed to account for the influence of various scattering mechanisms. Typical mechanisms include Coulombic interactions with remote impurities or background dopants, scattering due to threading dislocations in the buffers, and alloy scattering. With our current growth conditions, high background doping level is likely to limit the achievable mobility. Hence we will focus on Coulomb scattering mechanisms and present a quantitative study within a simple framework published by AT&T Bell Laboratories [53].

Consider free 2-D electrons in a normalization area A in the x-y plane. The electrons are scattered by potential energy V(z,$\mathbf{r}$) from the impurities, where $\mathbf{r}$ is the in-plane position. Define the initial and final states to be the plane waves $\phi_i(z)$ and $\phi_f(z)$. Using an isotropic effective mass m*, the elastic scattering rate is calculated by Fermi's golden rule within the Born approximation

$$\begin{aligned}
\tau^{-1} &= \frac{2\pi}{\hbar}\sum_f |\langle f|V|i\rangle|^2\,\delta(E_f - E_i) \\
&= \frac{2\pi m^*}{\hbar^3|k_f|}\int \frac{A}{(2\pi)^2} d^2\mathbf{k}\delta(k_f - k_i) \\
&\quad \times \left|\int dz\phi_f^*(z)\phi_i(z)\int \frac{d^2\mathbf{r}}{A}\times exp[i(\mathbf{k}_f - \mathbf{k}_i)\cdot\mathbf{r}]V(z,\mathbf{r})\right|^2 . \qquad (3.8)
\end{aligned}$$

Next we represent the scattering potential V(z,$\mathbf{r}$) by its 2-D Fourier transform, or the power spectrum

$$V_{eff}(\mathbf{q}) = \int exp(i\mathbf{q}\cdot\mathbf{r})\frac{d^2(\mathbf{r})}{A}\int_{-\infty}^{\infty} V(\mathbf{r},z)\phi_f^*(z)\phi_i(z)dz, \qquad (3.9)$$

$$S(\mathbf{q}) \equiv \lim_{A\to\infty} AV_{eff}^2(\mathbf{q}). \qquad (3.10)$$

Thus the elastic scattering rate is

$$\begin{aligned} \tau^{-1} &= \frac{2\pi m^*}{\hbar^3 |k_f|} \int \frac{A}{(2\pi)^2} d^2\mathbf{k} \delta(k_f - k_i) V_{eff}^2 \\ &= \frac{m^*}{2\pi\hbar^3} \int S(\mathbf{q}) d^2\mathbf{k} \delta(k_f - k_i). \end{aligned} \tag{3.11}$$

The elastic scattering geometry is show in Fig. 3.9. In the degenerate, low-temperature limit, both $\mathbf{k}_i$ and $\mathbf{k}_f$ are the Fermi wave vector. The above integral over the final wave vector is confined by the delta function to the Fermi surface.

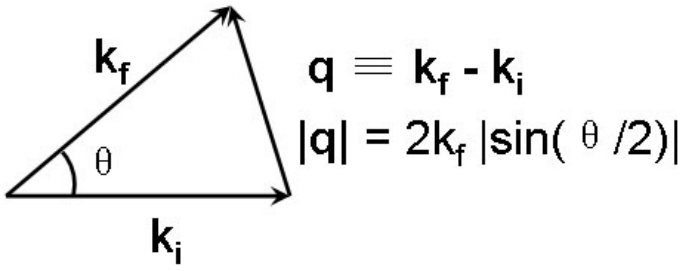


Figure 3.9: Elastic scattering geometry in two-dimensions. $\mathbf{k}_i$ and $\mathbf{k}_f$ refer to the initial and final wave vectors. θ is the scattering angle.

If the potential fluctuations are isotropic, so that S($\mathbf{q}$) is independent of the angle θ, and $dq/d\theta = k\sqrt{1 - q^2/4k^2}$. The total relaxation time is

$$\begin{aligned} \tau^{-1} &= \frac{m^*}{2\pi\hbar^3} \int_0^{2\pi} d\theta S(\mathbf{q}) \\ &= \frac{m^*}{\pi\hbar^3} \frac{1}{k} \int_0^{2k} \frac{S(q)dq}{\sqrt{1 - q^2/4k^2}}. \end{aligned} \tag{3.12}$$

The mobility reflects the momentum relaxation rate, which includes the fraction of the momentum lost, $1 - \cos(\theta) = q^2/2k^2$,

$$\tau_m^{-1} = \frac{m^*}{\pi\hbar^3} \frac{1}{k} \int_0^{2k} \frac{S(q)dq}{\sqrt{1 - q^2/4k^2}} \frac{q^2}{2k^2}. \tag{3.13}$$

Next we need to include the screening for each wave vector $\mathbf{q}$, which causes the

screened potential reduced by

$$\epsilon(\mathbf{q}) \equiv \frac{V(\mathbf{q})}{V_0(\mathbf{q})} = \frac{q}{q+q_s}, \tag{3.14}$$

where

$$q_s \equiv \frac{e^2 DOS}{2\epsilon\epsilon_0} = \left[g_v g_s (m^*/m_0)/\epsilon\right](e^2 m_0/4\pi\epsilon_0\hbar^2). \tag{3.15}$$

For electrons in tensile-strained silicon, the valley and spin degeneracy g_v and g_s are both 2. With the above equations (3.13) and (3.15), various scattering mechanisms can be evaluated with the integral in the form of the screened power spectrum of potential. In particular, we are interested in the Coulombic scattering, which is caused by ionized impurities either from the remote dopant layer or from uniform background charges.

First we will consider the remote impurity scattering. The supply layer is modeled as a thin layer at $z = -h$ from the top of the strained Si channel ($z = 0$). Monroe et al. showed that the power spectrum of the charge sheet at its own plane is

$$S(\mathbf{q}, z = -h) = N_D d_{doping} \left(\frac{e^2}{2\epsilon\epsilon_0 q}\right)^2. \tag{3.16}$$

And away from the sheet the potential decays exponentially

$$S(\mathbf{q}) = \frac{e^4 N_D d_{doping}}{\left[2\epsilon\epsilon_0(q+q_s)\right]^2} e^{-2qh} f(q), \tag{3.17}$$

where

$$f(q) = \left(\int_{-\inf}^{\inf} dz |\phi(z)|^2 e^{-qz}\right)^2. \tag{3.18}$$

And $f(q)$ is close to unity if h is replaced with the effective setback h_{eff} between the centroid of the dopant sheet and the centroid of the wave function. The density of states gives an approximate 2DEG wavefunction width of about a quarter of the

Bohr radius $a_B = (4\pi\epsilon\hbar^2)/(me^2)$.

$$h_{eff} = d_{doping}/2 + d_{spacer} + \frac{\pi\epsilon\hbar^2}{m^* e^2}. \tag{3.19}$$

The final result is that, for remote impurity scattering

$$\mu_{remote} = \frac{e\tau_m}{m^*} \approx \frac{16\sqrt{\pi g_v g_s e^2 n_{2D}^3}\, h_{eff}^3}{\hbar N_D d_{doping}}. \tag{3.20}$$

The predicted mobility increases rapidly with both effctive setback thickness and increasing density. The Fermi wave vector increases with the increasing density, so the integral in (3.13) will be more dominated by smaller scattering angles. As an estimate, for an effective setback $h_{eff} = 15\ nm, n_{2D} = 6\times10^{11}\ cm^{-2}, N_D d_{doping} = 1\times10^{12}\ cm^{-2}$, the calculated μ=190,000 cm^2/Vs, more than one order of magnitude higher than the highest mobility that we have seen. Therefore the Coulombic scattering from remote impurity is not our mobility limitation mechanism.

Next we will consider the effect of background impurities. The background impurities are treated as a uniform charge distribution extended to the whole space.

$$\begin{aligned} S(\mathbf{q}) &= \frac{N_{background} e^4}{\left[2\epsilon\epsilon_0(q+q_s)\right]^2} \int_{-\infty}^{\infty} dz e^{-2q|z-\overline{z}|} \\ &= \frac{N_{background} e^4}{\left[2\epsilon\epsilon_0(q+q_s)\right]^2} \frac{1}{q}. \end{aligned} \tag{3.21}$$

For the well-screened case, $q \ll q_s$, the integral (3.13) yields

$$\mu_{background} = \frac{e\tau_m}{m^*} = \frac{\sqrt{g_v^3 g_s^3 e^2 n_{2D}}}{4\sqrt{\pi}\hbar N_{background}}. \tag{3.22}$$

The above equation shows that the mobility will decrease inversely proportional to the background impurity level.

The total electron mobility is related to the two Coulomb scattering mechanisms

by the following equation:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{remote}} + \frac{1}{\mu_{background}}. \tag{3.23}$$

3.3.2 The Effect of Background Impurities

One of the major drawbacks of our RTCVD system is the high background phosphorus doping level due to the reactor history. By using dichlorosilane as the silicon precursor at growth temperature between 600 - 750 °C, SIMS analysis shows a typical background P level of around 3×10^{17} cm^{-3} in Si. The P level usually increases even more with the addition of germanium, perhaps due to the lower heat of formation of GeP than that of SiP phosphide (6 vs. 15 kcal/mole) [52]. Levels of around 1×10^{18} cm^{-3} are typical in SiGe. Fig. 3.10 shows a SIMS analysis of multiple Si/SiGe quantum wells. Note the background phosporous level rises in SiGe layers. As a result, our achieved electron mobility is limited by scattering from such ionized impurities.

In order to evaluate the detrimental effect of background doping level on the 2DEG mobility, we calculated electron mobilities in #4736 for different background doping levels using equations (3.20), (3.22) and (3.23). To provide a more accurate calculation, we also take into account that 2-D electron density will depend on the background impurities in any given structure. This can be modeled by solving one-dimensional Poisson's equation self-consistently. We used a free program written by G. L. Snider at Notre Dame [54] and modified its material parameters to include strained Si and SiGe bulks. For simplicity, a constant background doping of phosphorous is assumed in all grown layers. For a fixed background level, we first extracted the 2-D electron density in strained silicon using Snider's program, then mobility components were calculated accordingly.

Fig. 3.11 shows the results for the mobility calculation. From the lower figure we can see that the two scattering mobility curves cross at a background doping level

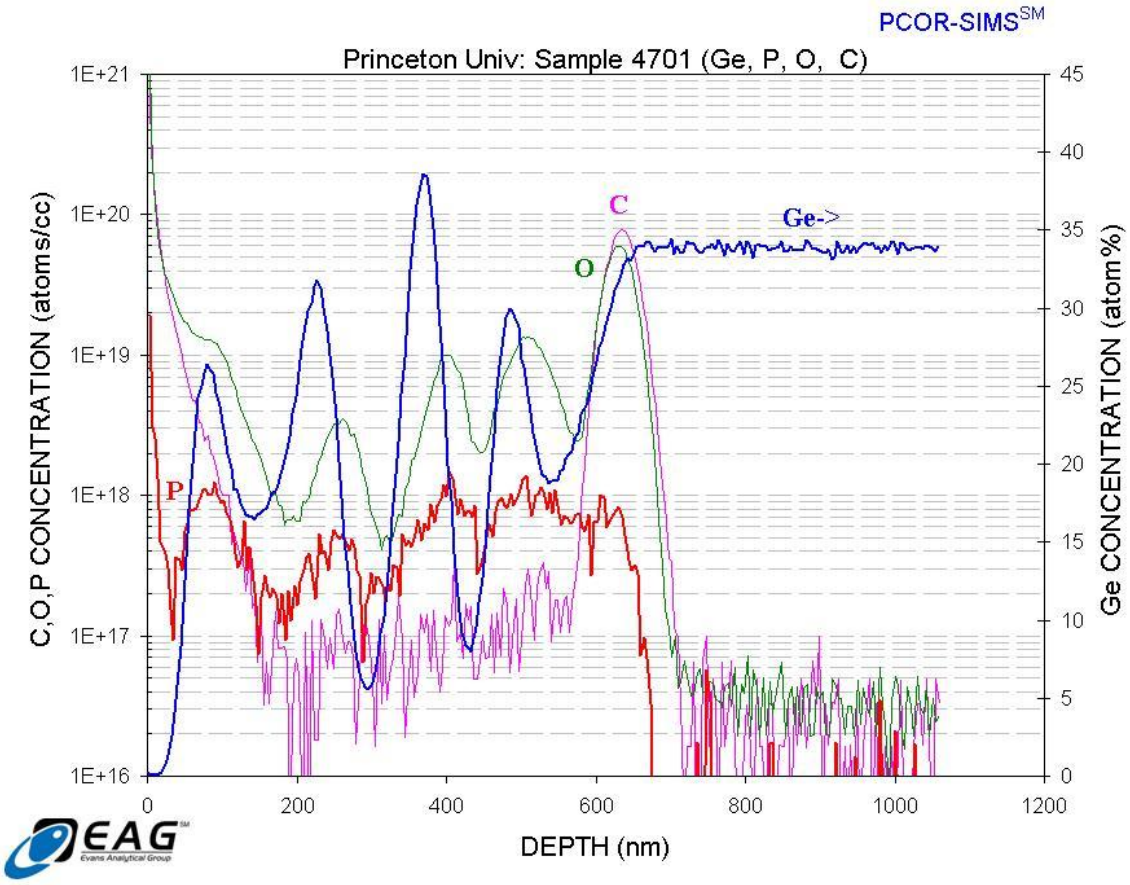


Figure 3.10: SIMS analysis of sample #4701 showing multiple Si quantum wells on $Si_{0.7}Ge_{0.3}$ relaxed buffers. The growth temperatures for Si and SiGe are 625 °C and 700 °C, respectively. The sample was not doped intentionally with phosphorus.

of 8×10^{15} cm^{-3}. In our case, the high background impurity level is clearly the limiting scattering mechanism. The measured density and mobility of sample #4736 both indicate a background doping level around 1 - 3×10^{17} cm^{-3}. Therefore, our experimental mobility of 10,000 cm^2/Vs is consistent with the theoretical calculation.

Another important quantity when evaluating 2DEG mobility is the Dingle ratio, τ_t/τ_s, defined as the ratio of the transport scattering time τ_t to the single-particle elastic relaxation time τ_s. A large ratio indicates that long-range Coulombic scattering at remote impurities is dominant, preferentially small-angle scattering occurs. On the other hand, if isotropic, short-range scattering events such as background impurities or interface charge scattering occurs, the momentum loss factor (1-cos θ) in the τ_t will

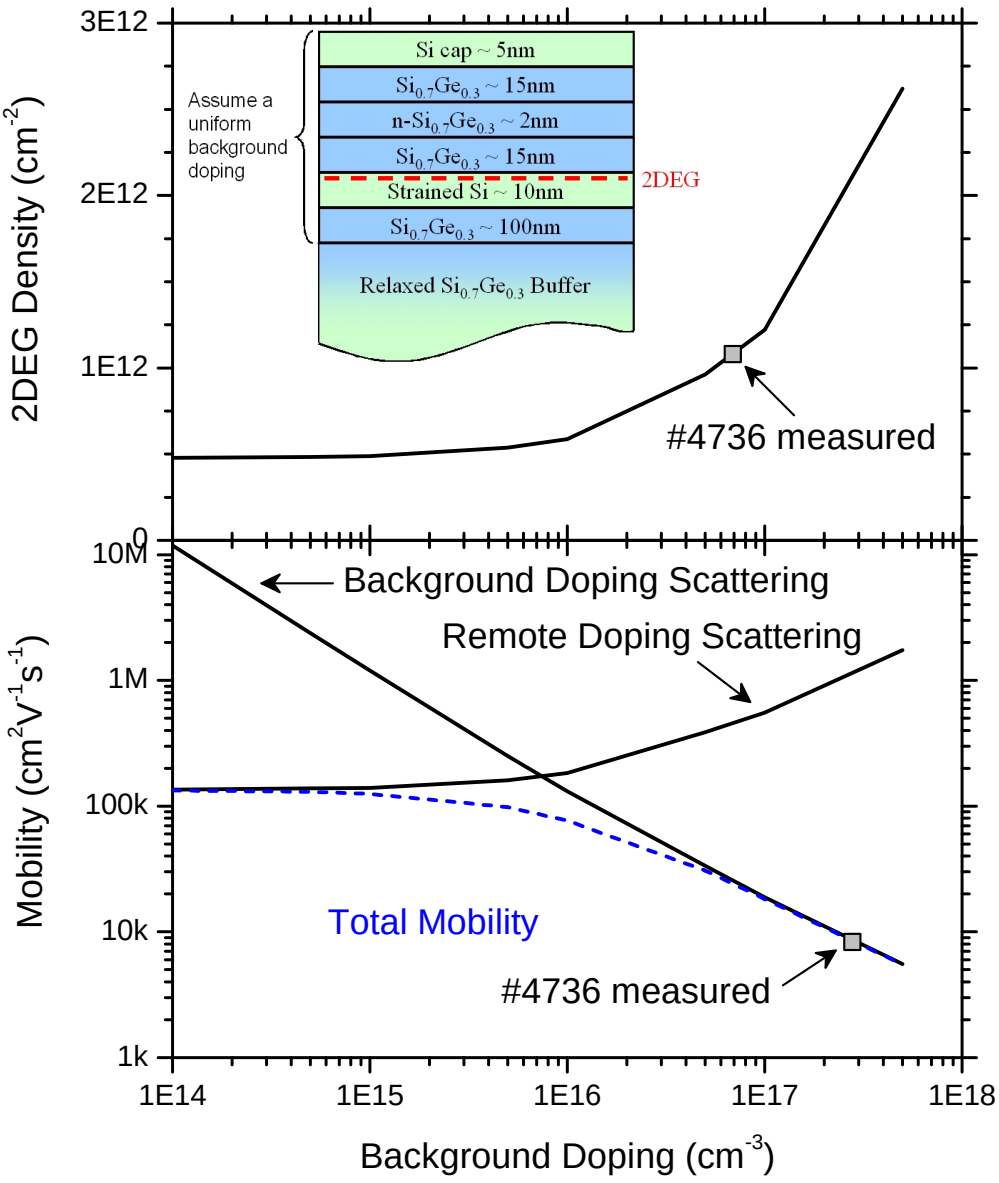


Figure 3.11: Calculated 2DEG densities and electron mobilities limited by Coulombic scattering mechanisms vs. uniform background impurity levels. The inset shows the layer structures assumed in the calculation.

drop. Hence the ratio will be close to unity. For our sample #4736, the τ_t can be estimated from the mobility and is around 1.08 ps. The τ_s is deduced from the onset magnetic field of SdH oscillations B_{on}

$$\tau_s \omega_B = 1 \;\Rightarrow\; \tau_s = \frac{1}{\omega_B} = \frac{m^*}{eB_{on}}. \tag{3.24}$$

For a B_{on} = 1.22 T as shown in Fig. 3.6 and $m^* = 0.19\ m_0$, τ_s = 0.89 ps. So the Dingle ratio is about 1.22, indeed very close to unity.

3.3.3 Efforts Towards Lower Background Impurities

The high background impurity level is an important problem to solve in our RTCVD. There are several ongoing concerns of possible means to reduce the background doping level.

Normally the background level decreases with higher growth temperature if all other conditions remain the same. In our experiments we found that 2DEG mobility increased from 5,000 to 10,000 cm^2/Vs after raising the silicon growth temperature from 700 to 750 °C. Fig. 3.12 shows the effect of growth temperature on background level [55]. However raising the growth temperature has its limitations. First, higher temperature will increase the growth rate, making it more difficult to control the thickness and abruptness of thin Si/SiGe layers. Second, the increased dopant diffusion will make it difficult to control the sharpness of doping profiles.

Using alternative silicon and/or germanium precursors is a promising solution. Several silicon precursors including disilane (Si_2H_6) and neopentasilane (Si_5H_{12}) are being installed and calibrated in our RTCVD system [56]. Fig. 3.13 shows a SIMS analysis of multiple Si/SiGe quantum wells using Si_2H_6 and GeH_4. We find a reduction of phosphorous background level in SiGe layers compared to the previous results in Fig. 3.10, especially at the Si/SiGe interface and in the SiGe spacer layer, which is

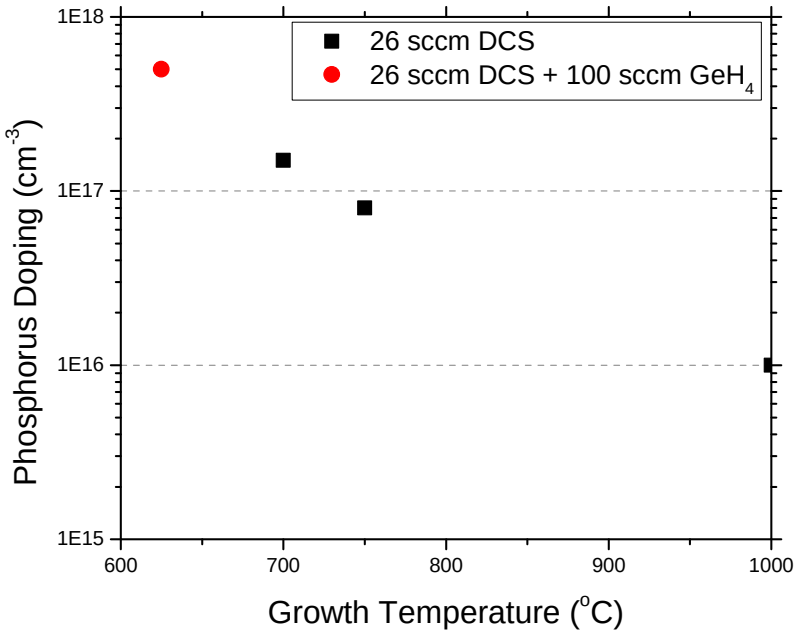


Figure 3.12: Background phosphorus doping levels in Si and SiGe layers vs. growth temperature.

just above the centroid of 2DEG. The background doping in Si seems to be about the same or slightly lower compared to the growth with dichlorosilane.

3.4 Modulation of Si/SiGe 2DEG Electron Density with Top Gating

3.4.1 Al_2O_3 High-k Gate Dielectric by Atomic Layer Deposition

The modulation of electron density in the Si/SiGe 2DEG is of great interest because the fabrication of complex low dimensional devices relies upon such control. Unlike in III-V semiconductor systems, Schottky gates on Si/SiGe heterostructures have proven

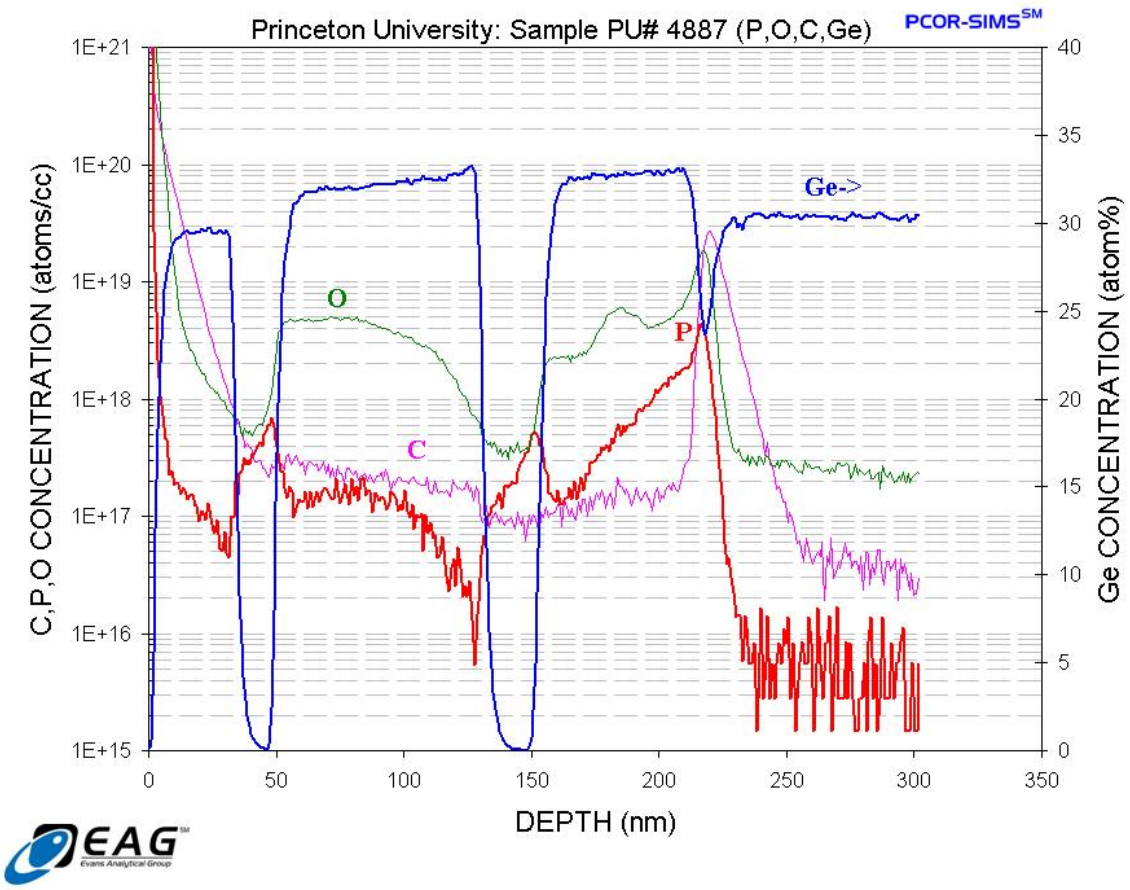


Figure 3.13: SIMS analysis of sample #4887 showing multiple Si quantum wells on $Si_{0.7}Ge_{0.3}$ relaxed buffers. The Si and SiGe layers are both grown at 575 °C using Si_2H_6 as the silicon precursor.

leaky [57]. It was argued that the large leakage was caused by dopant segregation at the surface or threading dislocations. Recently palladium metal top gates have been successfully applied to quantum dot gate geometries [58, 59]. However, the leakage problem over large area remains poorly understood.

As an alternative, effective gating by gate dielectrics have been proposed [60]. Atomic-layer-deposited (ALD) gate dielectric shows superior characteristic compared to plasma-enhanced CVD (PECVD) silicon dioxide and metal Schottky gate in terms of leakage and interface trap density. A variety of ALD thin films have been intensively studied as high-k gate dielectrics for CMOS applications. At Princeton, we can deposit ALD Al_2O_3 with a state-of-the-art Cambridge NanoTech model Savannah

100 reactor. This process for Si/SiGe 2DEG gating was first developed by Lai et al. in Professor Daniel C. Tsui's group at Princeton [61].

The principle of ALD is based on sequential pulsing of chemical precursor vapors, a cycle of which forms one atomic layer. This generates pinhole free coatings that are extremely uniform in thickness, even deep inside pores, trenches and cavities. As an example of Al_2O_3 deposition, one trimethyl aluminum (TMA) and one H_2O vapor pulse form each cycle, and deposit a monolayer of Al_2O_3 of approximately 0.9Å in thickness. The two reaction steps in each cycle are:

$$Al(CH_3)_{3(gas)} + : Al{-}O{-}H_{(solid)} \rightarrow : Al{-}O{-}Al(CH_3)_{2(solid)} + CH_4, \quad (3.25)$$

$$2H_2O_{(gas)} + : O{-}Al(CH_3)_{2(solid)} \rightarrow : Al{-}O{-}Al(OH)_{2(solid)} + 2CH_4. \quad (3.26)$$

Fig. 3.14 shows such ALD cycles. In addition to its gating capacity, ALD Al_2O_3 can also be used as surface passivation for future device packing, as it is robust against surface reactions and moisture absorption over large area.

3.4.2 Modulation of Si/SiGe 2DEG Electron Density

For device fabrication, a 2DEG sample #4748 was first grown and subsequently etched into a Hall bar. After a wet chemical clean of sample surface, a 90-nm thick Al_2O_3 layer was deposited at a substrate temperature of 300 °C with 1000 cycles. Prior to the ALD process, the native oxide of the Si substrate was removed by diluted HF dip. The first 20 cycles are pulsed with only H_2O vapor to form well-defined chemical native silicon oxide. Then each complete cycle has two precursor exposure pulses and a 5-sec N_2 purge in between. The growth rate at 300 °C is confirmed to be 0.9 Å per cycle using ellipsometry (model Gaertner Scientific L3W16). Contact holes are wet etched through the oxide. The etch rate of Al_2O_3 in 1:10 buffered oxide etch (BOE) solution is 4 Å/s. Ohmic contacts are then made by thermal evaporation,

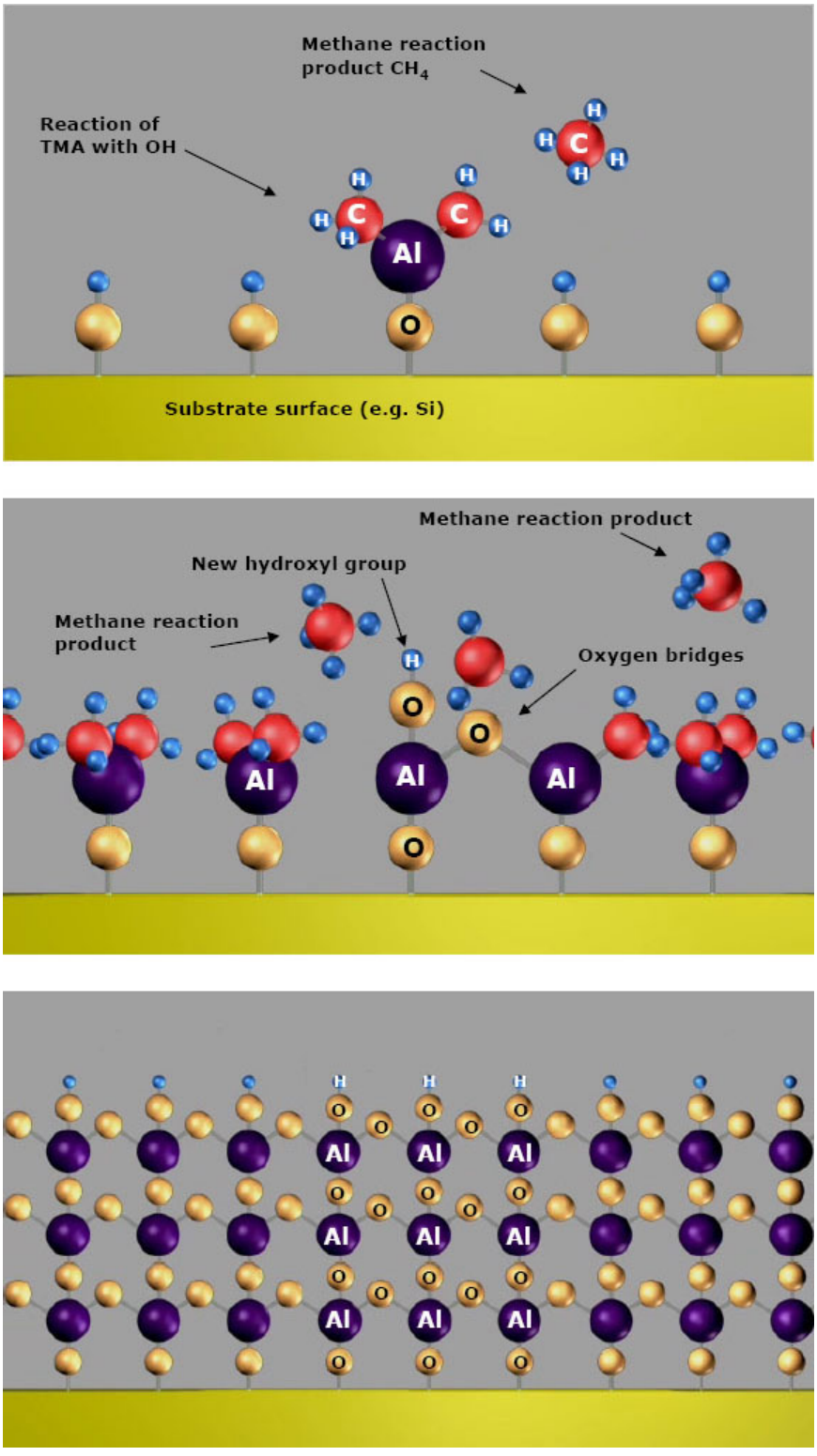


Figure 3.14: ALD cycle for Al_2O_3. Two reaction steps in each cycle as well as completed monolayers are shown. (Image courtesy of Cambridge NanoTech, www.cambridgenanotech.com)

lift-off and annealing using the same process described before. Finally, an aluminum gate is defined by lift-off on the gate dielectric. Fig. 3.15 shows the schematic view of the finished device structure.

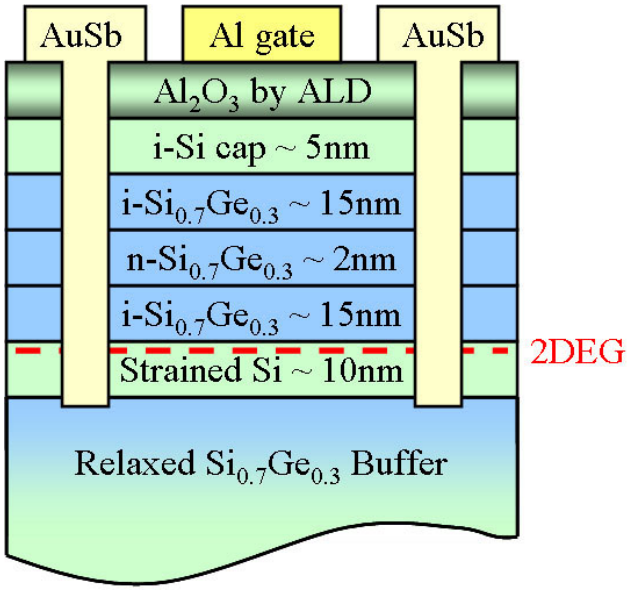


Figure 3.15: Schematic view of an n-channel Si/SiGe MOSFET with ALD Al_2O_3 as gate dielectric.

After the gate fabrication, the sample was mounted in a He-3 refrigerator. The gate leakage is negligible (< 20 pA) within the entire gate voltage scan range, as shown in Fig. 3.16. Low-temperature magneto transport traces were taken with applied gate voltages. Fig. 3.17 shows the traces at different gate voltages. The electrons are depleted with more negative gate voltage applied as in a depletion-mode n-channel MOSFET. The reduction in electron density is reflected in both the change of Hall slope and the SdH oscillation period. To take a closer look at the SdH and quantum Hall effect, Fig. 3.18 shows the SdH oscillations and the corresponding filling factors at the resistance minina at two difference gate voltages. At both gate voltages the behavior is very similar to the 2DEG #4736 without top gating. At low field, the filling factor ν changes by 4 indicating a total four-fold degeneracy, at field beyond 4 T only the two-fold valley degeneracy remains.

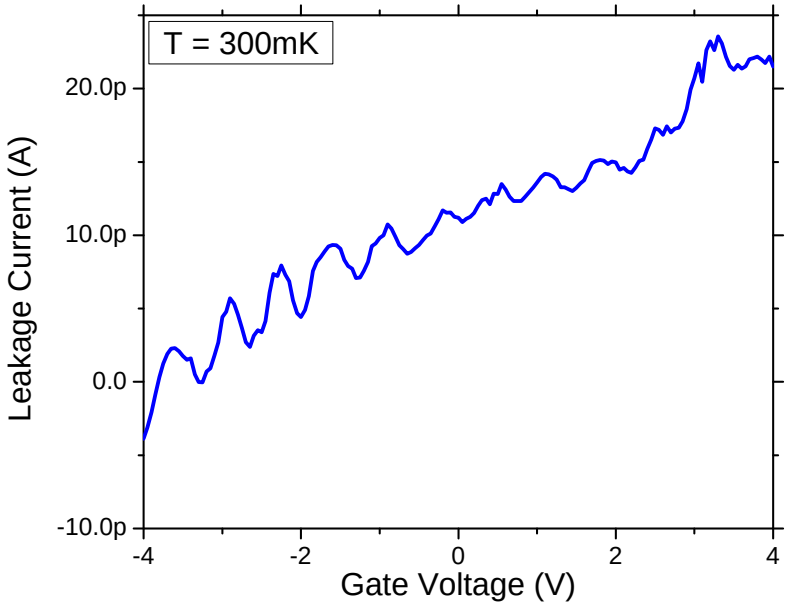


Figure 3.16: Gate leakage current through the ALD Al_2O_3 vs. applied voltage.

Also as a result of the depleted 2DEG with negative gate voltage, the electron mobility is reduced. Based on our previous equations (3.20) and (3.22), the elastic Coulombic scattering rates strongly depend on Fermi wave vector. If we assume that the background impurity scattering is the limitation mechanism, then the $\mu_{background}$ should be proportional to the Fermi wave vector, or the square root of electron density. Another observation from the magneto transport measurement is that the onset magnetic field of SdH oscillations also shifts to the right as more negative gate voltage is applied, indicating a shorter single-particle elastic relaxation time τ_s. As a result of the reduction in both relaxation times τ_t and τ_s, the Dingle ratio does not change much with the gate voltage. Fig. 3.19 shows the measured results of both electron density and mobility as a function of the applied gate voltage.

To quantitatively study the gating characteristics, we calculated the electron density by incorporating a simple MOS structure into the 1-D Poisson's equation solving scheme we mentioned in the previous section. The ALD Al_2O_3 is modeled with rela-

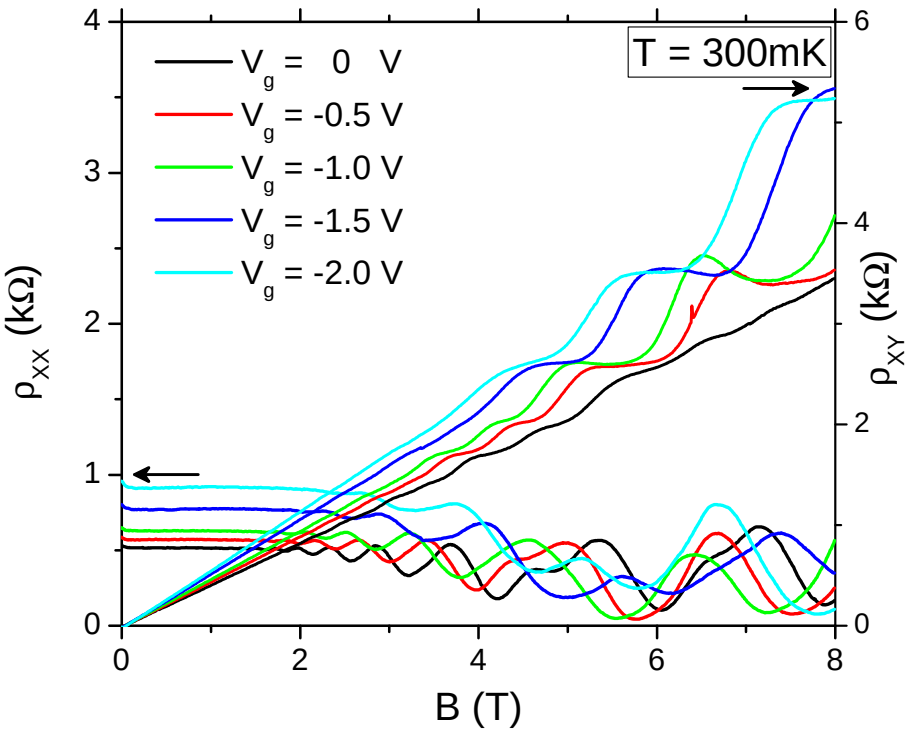


Figure 3.17: Longitudinal resistance ρ_{XX} and Hall resistance ρ_{XY} vs. magnetic field at T = 300 mK, with an applied top-gate voltage V_g from 0 to –2 V.

tive dielectric constant of 9.0, band gap of 7.0 eV, and conduction band offset to Si of 2.5 eV [62]. No oxide-silicon interface charge states are assumed. The calculated result is also included in Fig. 3.19. An inflection point at a gate voltage of about –1 V is predicted by the modeling. However, it is only weakly observed in the experimental data. For gate voltages larger than the threshold, our model shows that the accumulated electrons will tend to stay in the undoped Si and SiGe cap layers, so the 2DEG density in Si channel remains almost constant. Below the threshold, electrons are depleted by the gate voltage as a linear function with a slope of 3.24×10^{11} cm^{-2}/V, or an equivalent capacitance of 0.052 μF/cm^2. The predicted capacitance between the gate and channel is estimated to be 0.068 μF/cm^2, by using ideal parallel plates

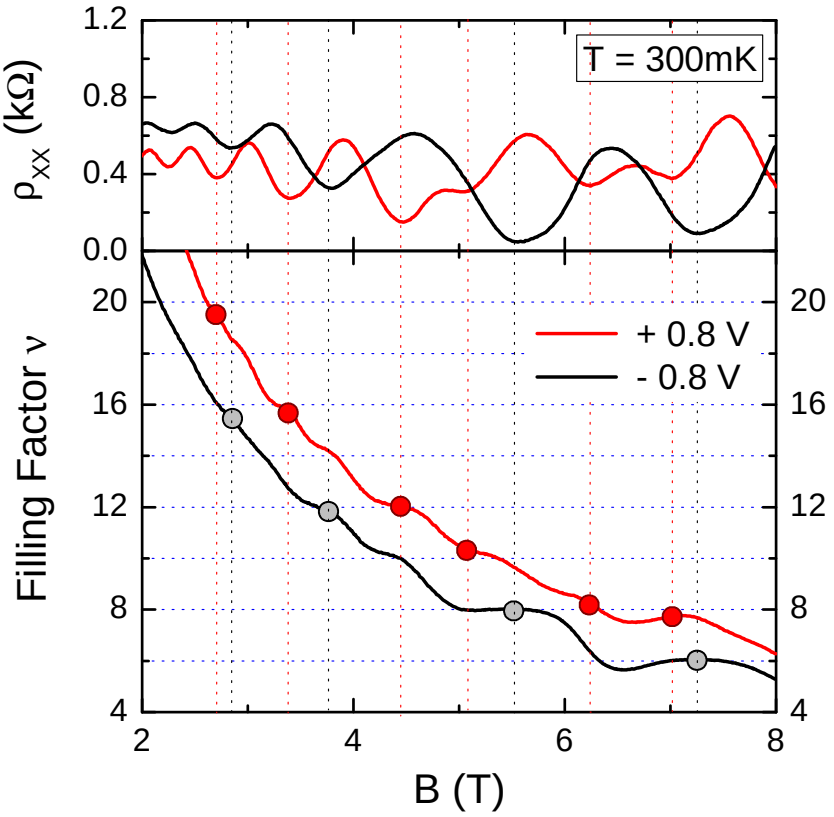


Figure 3.18: Shubnikov-de Hass oscillations and quantum Hall effect at integer filling factors at T = 300 mK, with applied top gate voltages of +0.8 and –0.8 V.

separated by 90 nm Al_2O_3 and 40 nm $Si_{0.7}Ge_{0.3}$.

Due to the high initial electron density, the 2DEG density remained in the low 10^{11} cm^{-2} range even with a high negative gate voltage ($\sim$ –4 V) applied. The channel resistivity was in the insulating regime ($\rho > h/e^2$) with such high voltages as the mobility decreased fast.

In conclusion, we have demonstrated Al_2O_3 as an excellent gate dielectric for modulation of electron density in a Si/SiGe 2DEG. The electron density can be depleted linearly by applying a negative gate voltage. Neither gate leakage nor hysteresis in either direction was observed.

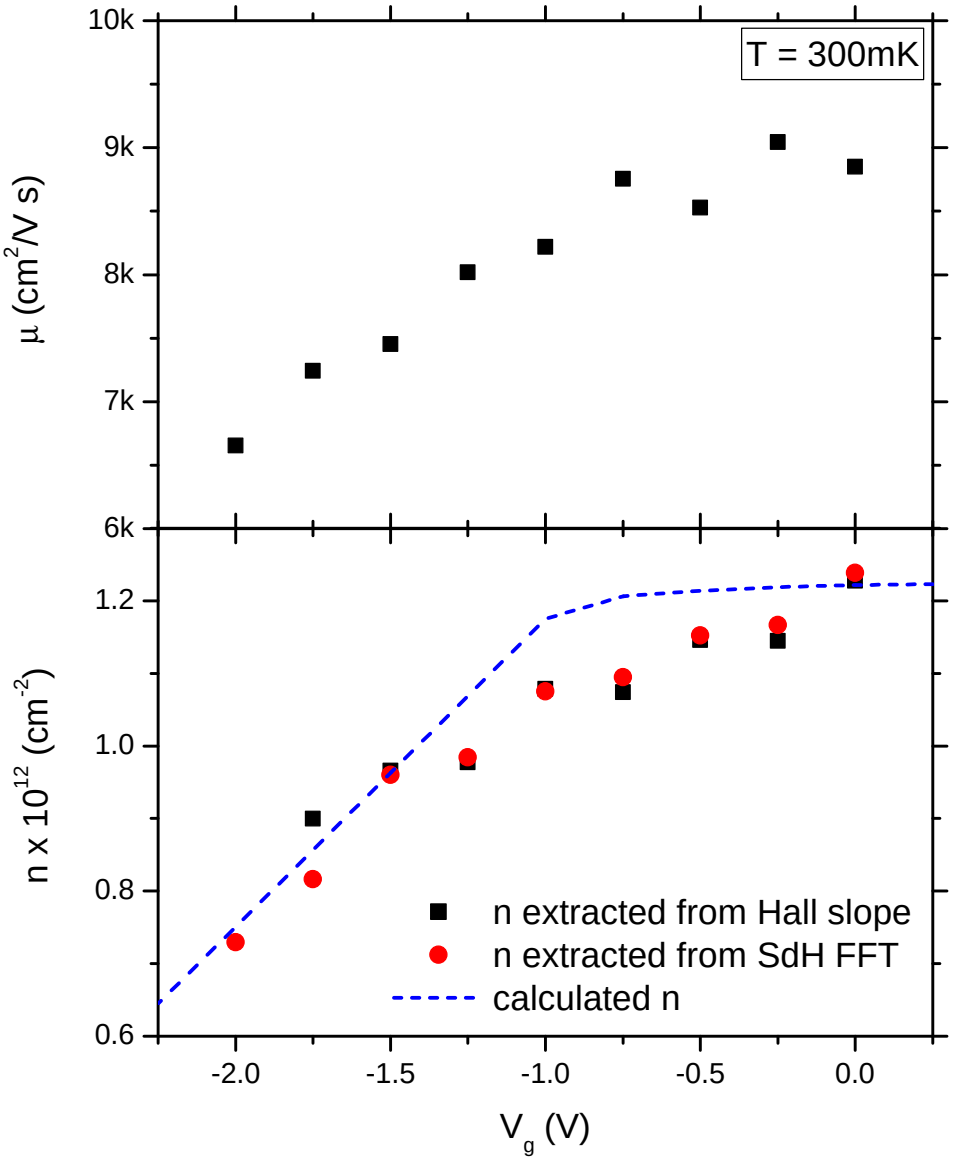


Figure 3.19: 2DEG density and mobility vs. applied gate voltage at T = 300 mK. Three methods for extracting the electron density are plotted: from Hall slope, from SdH oscillation period, and from solution of 1-D Poisson's equation.

3.5 Summary

Band engineering with modulation-doped Si/SiGe heterostructures enables the realization of two-dimensional electron gases, which has been the primary vehicle for research on semiconductor based quantum computing. In such systems 2-D electrons are trapped in a quantum well formed at the heterojunction, in which the low temperature mobilities are limited by Coulombic scatterings or interfaces rather than phonons.

High quality 2DEG's have been successfully employed on both 20% and 30% Ge commercially available relaxed buffers. Electron mobility around 10,000 cm^2/Vs is achieved. We first studied the electrostatics to get estimates of band diagrams as well as electron densities. Then we calculated the mobility of a 2DEG by considering the screening from Coulomb interactions. High background phosphorus impurity levels are our current mobility limiting mechanism. Several methods for improving the mobility have been proposed.

Electron spin resonance provides an accurate way to study the g-factor in the Si/SiGe 2DEG systems. The g-anisotropy in external magnetic fields can be tuned by adding a small amount of Ge into the Si channel, which can provide a mechanism to manipulate electron spins. Growth of such 2DEG with up to 5% Ge is demonstrated.

Finally we developed an experimental technique to implement ALD oxide as gate dielectrics on the modulation-doped heterostructures. As an example, ALD Al_2O_3 can be deposited at low temperature with digital thickness control. The 2DEG in the depletion regime with negative gate voltage applied showed well-behaved density tuning with negligible leakage current. The successful modulation of Si/SiGe 2DEG opens up new ways to explore low dimensional physics as well as device applications in previously inaccessible regimes.

Chapter 4

Parallel Two-Dimensional Electron Gases in Double Quantum Wells

4.1 Introduction

2DEG systems in semiconductors have been an incubator for both new physics and revolutionary technologies. Considering the many breakthroughs in single quantum well 2DEG's, it is quite natural to extend the study towards double or multiple quantum well systems. The additional degree of freedom results in rich physics not present in a single-layer system. One recent prominent example is the quantum cascade laser (QCL) [63]. One-dimensional multiple quantum well confinement in QCLs leads to the splitting of the band of allowed energies into a number of discrete subbands, which makes possible a population inversion between two subbands. Although QCLs were first fabricated in the III-V semiconductor systems, the intersubband transitions are independent of the relative electron and hole momenta across the bandgap, thus can be applied to indirect semiconductor systems such as silicon as well. Since the first Si/SiGe quantum cascade emitter was demonstrated in 2000 [64], Si/SiGe laser has been an active research topic.

A double quantum well (DQW) incorporating a 2DEG in each quantum well is among the simplest structures exhibiting significant interaction effects between two layers of 2DEG's. For example, one of the observed phenomena, which is directly related to the wave nature of electrons, is the wave-function coupling between two closely spaced parallel 2DEG's [65]. When the interlayer separation is comparable to the intralayer distance of the individual electrons in each 2DEG, interlayer Coulomb interactions are then just as important as intralayer ones and the system allows collective phases that do not exist in the individual layers. DQW systems in GaAs/AlGaAs heterostructures have been widely studied both theoretically and experimentally. Many fascinating new physical properties are reported, these include: quantized Hall effect (QHE) when electrical currents flow in parallel through the two wells [66], a giant enhancement of the zero bias interlayer tunneling conductance [67, 68], the vanishing of both the longitudinal and Hall resistances when equal but oppositely directed currents flow in the two layers [69, 70], and much more.

No experiments on DQW systems in Si/SiGe heterostructures exist to our best knowledge. It is the purpose of this chapter to study such DQW systems. Not only because they are as promising for the study of many-body physics as those already demonstrated in the III-V systems, but also because they are potential building blocks for quantum information processing, or in other words, the "Lego block" of our silicon-based quantum computer.

Let us consider the Loss-DiVicenzo proposal again. In their scheme the spin of single electron confined in quantum dot is used as qubits. Single-qubit operations can be achieved by local magnetic fields or g-factor engineering. Two-qubit operations are based on interactions resulting from exchange coupling (J) between adjacent qubits. Fig. 4.1 shows the interaction between two single-electron dots. When J is large, the two wavefuctions will overlap so operations such as swap can be performed. Such a quantum device involving two-qubit interactions is also referred as a quantum dimer.

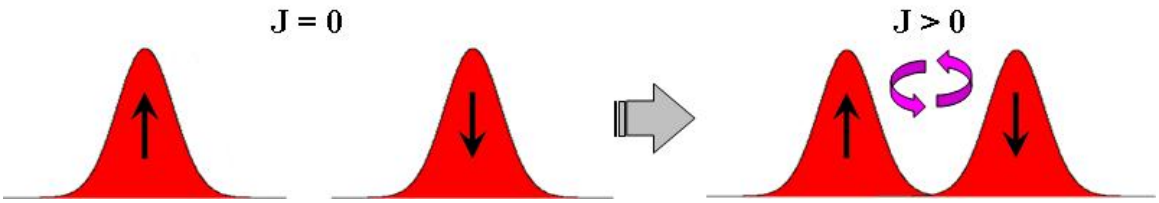


Figure 4.1: Exchange interactions between two spin qubits: when J = 0, the two qubits are uncoupled; when J > 0, the two qubits are coupled and two-qubit operations can be performed.

The conventional method to realize spin exchange coupling is to use double quantum dot. Fig. 4.2 (a) shows such a double quantum dot device. Two quantum dots are connected to each other, and their coupling is controlled by two lateral finger gates. The strength of the interaction depends on the gate voltages and is very sensitive to the gate voltage noise. Quantum-gate mechanisms in double quantum dot were studied extensively [71, 72]. However, experiments were not feasible until very recently [73]. Alternatively, if we could grow and fabricate quantum dots based on DQW systems, a quantum dot dimer would need only one dot that contains two parallel 2DEGs, as shown in Fig. 4.2 (b). It potentially offers a much neater design. In addition, our epitaxial regrowth technique (see Chapter 6 for a complete discussion) can provide 3-D confinement to both qubits and dimers and reduce the number of gates. The exchange interaction depends only on the growth structure hence is better controlled. Ideally each qubit/dimer requires no gate. An overall top gate is only needed to balance the two well densities in the dimer if they are different.

In collaboration with Professor Leonid Rokhinson's group, our group is among the first to propose the use of Si/SiGe DQW for silicon-based quantum computers [74]. It enables a scalable architecture for semiconductor-based quantum computing. We call it the "flying qubit" architecture, in a sense that electrons are physically shuffled in real 3-D space other than sitting in 2-D channels. Fig. 4.3 depicts this idea. Controllable parallel 2DEG's in Si/SiGe DQW systems are used as the interaction dimers and form the backbone in such an architecture.

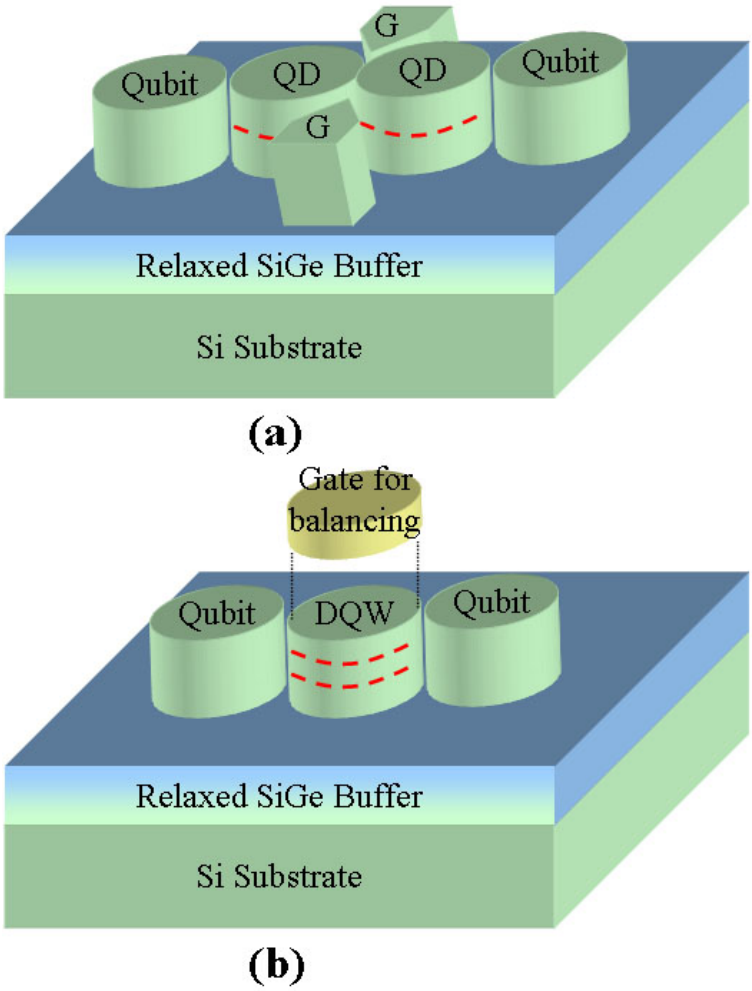


Figure 4.2: Schematic view of two quantum dimer fabrication schemes: (a) a coupled double quantum dot, the exchange coupling is controlled by two side finger gates; (b) a single quantum dot of double quantum wells, the exchange coupling is controlled by primarily the as-grown structure of the DQW and not by a gate voltage.

4.2 Modeling of the Double Quantum Well Systems

4.2.1 Design of Double Quantum Well Systems

In the following section we will study two types of DQW system design. The first design has two asymmetric quantum wells with doping supply placed only on one side. In the second design, the two quantum wells are symmetric with the same

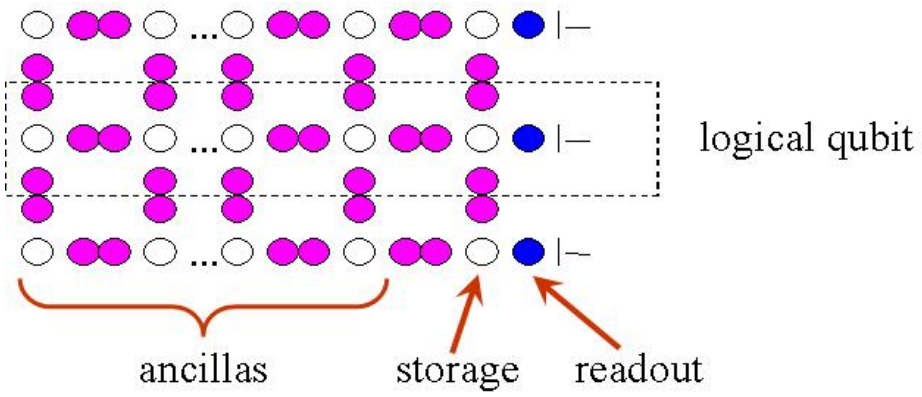


Figure 4.3: The "flying architecture" map for a quantum computer. Each qubit (white circle) is coupled to four identical qubits in the array via a quantum dimer (adjacent pink circles).

doping supply and spacer layers from both sides. Fig. 4.4 shows the detailed layer structures that will be studied. No silicon cap is added to avoid parasitic effects in band calculation due to the extra quantum well at the surface. In the asymmetric design, it is necessary to make the top quantum well thinner so that more carriers can be transferred to the bottom well for balancing the electron densities in the two 2DEG channels.

For the band diagram and electron density calculation, we used the same program and material parameters that were presented in Chapter 3. To include the quantum mechanics effects, we solved both the Poisson and Schrödinger equations self-consistently in the DQW region. Considering the simple one-dimensional scenario, the underlying equations to find the conduction band and electron states are:

$$-\nabla \cdot \epsilon_s(x)\nabla\phi(x) = -\frac{\partial}{\partial x}\epsilon_s(x)\frac{\partial}{\partial x}\phi(x) = q\left[N_D(x) - n(x)\right], \tag{4.1}$$

$$-\frac{\hbar^2}{2}\nabla \cdot \frac{1}{m^*(x)}\nabla\psi(x) + V(x)\psi(x) = -\frac{\hbar^2}{2}\frac{\partial}{\partial x}\frac{1}{m^*(x)}\frac{\partial}{\partial x}\psi(x) + V(x)\psi(x) = E\psi(x), \tag{4.2}$$

where ϕ is the electrostatic potential, ϵ_s is the dielectric constant, N_D and n are the ionized donor and electron concentrations, ψ is the wave function, E is the energy,

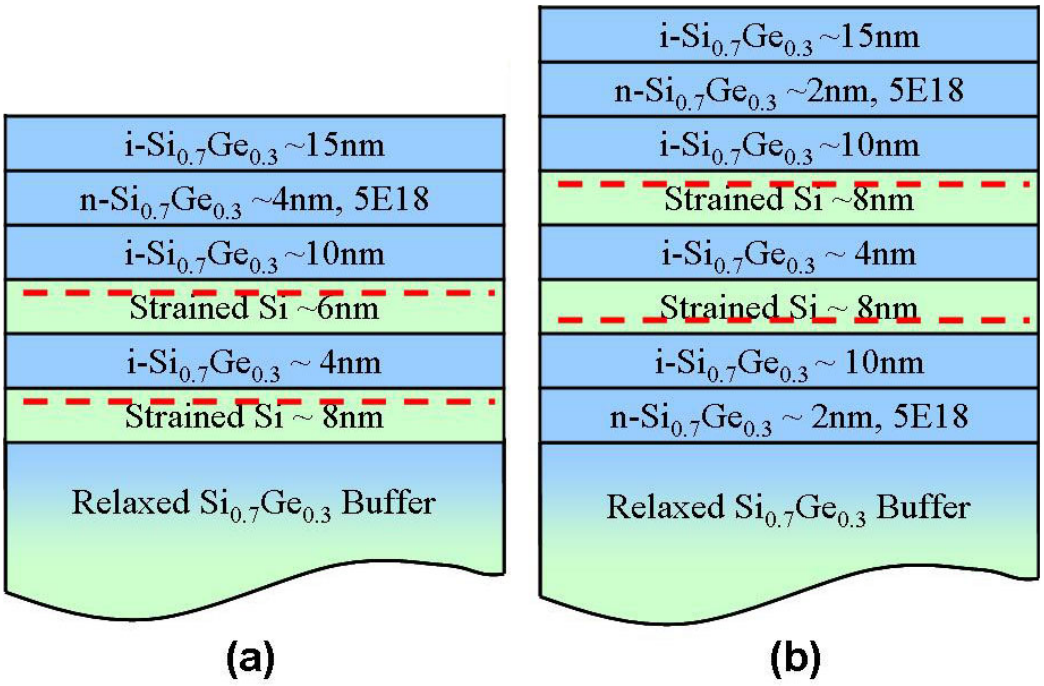


Figure 4.4: Schematic view of layer structures of two double quantum well systems: (a) asymmetric DQW with only one supply layer, (b) symmetric DQW with double supply layers. The red dashed line indicates a 2DEG.

and V is the potential energy, which is simply equal to the conduction band energy. The above two equations are related by:

$$V(x) = V_{CB}(x) + \phi(x), \tag{4.3}$$

$$n(x) = \sum_{k=1}^{m} \psi_k^*(x)\psi_k(x) \times \int_{E_k}^{\infty} \frac{\sqrt{2m^*}}{\pi\hbar\sqrt{E - E_k}} \left[\frac{dE}{1 + exp(E - E_k/kt)}\right], \tag{4.4}$$

where V_{CB} represents the conduction band edge potential at zero doping, the electron density is calculated by the summation over all the subbands from solving equation (4.2).

In all the following calculations, SiGe refers to $Si_{0.7}Ge_{0.3}$. For simplicity, a moderate level of 5×10^{16} cm^{-3} background doping of phosphorous is assumed in all grown Si and SiGe layers. The temperature is T = 4 K.

4.2.2 Asymmetric Double Quantum Wells

The first structural design contains two asymmetric quantum wells with doping supply from the top. The top channel is very thin to compensate for the fact that it is closer to the supply layer, in an effort to balance the electron densities in the two wells. The structure shown in Fig. 4.4 (a) is used for calculation. The Schrödinger equation is used between depth 50 Å and 800 Å from the top, outside this region only the Poisson's equation is solved assuming Boltzmann statistics. The model and materials parameters described in Appendix B are used. The boundary condition at the top surface is defined by a barrier height between the Fermi level and the conduction band $V_{Schottky} = E_f - E_c$. Fig. 4.5 shows the electron densities in each quantum wells and the total density with different barrier height.

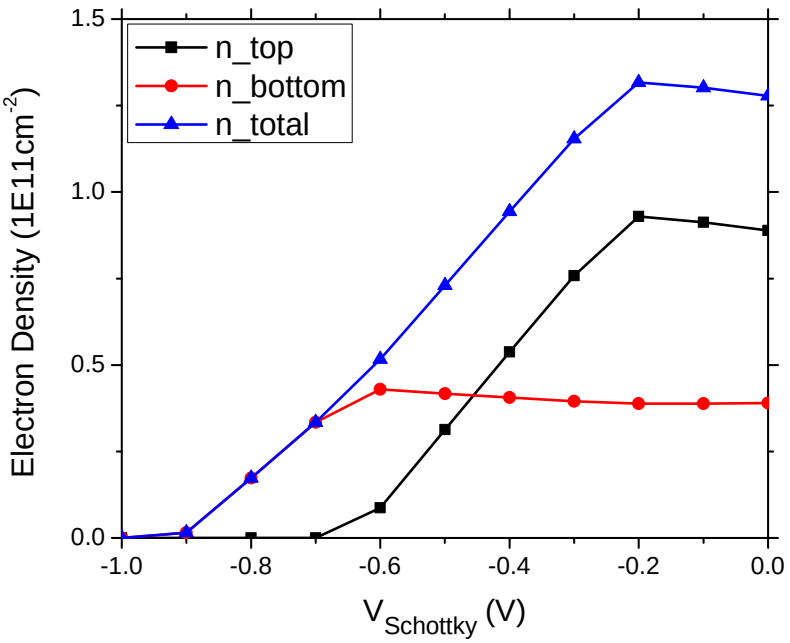


Figure 4.5: Electron densities in asymmetric DQW system with different surface Schottky barrier height applied.

The calculation shows that the balance of the two 2DEG densities occurs when the

surface Fermi level is at mid-gap with $V_{Schottky} = -0.45$ V. In the accumulation region the density in the bottom well remains fairly flat, only the density in the top well increases with more applied positive voltage. When the Fermi level at the top surface is raised close to the conduction band ($|V_{Schottky}| < 0.2$ V), the electron density in the DQW saturates. Further increasing the Schottky voltage will populate electrons only into the top SiGe layers outside the quantum wells. In the depletion region, after the top well is completely depleted, the density in the bottom well decreases at a slower rate, as a result of the larger spacing between the bottom 2DEG channel and the top gate.

Fig. 4.6 shows the band alignment diagrams for when the double well densities are balanced ($V_{Schottky} = -0.45$ V) and when the top quantum well is depleted ($V_{Schottky} = -0.8$ V). Since we are only interested in electrons, for simplicity only the conduction band edge is plotted. The Fermi level deep in the substrate buffer layers is pinned close to the conduction band edge due to background impurities, so the band alignment in the bottom well only varies a little compared to the dramatic change in the top well. Adding back-gating should greatly help to adjust the band alignment in the bottom well and keep the double well electron densities balanced at any total density level.

4.2.3 Symmetric Double Quantum Wells

The symmetric double quantum wells require two parallel 2DEG's with identical spacer and supply layers. Although conceptually simple, it can be very difficult for growth control due to the out-diffusion of dopants from the bottom supply layer towards top layers, which not only reduces the effective spacer thickness of the bottom well but also can cause increased background impurity doping.

The calculated electron densities are shown in Fig. 4.7. The Schrödinger equation is used in the region between 50 Å and 1000 Å from the top in the structure (Fig. 4.4 (b)). Since the bottom well has its own supply layer from the substrate side,

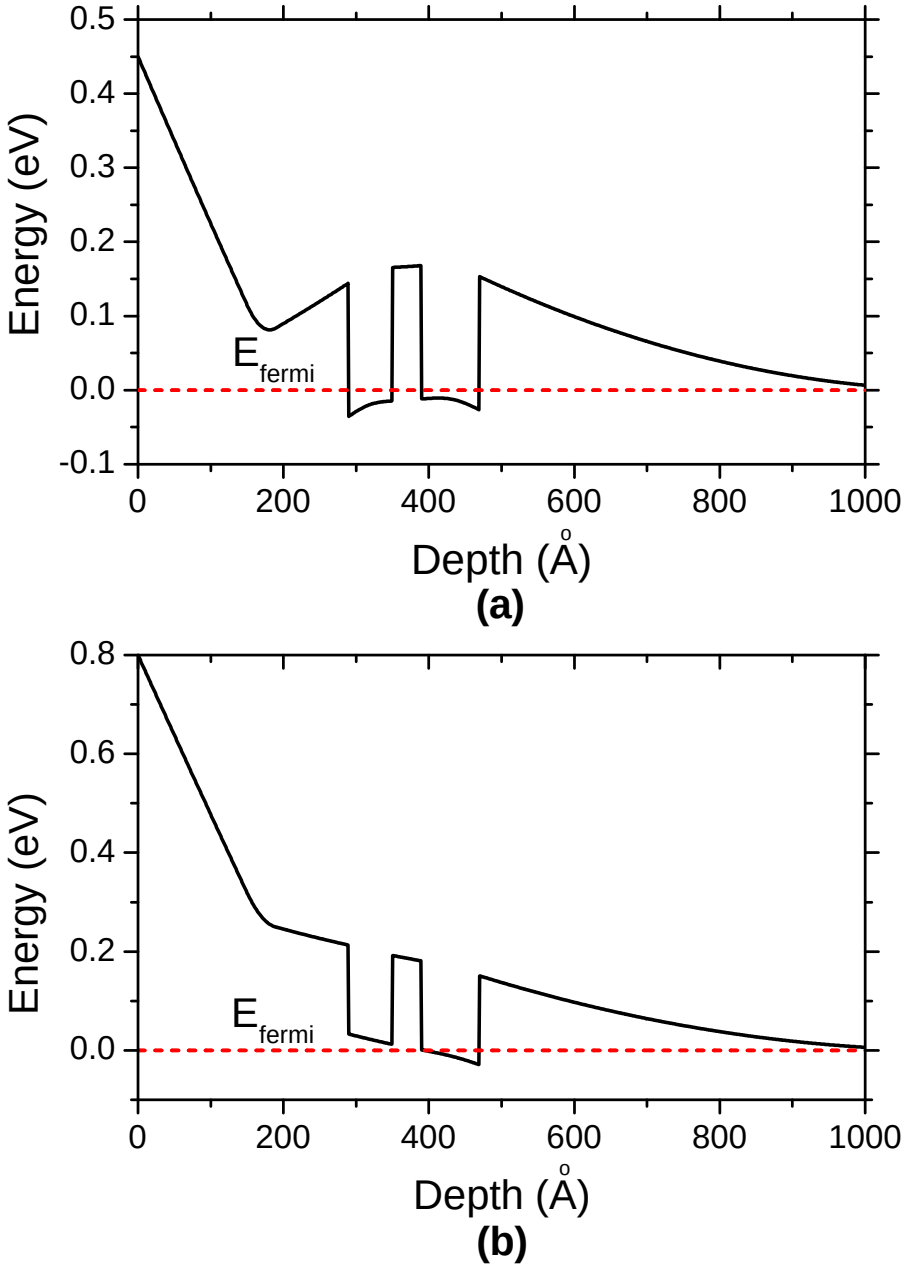


Figure 4.6: Conduction band diagrams in asymmetric DQW design with surface potentials at (a) $V_{Schottky} = -0.45$ V, (b) $V_{Schottky} = -0.8$ V.

the DQW band alignment should be symmetric when no surface Schottky barrier is applied and the electron densities in the two quantum wells are balanced. The top well is completely depleted when the surface Fermi level is at mid-gap with around $V_{Schottky} = -0.5$ V. The carriers in the bottom well are depleted much slower when more negative Schottky barrier is applied. There are still some electrons left in the bottom well ($\sim 0.5 \times 10^{11}$ cm^{-2}) even when $V_{Schottky}$ is as high as –1 V. In the accumulation region, the densities in the DQW remain almost balanced over a wide range as long as the top surface potential is close to conduction band edge. No more electrons are added to the DQW when the surface barrier passes the conduction band edge ($V_{Schottky} > 0$), and the density in top well cannot be tuned to much higher than that in the bottom well.

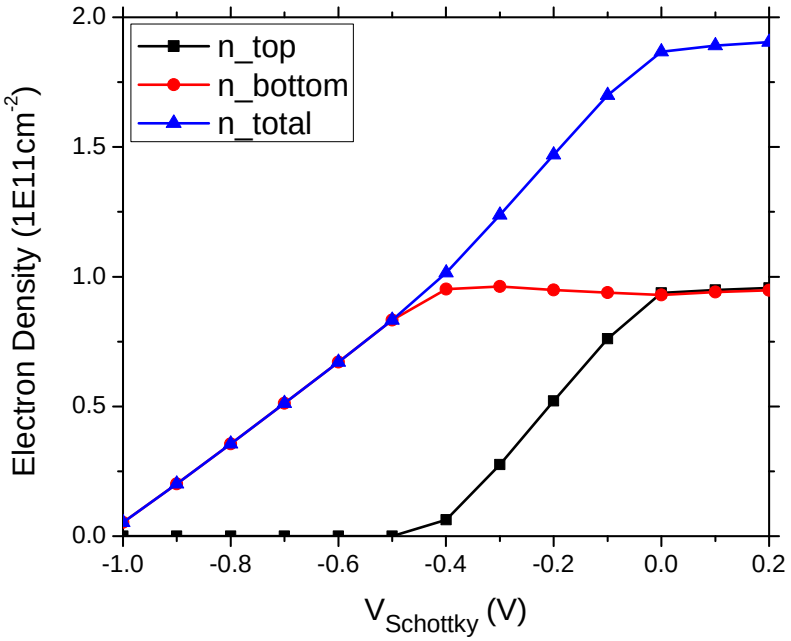


Figure 4.7: Electron densities in symmetric DQW system with different surface Schottky barrier heights applied.

We choose $V_{Schottky} = 0$ and $V_{Schottky} = -0.8$ V to check the energy band alignment

for balanced and depleted DQW, as shown in Fig. 4.8. Compared with the band alignment in the asymmetric DQW system, the Fermi level in the layers below the bottom well converges to the conduction band more quickly due to the bottom supply layer. Therefore without back-gating it is even more difficult to tune the density in the bottom well.

A very important feature of the symmetric DQW system is the symmetric and anti-symmetric split behavior. We can show this by calculating the lowest two quantized states assuming a flat-band condition with no dopants. Fig. 4.9 shows the wave functions of such lowest two quantized states. Clearly there is a large tunneling coupling between the two wells. In fact, the quantized states are no longer stationary states, they form symmetric and anti-symmetric subbands which are characterized by the energy gap Δ_{SAS}. The symmetric subband is of lower energy. This is directly analogous to the formation of a pair of bonding and anti-bonding orbitals in a hydrogen molecule. For the separation of 4 nm between the two silicon quantum wells in our model, our calculation predicts a $\Delta_{SAS} = 0.1$ meV, which is comparable to typical values of 0.1 - 1 meV measured in III-V compound semiconductor systems [75].

4.2.4 Comparison of Double Quantum Well Schemes

So far we have calculated the conduction band alignment, 2DEG densities and electron subband structures for both asymmetric and symmetric DQW schemes. The density balance of the two 2DEG channels can be achieved and controlled through a variable electric field induced by top-gating. A back gate is desirable to adjust band alignment below the bottom well and to allow independent control of electron densities in the two wells.

The asymmetric double quantum wells using only one top supply layer are easier to grow. This design offers a wider range of electron density in the top well that

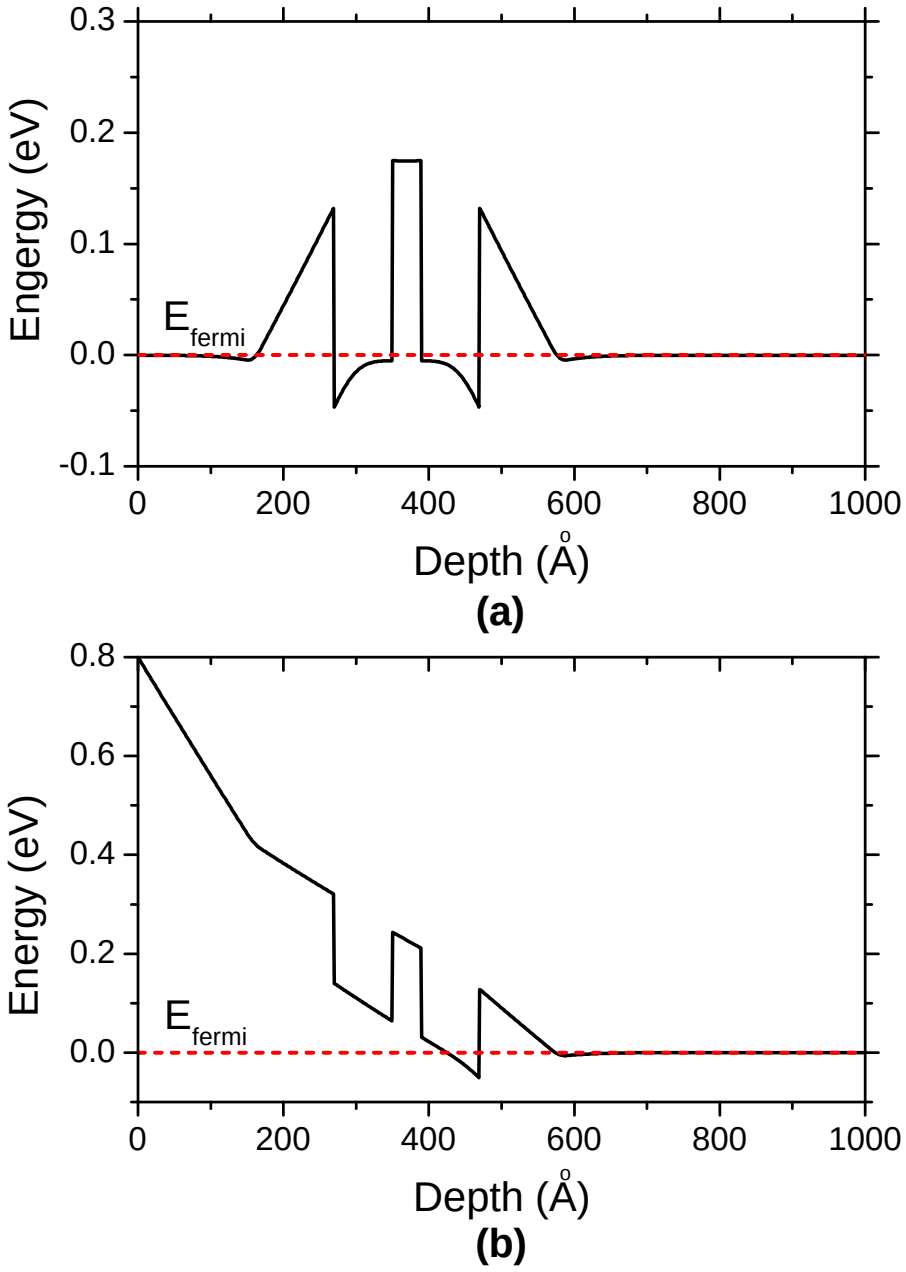


Figure 4.8: Conduction band diagrams in symmetric DQW designs with surface potentials at (a) $V_{Schottky} = 0$, (b) $V_{Schottky} = -0.8$ V.

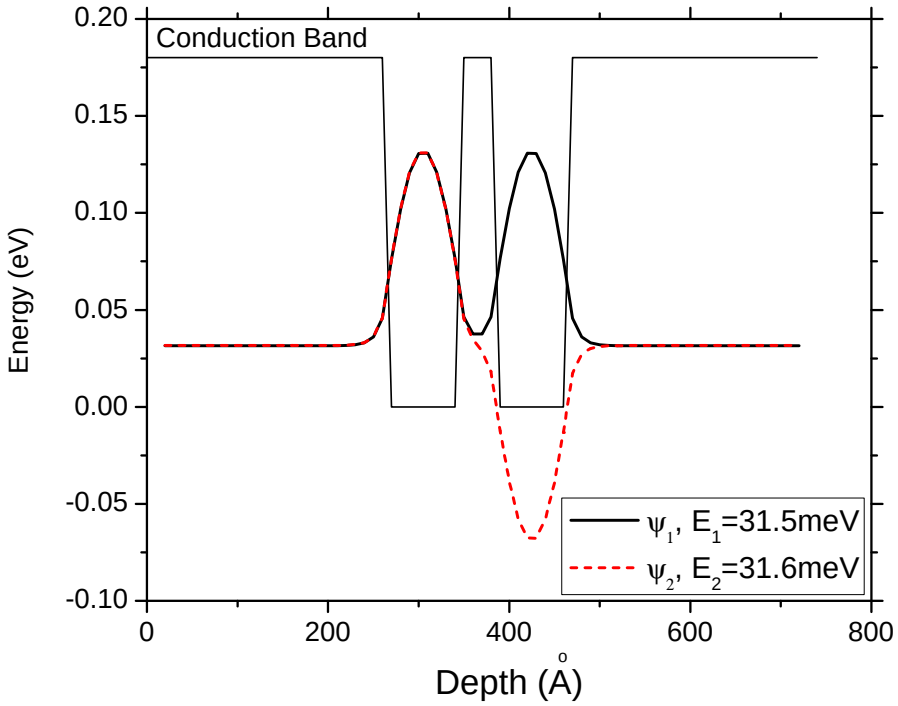


Figure 4.9: The conduction band edge and the electron wave functions of the lowest two quantized states in the symmetric double quantum well structures. The strained Si conduction band is at V = 0.

can be tuned by top-gating. However, the exact band alignment below the bottom well is very sensitive to the background impurities and substrate doping, making the accuracy of predetermination of density in the bottom well very poor. Since the structure is asymmetric, we cannot directly compute the symmetric anti-symmetric splitting as in the symmetric double well case. We expect the strength of subband interaction is similar to that in the symmetric double well given their similar quantum well width and same tunneling barrier thickness.

For the symmetric double quantum wells with two supply layers, our calculation shows the presence of symmetric and anti-symmetric pairs in the two-level system. The splitting Δ_{SAS} is a fraction of 1 meV which indicates a weak interaction, but it should also depend largely on the tunneling barrier thickness, doping level and

other growth parameters. The main drawback of the symmetric design is the tail of dopant out-diffusion and perhaps increased background impurities level from the bottom doping supply layer during the growth.

4.3 Characterization of the Double Quantum Well Systems

4.3.1 Growth of Si/SiGe Double Quantum Wells

We first attempted to grow an asymmetric double quantum well on our relaxed SiGe buffers. Sample #4692 has the same layer structures as shown previously in Fig. 4.4 (a) with an additional 4-nm thick silicon cap. Sample #4652 has a thicker SiGe barrier of 8 nm for SIMS analysis. The most critical technology issue is the abruptness and flatness of Si/SiGe/Si interfaces in the active DQW region. Since the barrier between the two strained silicon channels is only 4 nm or thinner, a growth rate of no more than 10 nm/min is desirable for improved abruptness and flatness.

Fig. 4.10 shows the Ge profile in sample #4652. The two thin silicon wells are clearly present. The Ge slope at all Si/SiGe interfaces is about 7% Ge per nm, which may be the SIMS limit. There are no fluctuations in oxygen and carbon profiles during these switchings. The rising end at the top surface is a pure SIMS effect.

Fig. 4.11 shows a cross section TEM image of the asymmetrical DQW sample. The clear contrast between the Si and SiGe layers demonstrates abrupt Si/SiGe interfaces with fluctuations on the order of a few Å. From the high resolution image (b) we also confirmed that the top quantum well is narrower than the bottom well. The thickness of both Si channels are about 2 nm less than the nominal values. Since the overall growth was mostly maintained at 625 °C for epitaxial SiGe, when the samples were heated to 700 °C or 750 °C for Si epitaxy, the temperature fluctuated for about

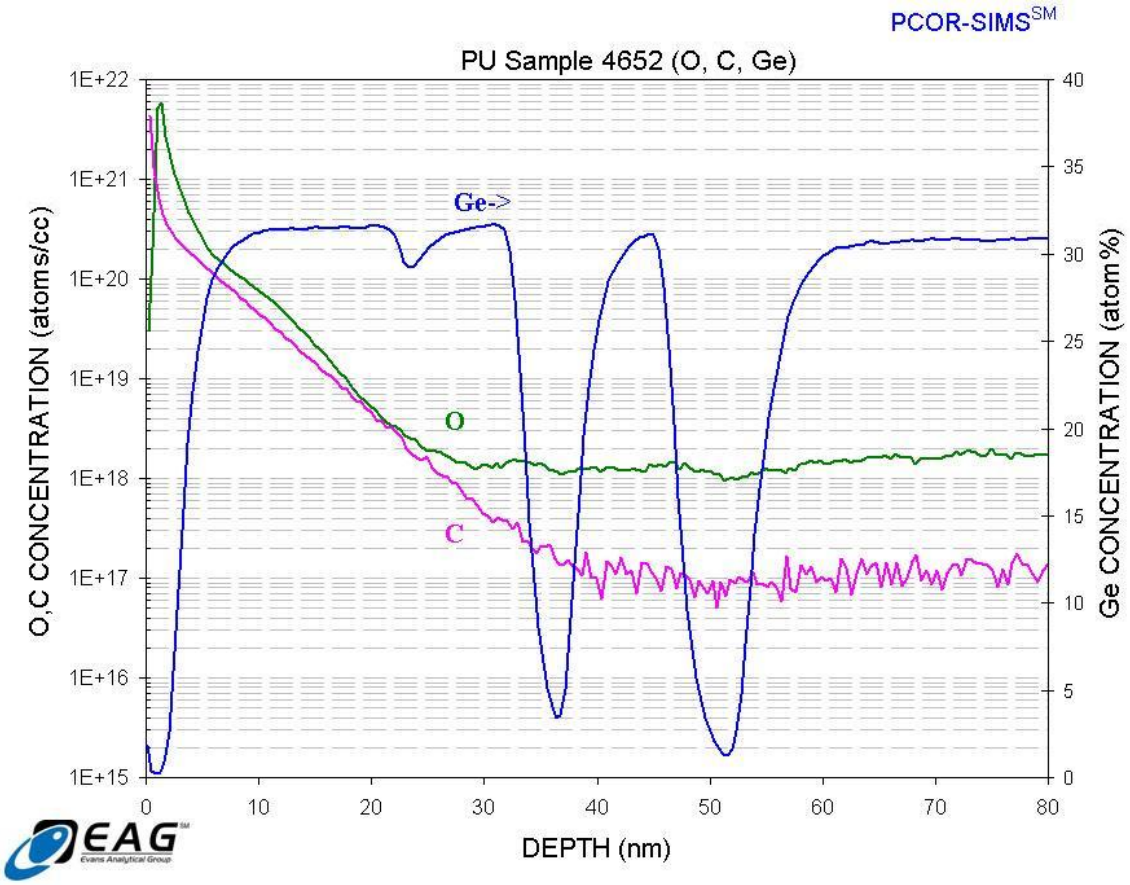
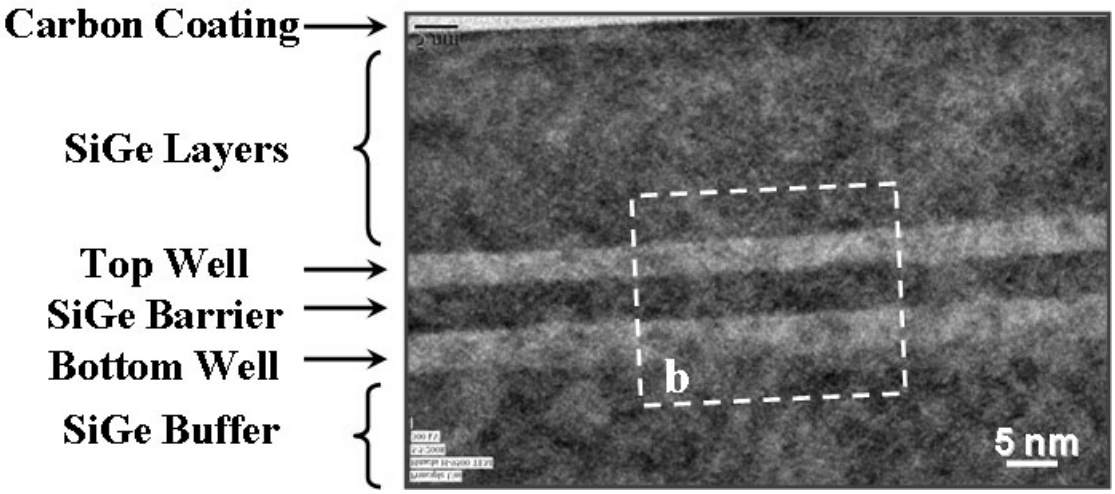


Figure 4.10: SIMS analysis of an asymmetric double quantum well structure with a 8nm barrier between the two wells.

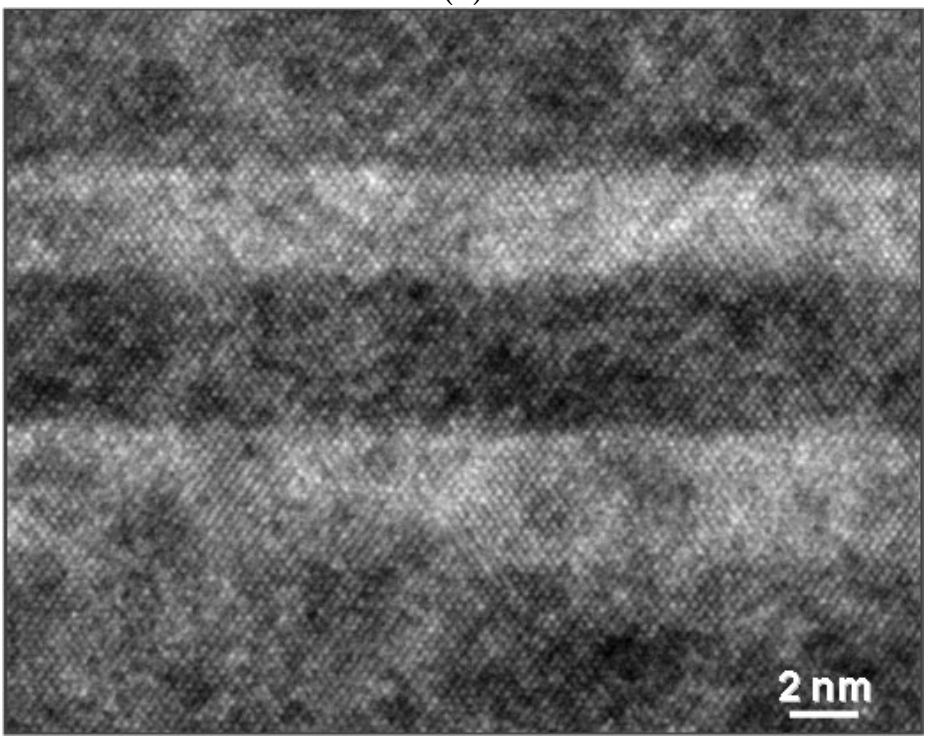
10 seconds when switching to these higher temperatures. This could cause a slower initial growth rate. Since the growth time was based on the steady-state growth rate of these layers, we naively did not allow for this transition time. We could take this into account in future growth design and compensate simply by increasing the growth time for thin silicon layers on top of SiGe.

4.3.2 Modulation of Si/SiGe Parallel Two-Dimensional Electron Gases

There are three types of experimental techniques that are commonly used to study the band structure and interactions between layers in double quantum wells. First a



(a)



(b)

Figure 4.11: (a) A cross section TEM image of an asymmetric double quantum well structure on $Si_{0.7}Ge_{0.3}$ relaxed buffers. (b) A high resolution TEM image showing the Si/SiGe/Si double quantum wells. The TEM was prepared by Dr. Nan Yao at Princeton and Hitachi laboratory, CA.

prominent negative transconductance was observed in the channel conductance characteristics due to resistance resonance [76, 77]. The second and also the most powerful tool is the Shubnikov-de Haas (SdH) oscillations originating from the sequential passage of Laudau levels through the Fermi level in external magnetic field. The intersubband transitions in DQW altered the SdH oscillations substantially and caused beating due to the mixing of the symmetric and anti-symmetric states [78, 79, 80]. A relatively new technique is to study the microwave induced absorption between the subbands. One recent example was interference oscillations of microwave photoresistance in GaAs/Al_xGa_{1-x}As/GaAs double quantum wells [81]. However, to the best of our knowledge, none of these effects were observed and reported in Si/SiGe systems.

The negative transconductance effect was observed in a Si/SiGe asymmetric double quantum well sample #4822. The sample has the same structure parameters as #4692 we described before, and an Al metal gate on top of 72-nm ALD Al_2O_3 was deposited for gating. The usual MOSFET structure with a Hall bar geometry was measured at T = 4.2 K and below. Both I-V and magneto-transport measurements were performed through collaboration with Professor Leonid Rokhinson's laboratory at Purdue University. The channel conductance G of the FET is shown in Fig. 4.12. A valley feature with negative transconductance is seen between $V_g = -2$ and –1 V.

In the following we will try to qualitatively explain these unusual characteristics. The measured conductance can be divided into three regions as labeled in the figure. In region I, G increases monotonously with V_g, which can be attributed to the increase of electron density in the bottom well. In this region no electrons were populated in the top well as shown in our previous theoretical calculations (see Fig. 4.5). In region III, G also increases which is mostly due to the increase of electron density in the top well, while the bottom well density remains roughly constant. In region II, G drops down from 1.28 to 1.22 mS, although the total electron density should continue to increase. In this region densities in both wells increase and the delocalized

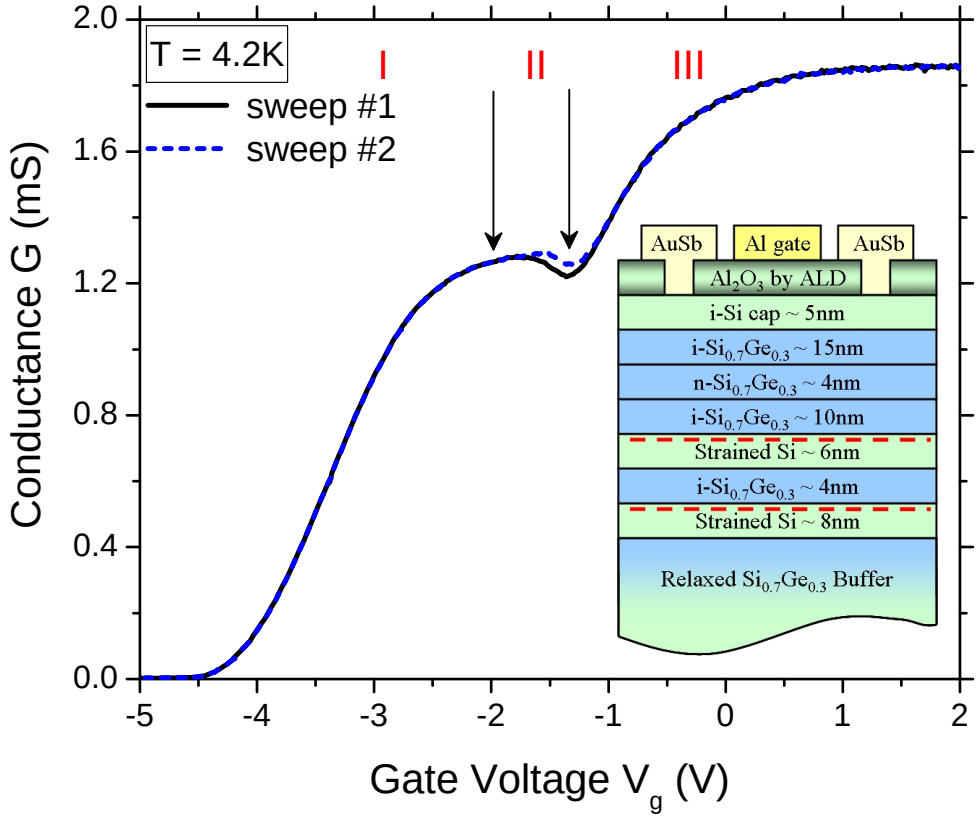


Figure 4.12: The sheet conductance measured as a function of gate voltage at T = 4.2 K.

electron wave functions interact strongly. The drop in G is influenced by the resonant coupling between two wells and the mobility modulation. The additional scattering from intersubband transitions and the alloy scattering from the thin SiGe barrier layer should decrease the 2DEG mobilities. The mobility reduction had a stronger effect on conductance than the increased total density, thus resulting in negative transconductance.

By a magnetic field dependent Hall measurement, we were able to extract the total electron density and mobility with varied gate voltage, as shown in Fig. 4.13. A substantial drop of mobility in the resonant coupling region II is clearly present. The

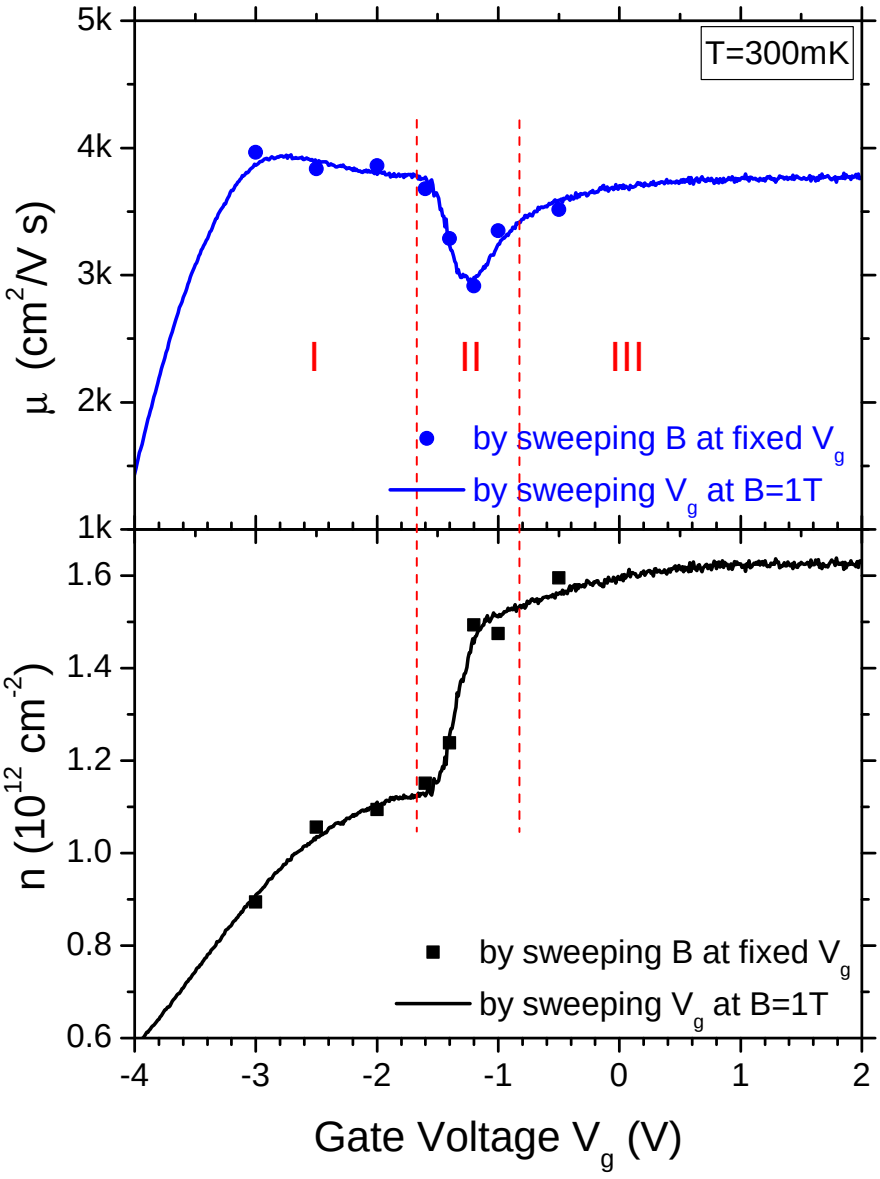


Figure 4.13: DQW 2DEG density and mobility vs. applied gate voltage at T = 300 mK. The data were extracted from Hall slope and sheet resistance by either sweeping the gate voltage at B = 1 T or sweeping the field at certain fixed gate voltages..

non-linear valley characteristics of mobility match the valley of channel conductance very well. In the same valley region we also found a sharp increase of the total electron density as a function of gate voltage. This could be explained by noting that with resonant tunneling, the two 2DEG's are coupled thus eliminating the capacitance associated with the interlayer barrier. This interlayer capacitance will manifest itself only when the two 2DEG's are decoupled. As a final note on the extracted mobility, the region III mobility is mostly due to the 2DEG confined in the bottom well, and both wells contribute to the measured mobility in region I. For the asymmetric DQW structure, the bottom well should yield a higher mobility since it has a larger effective set-back from the remote dopants. Our measurement suggests very little difference in the two mobilities, which again can be attributed to the background doping scattering as the limiting scattering mechanism for decoupled 2DEG's. On the other hand, the region II mobility can be used to evaluate the interlayer scattering strength.

Magneto-transport data were also taken at 300 mK with varied applied gate voltages, as shown in Fig. 4.14. We could not resolve any beating features in the SdH oscillations, only single oscillation period was found in FFT spectrum of ρ_{XX} magnetoresistance oscillations. We believe the missing of the SdH beating is due to the fact that the symmetric anti-symmetric splitting Δ_{SAS} in our sample could be much less than the Landau level broadening at these temperatures. We do not have direct calculation of Δ_{SAS} in asymmetric DQW structures. Our calculation for the symmetric case gives a Δ_{SAS} of 0.1 meV for a 4 nm barrier, which is rather small as our previously estimated Landau level broadening is $\Gamma \approx 0.46$ meV. No other experimental data were reported in Si/SiGe systems. We hope that a reduced background doping level and a thinner barrier would help to resolve the beating in future Si/SiGe DQW systems.

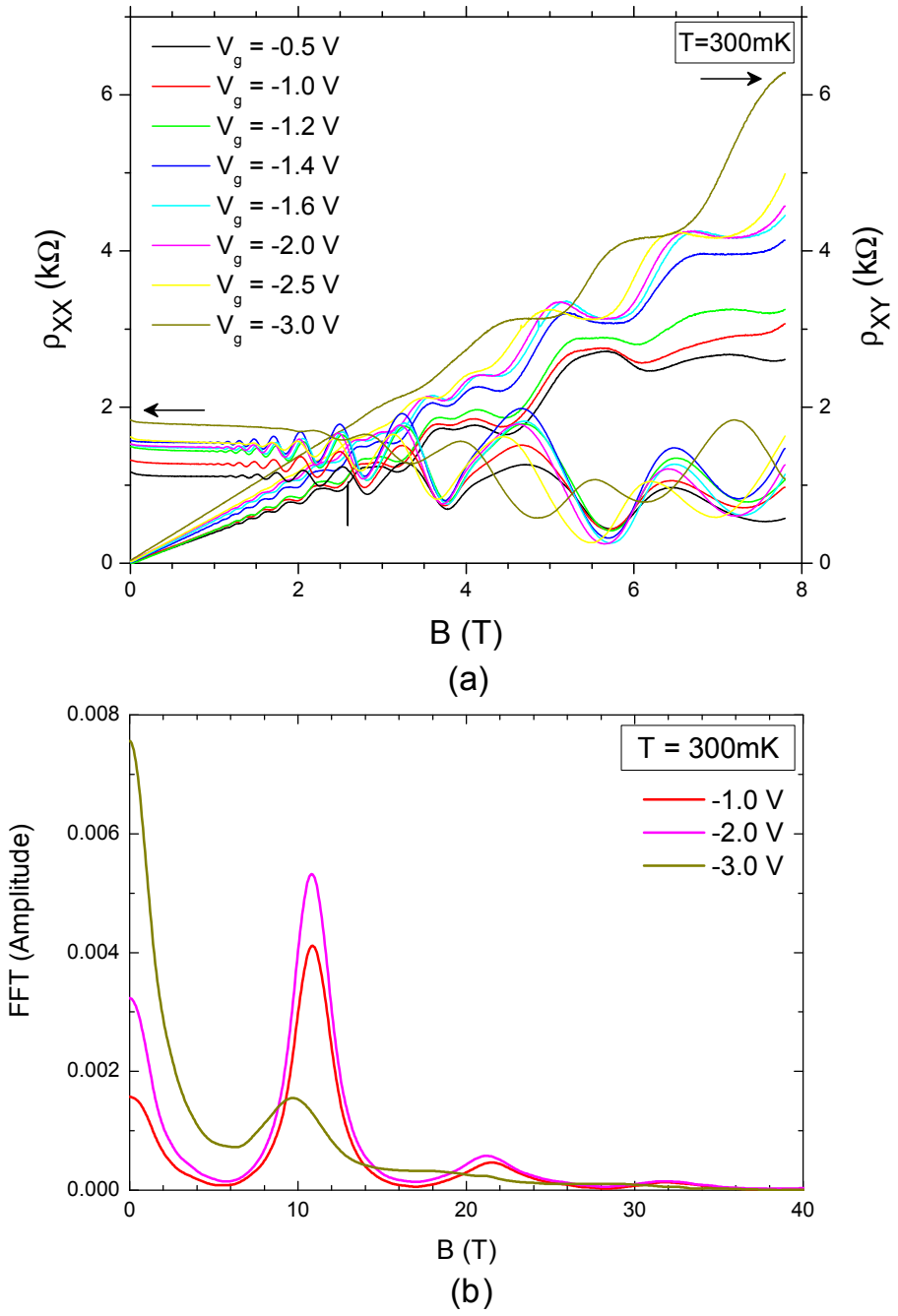


Figure 4.14: (a) Longitudinal resistance ρ_{XX} and Hall resistance ρ_{XY} vs. magnetic field at T = 300 mK, with an applied top gate voltage Vg from –0.5 to –3 V. (b) The Fourier spectrum of the longitudinal resistance at Vg = –1, –2 and –3 V.

4.4 Summary

This chapter is dedicated to the coupled double quantum well systems based on Si/SiGe heterostructures, a subject that has been extensively studied in III-V semiconductor systems but is relatively new in the Si-Ge field. Successful realization of Si/SiGe DQW systems can have a great impact on the study of many-body physics phenomenon such as electron interactions and intersubband transitions. Our emphasis of the potential applications of such DQW systems is on their role as quantum dimer for two-qubit exchange interactions in the Loss-DiVicenzo quantum computer proposal. The use of such quantum dimers allows a novel, simple "flying-qubit" architecture for silicon-based quantum computing.

Two types of DQW system designs were theoretically studied with self-consistent calculations of the Poisson and Schrödinger equations: asymmetric and symmetric double quantum wells. Conduction band alignment with different surface barrier height is calculated to determine electron density distribution in the two wells. The conditions at which the balancing of two wells can occur were obtained for both structures. For symmetric structures at balanced condition, the formation of symmetric and anti-symmetric states is shown with an energy gap $\Delta_{SAS} = 0.1$ meV. In reality, the symmetric structures are more difficult for growth control than the asymmetric structures due to the dopant out-diffusion from the bottom supply layer.

Asymmetric double quantum well growth on relaxed SiGe buffer was successfully demonstrated in the Princeton RTCVD system, with precise control of thin layer thickness and a high degree of interface abruptness and flatness. With ALD Al_2O_3 gate dielectric and top-gating, we successfully observed a negative transconductance effect in the asymmetric DQW structure as a result of resistance resonance for the first time in Si/SiGe. A substantial mobility drop is found over a region when electrons in two well delocalize and interact strongly. However, further magento-transport study of the sample did not reveal any beating of Shubnikov-de Haas oscillations. We

suggest a small energy gap Δ_{SAS}, which is less than the Landau level broadening with our sample growth and measurement conditions. Further improvement of the growth to enhance a stronger tunneling coupling between the parallel 2DEG's is needed to study the SdH beating effect.

Chapter 5

Fabrication Methods for Quantum Dot Applications

5.1 Introduction

With the improvements in techniques to relieve strain such as the relaxed buffer layers or silicon-on-insulator (SOI) substrates [82], SiGe layers grown on 300-mm-diameter scale have become available for use in research and development. Similarly, progress in the fabrication techniques for nano-device applications have seen many recent advances. The technological challenge for semiconductor quantum dot applications is to create structures as small as possible to increase the quantization energy and the charging energy of single electrons or holes. For example, it is well known that the quantization energy of electrons confined in a 1-D quantum well is inversely proportional to the square of the well width. Such devices usually require patterns with at least one lateral dimensional between the size of an individual atom and approximately a few hundred nanometers.

This work will focus on directly etching the semiconductor containing the quantum dot for side gating other than patterning a top gate to modulate the electrostatic

potential in the dot. Side gates were created in the same 2DEG layer by the same etch step that created the dot – a narrow trench separates the dot and the side gates, as shown in Fig. 5.1. In this process flow, the two most critical fabrication steps are nanolithography for defining the nanopatterns and etching for the pattern transfer. It is the purpose of this chapter to report on the development of fabrication methods that are relevant for quantum dot applications of this thesis.

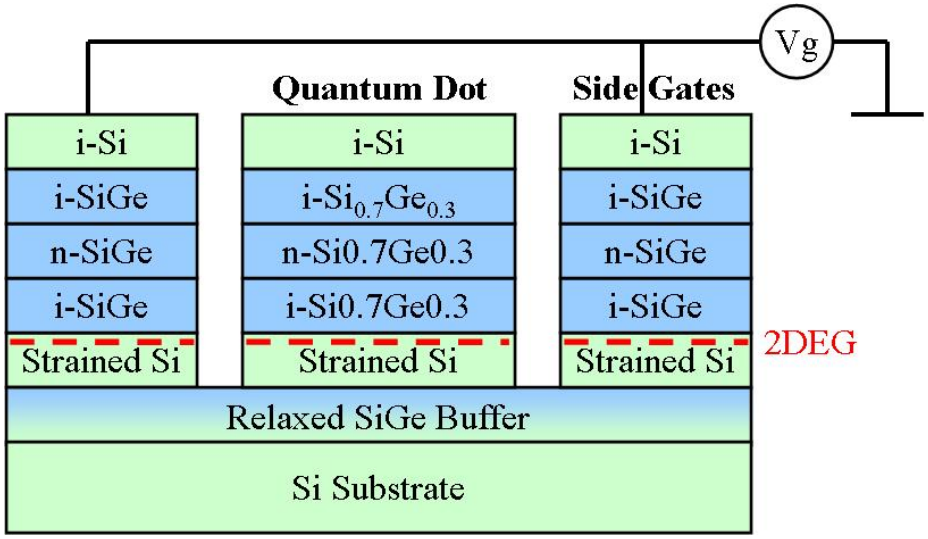


Figure 5.1: Schematic cross-section of side-gating structures for a 2DEG quantum dot.

The three popular nanolithography techniques seen in quantum dot applications are electron-beam (e-beam) lithography (EBL), scanning probe lithography (SPL) and nanoimprint lithography (NIL). EBL is the conventional nanolithography technique that is most commonly used. SPL such as atomic force microscope (AFM) lithography combined with wet etching is a novel low-energy process that can avoid radiation and etching damage thus can lead to better device surface/interface. Both EBL and AFM lithography are used in this thesis and will be discussed. NIL [83] is a promising scheme that allows high throughput and uniformity. It has two basic steps. First a mold with nanostructures on its surface is pressed into a thin resist on a substrate, followed by removal of the mold. The second step uses an anisotropic

etching process to transfer the pattern in to the entire resist.

Compared to other steps in growth and fabrication, the etching process has been a more mature technology with less new breakthrough advances. Selectivity and isotropy are considered as the two figures of merit. The two fundamental types of etchants are liquid-phase (wet) and plasma-phase (dry). Both wet and dry etching, as well as a mix of both, were used and investigated, and will be presented in this chapter.

5.2 Nanolithography Methods

5.2.1 Electron-Beam Lithography at Princeton

E-beam lithography, derived from the early scanning electron microscope (SEM), can be traced back as early as in the late 1960s. EBL is a direct-write technique that uses a beam of high-energy of electrons to produce a pattern in a resist - typically a common polymer such as PMMA (polymethyl methacrylate) [84]. The main attributes of EBL are [85]:

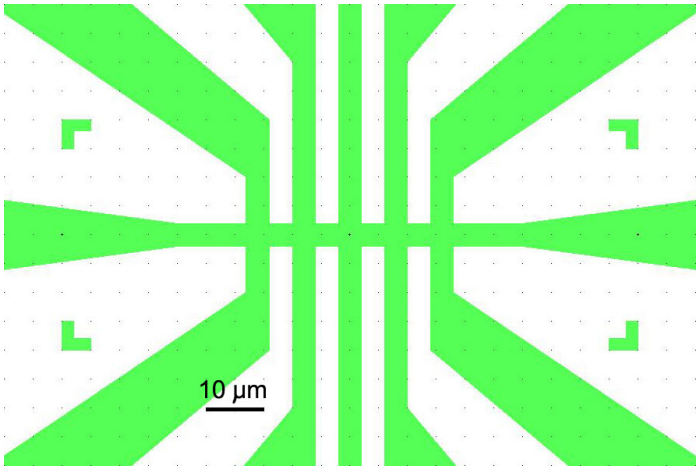
1. It is capable of very high resolution, almost to the level of a few nanometers.
2. It is a flexible technique that can work with a variety of materials and an almost infinite number of patterns.
3. It is slow, being one or more orders of magnitude slower than optical lithography.
4. It is expensive and complicated - EBL tools can cost many millions of dollars and require frequent service to stay properly maintained.

The e-beam lithography work in this thesis was all performed at Princeton in a Raith e_Line system and nanoengineering workstation by nanolithography specialist

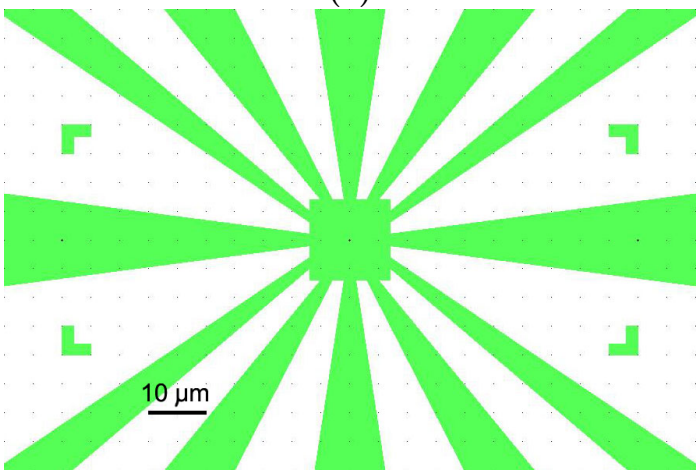
Dr. Mikhail Gaevski. The Raith e_Line uses thermal field emission filament technology and a laser-interferometer controlled stage. It is also equipped with a load lock, an automatic height sensing, and a fixed beam moving stage (FBMS). The typical column voltage is 10 kV. A typical aperture of 30 μm is used to control the e-beam current.

Before the critical dimension nanopatterns are written by nanolithography, an optical lithography step is employed to define large design features on the wafer such as contact pads and alignment marks. Fig. 5.2 shows the design view of the two active device geometries in L-Edit, Tanner EDA. In Fig. 5.2 (a) the core structure is a Hall bar, which is commonly used for quantum point contact fabrication or cutting through a conducting path for a leakage test across a gap. Fig. 5.2 (b) uses a square island with multiple contact leads which can be implemented for a variety quantum dot applications. Both active regions are small enough to fit in one writing field (typically 50×50 μm) to avoid stitching error caused by moving the stage in EBL. The placement and separation of contact leads can also allow relaxed alignment tolerance ($\sim$ a few hundred nm) for EBL. Both layouts share the same four alignment marks for subsequent e-beam writing.

A key in successful EBL is the choice of proper resist. It is remarkable that even today much work continues to be done with PMMA resist on converted SEMs. 950k PMMA 4% diluted in chlorobenzene is the standard resist. In this work we also used an alternative resist of ZEP-520, which has better dry etching resistance compared to conventional PMMA. The ZEP-520 was coated to the sample by 40-sec spin-on at 4000 rpm. The sample is then post-baked at 180 °C for 10 minutes. For the e-beam writing in Raith, a typical area dose of 35 μC/cm^2 is used. After the e-beam exposure and development of the nanopatterns using developer ZED-N50, the ZEP-520 resist is hard baked at 130 °C for 3 minutes on a hot plate. Then the patterns are etched in the substrate by either wet-chemical etching or RIE. After etching the resist is removed



(a)



(b)

Figure 5.2: Design view of optical photolithography masks with alignment marks for (a) a Hall bar geometry for e-beam patterning of multiple quantum point contacts or gaps for leakage tests; (b) a symmetric square island geometry for complex quantum dot structures. The mask is designed in L-Edit, Tanner EDA.

by ZDMAC remover, and a solvent clean (acetone/isopropyl alcohol). Finally an optional UV/ozone clean in a UVOCS cleaner can be used to remove residual e-beam resist [86].

The feature size and surface cleanliness of the final nanopatterns will depend on the choice of etching process after the resist development, and will be discussed in the next Section 5.3.

5.2.2 PFOTS-aided AFM Lithography

The scanning probe microscopy (SPM) field began with the invention of the scanning tunneling microscope (STM) [87, 88] in 1981. It has enabled the researchers to image the world at the atomic scale. Among the many established types of SPM, atomic force microscopy (AFM) [89] is one of the foremost methods for imaging, measuring and manipulating matter at the nanoscale. With the discovery of AFM anodic oxidation, AFM lithography demonstrated a powerful tool to pattern a H-passivated Si (100) surface down to 10 - 30 nm size [90].

At Princeton we developed AFM lithography based on a Digital Instruments (DI) Dimension 3100 AFM. Three functionalities are added to the microscope to enable lithography, as shown in Fig.5.3:

1. The "nanoman" software package from DI which provides the flexible, yet accurate control of the in-plane position and movement of the AFM tips.

2. The Signal Access Modules (SAM) in-line hardware accessories that can apply a DC-voltage to the AFM tip during the local anodic oxidation.

3. A home-made humidity-controlled chamber environment which supplies water-vapor as the electrolyte for anodic oxidation.

AFM lithography can be used to pattern Si (or SiGe) by anodic oxidation of silicon under the tip with applied negative voltage. Because the oxide thickness is limited to ~ 4 nm, only about 2-nm silicon can be oxidized [92]. To pattern thicker SiGe layers, a two-step wet etching can be used as shown in Fig. 5.4. A thin silicon cap on top of the SiGe is first oxidized by AFM, then with a dilute HF dip to remove the oxide, followed by a selective wet etching (CH_3COOH:H_2O_2:HF = 1:2:3) [93] to transfer the pattern into underlying SiGe. This is difficult to control in practice since the thin silicon is not a perfect barrier for the selective etching. This limitation is overcome by

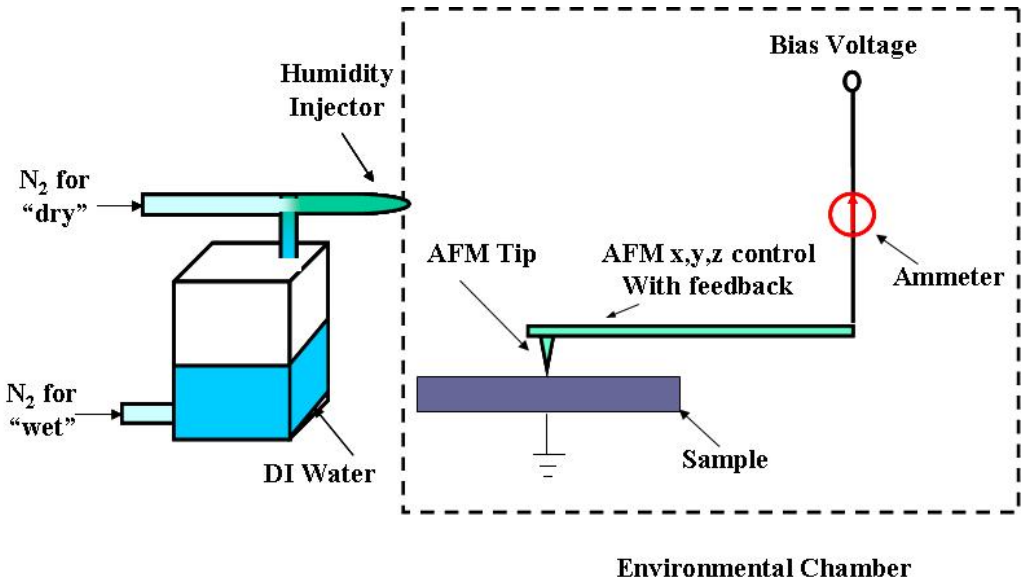


Figure 5.3: The instrument setup for AFM lithography [91].

adding a self-assembled monolayer perfluorooctyl trichlorosilane (PFOTS) [94] before AFM oxidation as an etch resist to improve the uniformity and repeatability.

Since only a 2-nm silicon surface layer will be oxidized by AFM oxidation, ultra-smooth PFOTS monolayers need to be obtained before the AFM lithography. We first removed native oxide on silicon substrates by an HF dip. Then the silicon substrates were heated in a 1:3 solution of H_2O_2 and H_2SO_4 at 80 °C for 30 minutes, to provide a smooth oxide surface for the PFOTS film growth. This acid treatment was followed by an extensive DI water rinse and nitrogen blow dry. For growth, the substrates were immersed at room temperature in a 1 mM solution of PFOTS in dodecane for 3 hours in a nitrogen glove box environment with minimal exposure to the ambient. The long immersion time can ensure a complete monolayer formation [94]. After growth of the self-assembled monolayers, the surface roughness was measured by AFM to be 1.8 Å. The monolayer thickness is estimated to be $\sim$ 2.6 nm.

AFM lithography was then performed on PFOTS-coated substrates at room temperature in tapping mode. The relative humidity was kept at $\sim$ 40% by bubbling nitrogen through water into an environmental chamber surrounding the scanning tip.

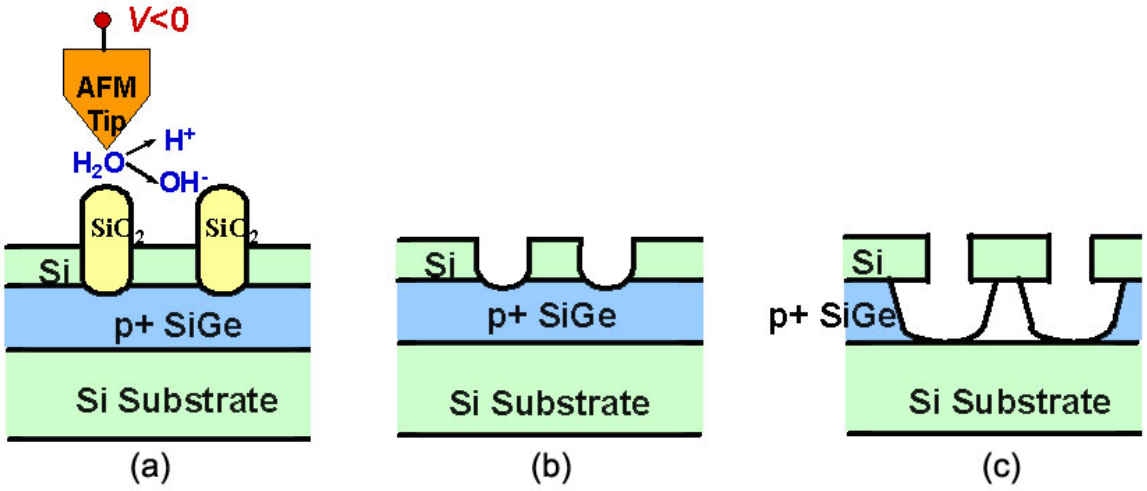


Figure 5.4: Process of nanopatterning Si/SiGe layers with AFM lithography and two-step wet etching: (a) AFM local oxidation, (b) Remove oxide by HF, (c) SiGe selective wet etching.

By applying a negative bias ($\sim$ –20 V) to the tip at a scanning speed of 0.4 μm/s, a 2-nm silicon surface layer underlying the PFOTS is locally oxidized. Oxide linewidths well under 100 nm can be achieved. By a dilute HF dip and a selective SiGe wet etching ($HF:H_2O_2:CH_3COOH$ = 1:2:3), the pattern is transferred to the underlying SiGe layer and stops at the silicon layer. Fig. 5.5 shows the complete process. The FWHM of the SiGe linewidth is on the order of 100 nm, which is comparable to the resolution of AFM lithography without PFOTS. High-resolution can be achieved by optimizing the bias voltage and writing speed [95].

Compared with the previous direct AFM lithography of Si/SiGe layers, the use of PFOTS monolayers as an etch resist greatly improved the pattern transfer uniformity and repeatability. When only the thin silicon cap layer itself was used as the selective etch barrier, the pattern transfer from AFM oxidation by wet etching were very non-reproducible, and the etch was limited to a short time ($\sim$ 20 seconds). An increased surface roughness after the wet etch was also observed. With this additional PFOTS film as a resist, now the selective etch can be several minutes long, so now thicker SiGe layers with lower Ge content can be patterned with far improved uniformity

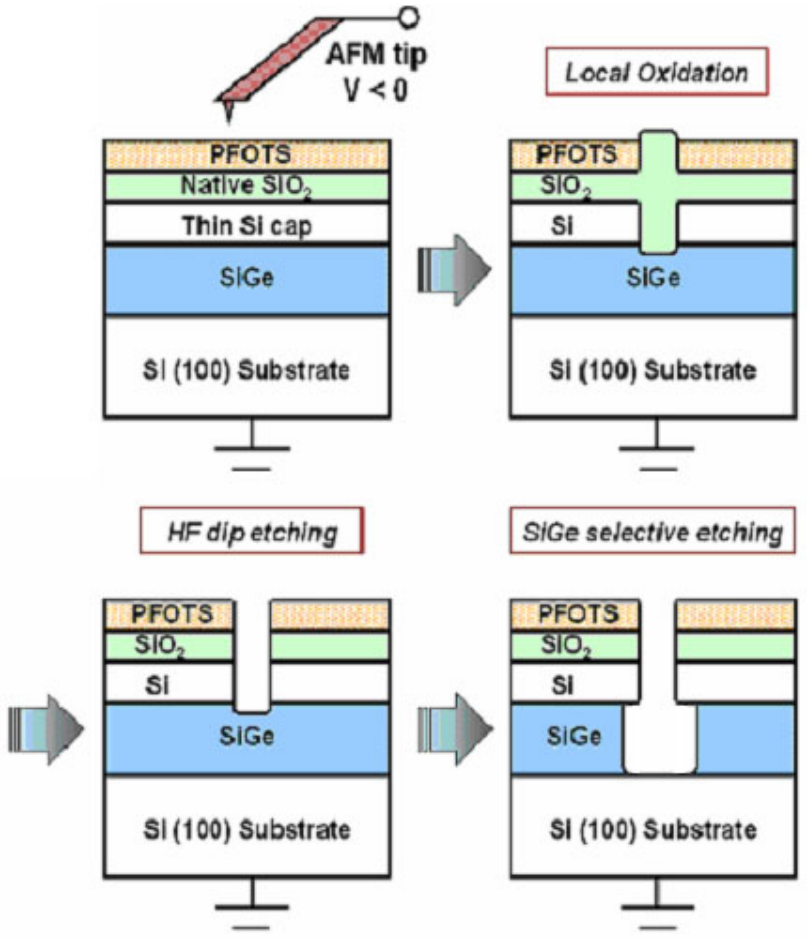


Figure 5.5: Process of PFOTS-aided AFM lithography. PFOTS is deposited on native oxide (for bonding) to prevent etching through 2-nm silicon surface layer during SiGe patterning for improved uniformity. The two-step etching process is used to pattern SiGe thicker than $\sim$ 2 nm.

than without PFOTS. Fig. 5.6 shows a comparison of the etching profile without and with the additional PFOTS. When etching time is 40 seconds or longer, undesirable pinholes were found on the silicon surface without PFOTS.

As a demonstration of AFM lithography with PFOTS of Si/SiGe nanostructures for quantum device application, we first grew a 2-D hole gas in compressively strained $Si_{0.7}Ge_{0.3}$ channel with a $Si_{0.9}Ge_{0.1}$ supply layer in sample #3716. The mobility and hole density are 1300 cm^2/Vs and 6×10^{11} cm^{-2} at T = 4.2 K. A Hall bar mesa was fabricated on the 2DHG. Then we cut a line through the Hall bar as shown in Fig. 5.7. Ohmic contacts are made to the 2DHG by lift-off of aluminum and subsequent

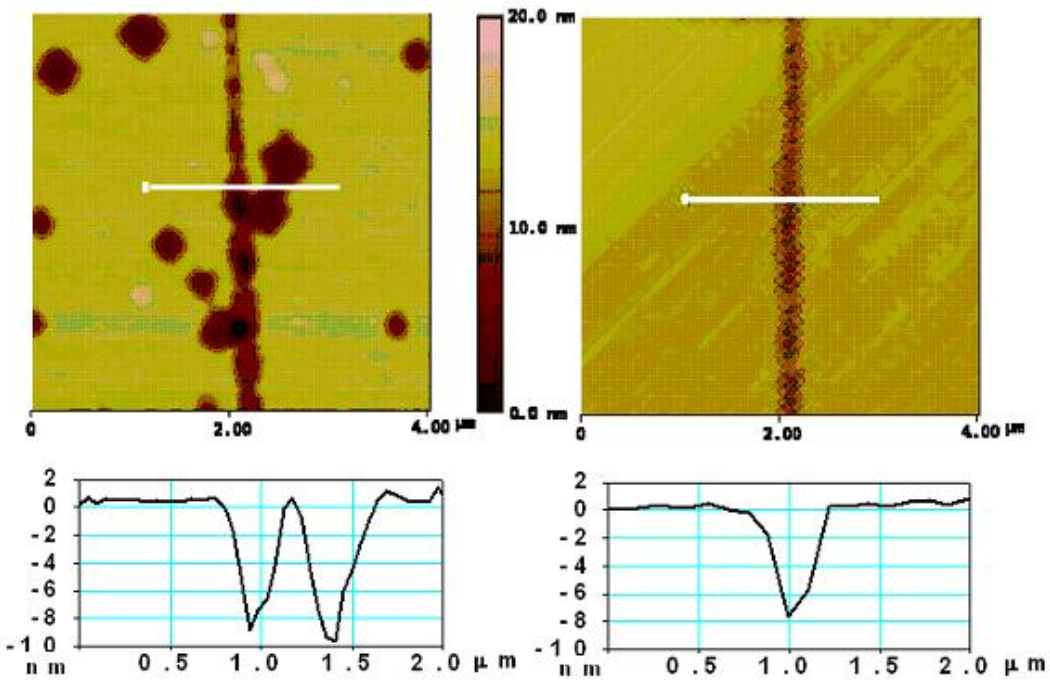
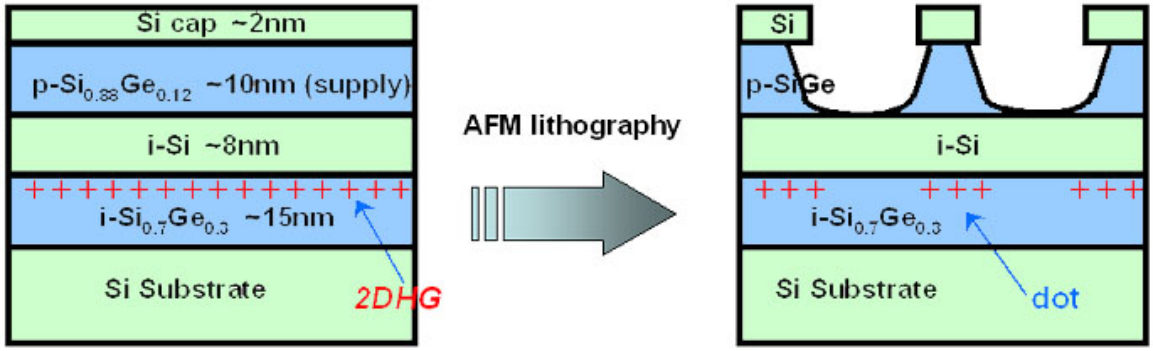


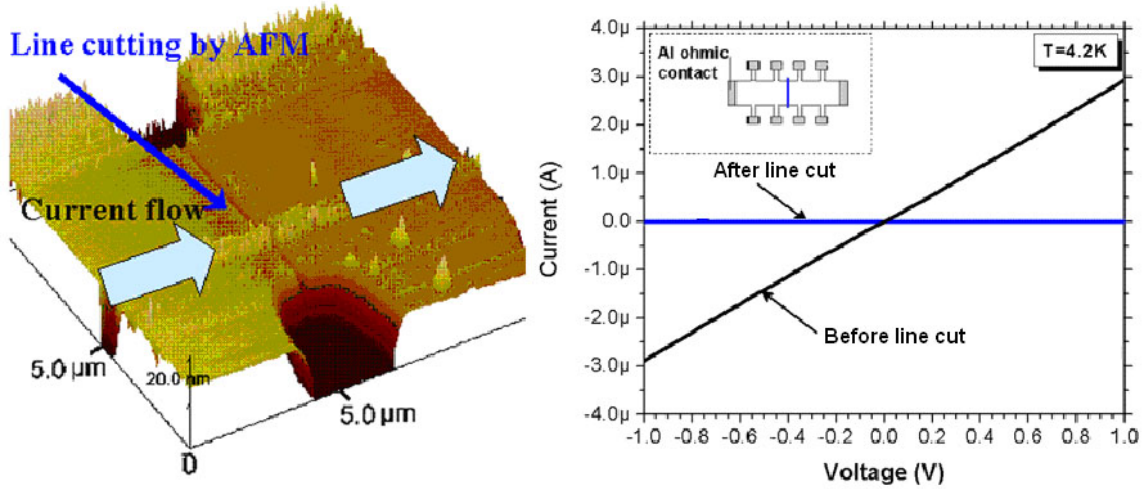
Figure 5.6: Surface image and profile along the labeled white line for a Si/SiGe pattern with (right) and without (left) PFOTS as a resist, the HF dip to remove silicon oxide and the SiGe selective wet etch for $\sim$ 40 sec.

annealing at 450 °C for 10 minutes. The two-terminal resistance after the line cutting was raised from 300 kΩ without cutting to larger than 10 GΩ. This shows the 2-D carriers are localized by nano-patterning of the 2DHG.

As one final comment on the PFOTS-aided AFM lithography, the use of PFOTS or other organic polymers as resist can also enable a much wider range of wet etching chemical selections. For example, PFOTS is an excellent mask against the HF/HNO_3/dilute system, the most popular etchant for isotropic silicon wet etching, which would be otherwise incompatible with the direct AFM lithography that uses either a thin Si-cap or SiO_2 as an etch mask. It makes AFM lithography a more convenient and versatile technique that can pattern complex Si/SiGe structures with a surface that can be locally oxidized by AFM.



(a)



(b)

Figure 5.7: (a) Schematic structures of the 2-D hole gas structure with $Si_{0.9}Ge_{0.1}$ supply layer for patterning by AFM lithography; (b) AFM image and I-V curve of Hall showing conducting path cut by PFOTS-aided AFM lithography of supply layer and increased resistance at 4.2 K after the cut.

5.2.3 Comparison of Nanolithography Methods

As a comparison of e-beam lithography and AFM lithography, we list both methods' advantages and drawbacks.

E-beam lithography is the most mature technique. It offers the highest throughput and fastest writing speed. Both lithography hardware packages and simulation/design softwares are commercially available and meet the industry standards. The main drawback for quantum dot applications is the lack of convenience due to the complexity of the system. The irradiation from the higher-energy electron beams may

also cause an undesirable charging effects [96]. Proximity effects due to electron scattering is also well known to limit the ultimate feature resolution [97]. However, at present most quantum dot applications do not require lines and spaces below 20 nm.

In comparison, AFM is a much more convenient tool than SEM as it can operate perfectly in ambient and does not require high voltage. It can completely avoid radiation and charging effects. In addition, AFM as an imaging tool can produce a true 3-D surface profile with higher resolution, while it is difficult to obtain height information of the surface topology with SEM.

One disadvantage of AFM lithography is the low throughput. There are several reasons for this in practice. First the technique is very surface-sensitive and the reproducibility is poor especially for more complex patterns. Second, there has been plenty of work showing 0-D dots and 1-D lines at nanoscale but few for larger features, for example, a 2-D square box consisting of many AFM scan lines can be very slow and requires a lot of calibration efforts. Third, the conventional AFM tips suffer from rapid wear which degrades the quality of the AFM local anodic oxidation. Another inconvenience of AFM lithography is that only wet etching can be used for pattern transfer because the SiO_2 and PFOTS are too thin to serve as a dry etch mask. The reliance on wet etching not only increases the minimum feature size due to undercut from isotropic etching, it also limits the materials and layer structures that can be etched.

Both e-beam lithography and AFM lithography can produce nanopatterns with about 50 nm minimum linewidth for our modulation-doped Si/SiGe heterostrutures. Because of difficulty with reproducibility and linewidth control with our early work in AFM lithography, even with PFOTS, the installation of the Raith e_Line system at Princeton, and the ability to use anisotropic RIE, the quantum dot devices discussed in this thesis will be mostly based upon e-beam lithography.

5.3 Etching Methods

5.3.1 Wet Etching of Si and SiGe

Wet etching is an etching method where the material is dissolved in a wet chemical solution. It is the simplest etching technology. In particular for Si, three types of wet chemicals are commonly used: HF/HNO_3 solution, potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) solution, and $HF/H_2O_2/CH_3COOH$ mixtures for etching SiGe.

HF/HNO_3 diluted in H_2O or CH_3COOH is the most popular isotropic wet etch of silicon. Various compositions give different etch rates, since the activation energy of the etching process is different in the different composition regions [98]. Composition in the high-HNO_3 region is generally preferred due to lab safety concerns. The typical etch rate of Si is very fast, about 100 nm/min for a composition such as $HF:HNO_3:H_2O$ = 1:5:10. The solution etches SiGe much faster than Si, making it very hard to control the etch thickness in Si/SiGe multi-layer structures. The HF/HNO_3 solution is well suited for making big mesas where precise control of the etch stop is not required, for example, a Hall bar mesa defined by optical lithography for Hall measurement. It is also applied in the semiconductor industry for the removal of contamination and lattice defects generated by the lapping of Si wafers.

The other group of commonly-used silicon etchants is alkali metal hydroxides or quaternary ammonium hydroxides based, such as KOH and TMAH solutions. Both solutions are non-flammable, and TMAH is gaining more popularity because it contains no alkali metal ions and hence is CMOS compatible. The etching characteristics are very different from the HF/HNO_3 wet etching. First, KOH and TMAH etch Si anisotropically, meaning that the etch rate is dependent on the crystallographic directions. The most slowly etched planes are the {111} planes. The {100}, {110}, and all other high-index planes are etched much faster. For this reason, the etched cavities

are bounded between {111} planes, resulting in the shape of V-grooves, truncated or full pyramids on regular (100) wafers. Second, unlike the acid-based solutions or KOH, TMAH does not not attack SiO_2 and therefore offers more selectivity. Moreover, recent studies showed that TMAH etching is also selective with respect to SiGe, which can be very useful for nanopatterning Si/SiGe by all selective wet-chemical etching [99]. The reported TMAH etch rates correspond to selectivities of 20:1 for $Si_{0.76}Ge_{0.24}$ and better than 4200:1 for SiO_2.

In our set-up, the anisotropic Si wet etching was performed in an aqueous solution of TMAH (25 weight %) at 120 °C. The etch rate on Si (100) substrate is extremely fast (on the order of μm/min). For SiGe with 30% Ge content, the etch rate is found to be less than a few nm/min.

Much work exists on wet etching of pure Si. With the rapidly growing field of SiGe technology, the properties of wet-chemical etchants targeting SiGe were also investigated. Selective SiGe etching with respect to Si has been done by acidic solutions such as $HF/H_2O_2/CH_3COOH$ [93]. The etch rate has been found to depend strongly on Ge content. For $Si_{0.7}Ge_{0.3}$ etched in $HF:H_2O_2:CH_3COOH$ = 1:2:3 solution, the etch rate is about 40 nm/min at room temperature and corresponds to a selectivity of 400 over Si. Fig. 5.8 shows the etch selectivity as a function of Ge content. Reasonable selectivity can be achieved for SiGe vs. Si with more than 20% Ge.

To compare all the above wet etching methods for Si/SiGe heterostructures, Table 5.1 shows their properties with regard to the isotropy and selectivity on different materials.

Table 5.1: Common properties of Si/SiGe wet-chemical etchants on planar substrates.

	Isotropy	Selectivity (target material)		
Solution		Si	SiGe ($\geq$ 20% Ge)	SiO_2
HF/HNO_3	isotropic	yes	yes, much faster	yes
KOH (heated)	anisotropic	yes	no	yes, much slower
TMAH (heated)	anisotropic	yes	no	no
$HF/H_2O_2/CH_3COOH$	isotropic	no	yes	yes

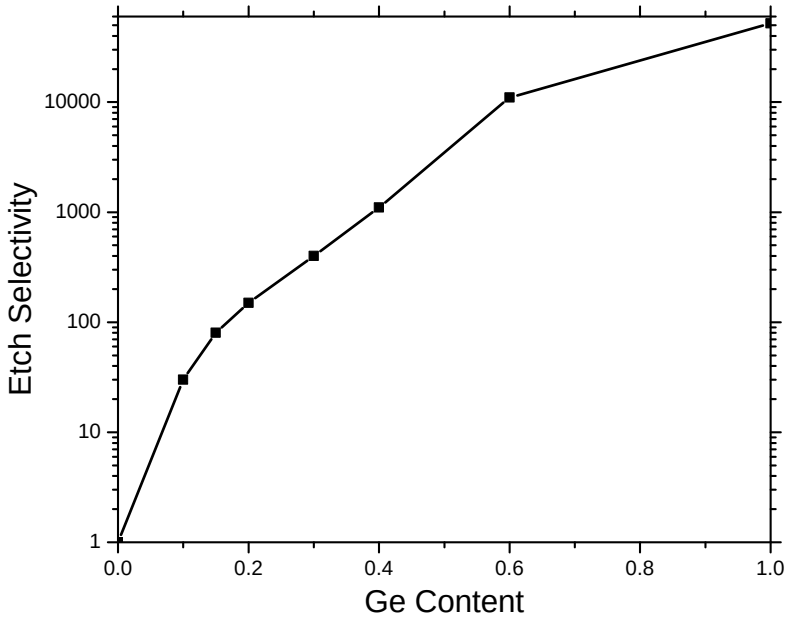


Figure 5.8: Etch selectivity vs. Ge content with respect to Si for p-type SiGe etched in HF:H_2O_2:CH_3COOH = 1:2:3. The etch rate data are obtained from [93].

The two-step wet etching process (SiO_2 etch and SiGe etch) can be combined and used as a low-damage fabrication technique for lateral nanopatterning of Si/SiGe heterostrutures. In fact, our first quantum point contact (QPC) type of nanodevice in $Si/Si_{0.7}Ge_{0.3}$ 2DEG was made by e-beam lithography and selective wet etch (see Chapter 7 for more details).

Fig. 5.9 shows the process and cross-sectional view of device fabrication after etch lithographic and etching steps. The 2DEG surface was first treated in H_2O_2/H_2SO_4 acid to form native oxide as an extra TMAH-resistant mask for better selectivity. High resolution QPC lithography was achieved by using a thin layer of 950K PMMA and e-beam exposure. Then both the thin oxide and Si cap in open paths were etched by a brief RIE. Wet etch could also be used here, for example, HF and TMAH dips. But RIE is the preferred method as it can also provide descumming of the positive PMMA resist in the exposed regions. The lithographically defined patterns

were first transferred into the SiGe supply and spacer layers by $HF/H_2O_2/CH_3COOH$ wet etching for about 20 seconds. The isotropic etch will result in an undercut of about 70% of the etch depth, and will stop at top of the Si channel. Finally the Si channel is also selectively removed by TMAH wet etching for about 10 seconds. Both SiO_2 and/or SiGe are excellent masks for TMAH etching even if the thin PMMA was stripped in previous etching steps.

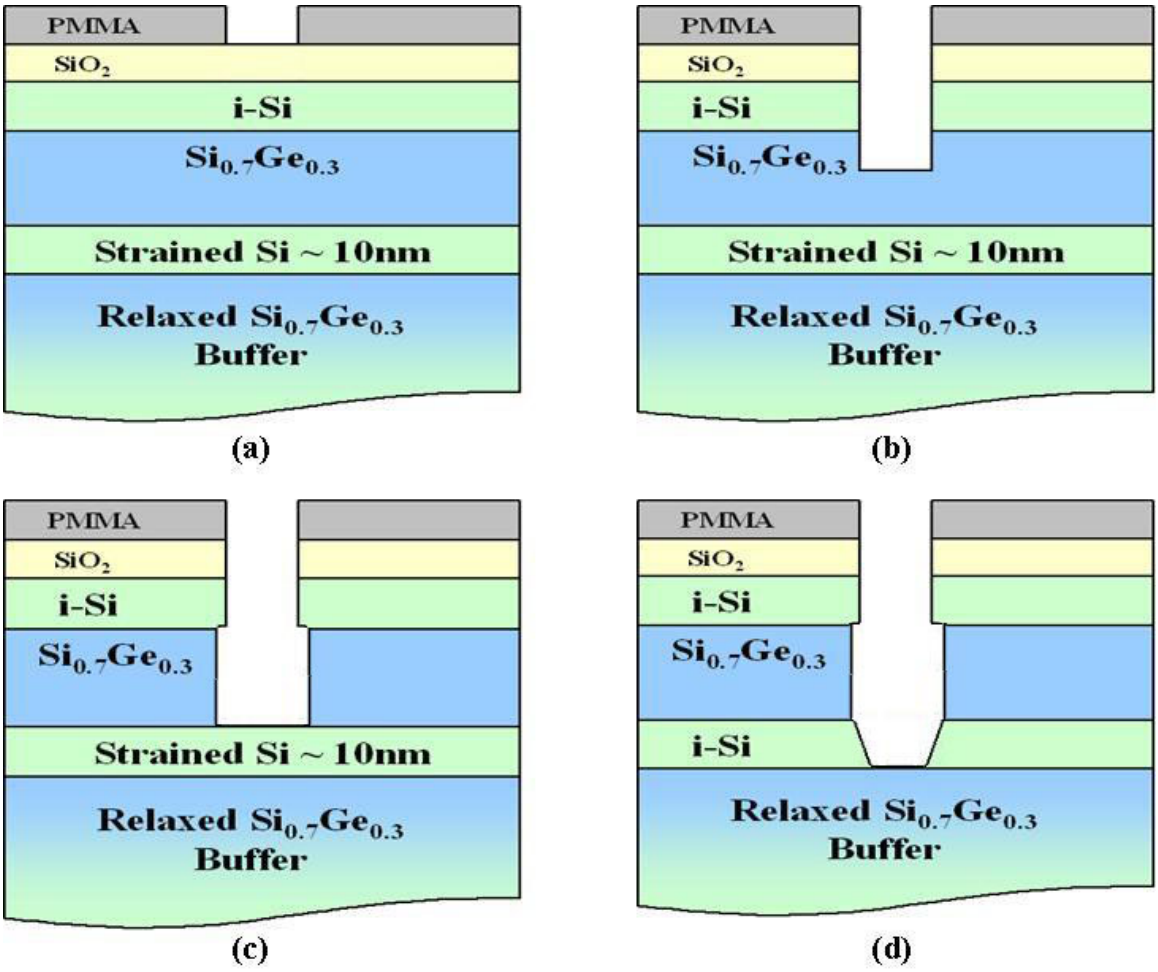


Figure 5.9: Process of QPC in Si/SiGe heterostructure 2DEG fabricated by e-beam lithography and selective wet-etching. (a) E-beam lithography and development of PMMA; (b) a shallow RIE to remove SiO_2 and Si; (c) SiGe wet etch; (d) Si wet etch.

Fig. 5.10 shows the SEM image of Si/SiGe QPC after all etching steps and the removal of PMMA resist. The micrograph was taken by the same SEM in the Raith e_Line system that is used for e-beam lithography. The narrowest gap between the

lateral gate and the central electron channel is about 200 nm wide. No significant undercut was observed in the active QPC region defined by e-beam lithography. The surface of area which was only etched by wet chemicals appears to be smoother than the surface surrounding the Hall bar mesa which was fabricated by optical lithography and RIE.

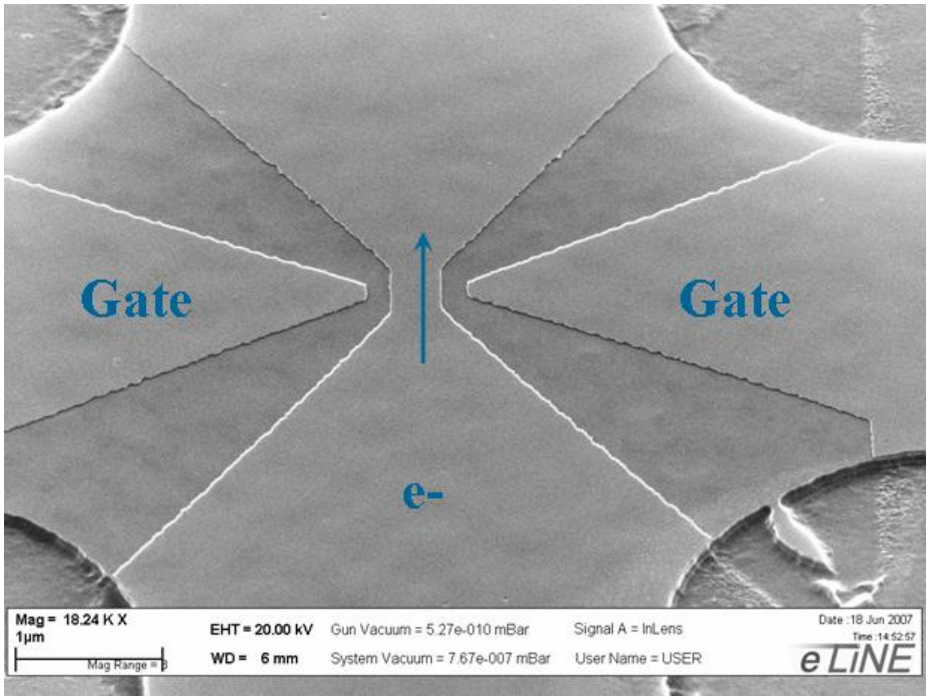


Figure 5.10: A SEM image of Si/SiGe QPC after all etching steps and the removal of PMMA resist.

After the QPC nanopatterns were created by e-beam lithography and selective wet etching, the whole sample surface was then passivated by Si/SiGe epitaxial regrowth for better surface/interface control, which will be the main topic in the next chapter. The final QPC device characteristics will be discussed in detail as part of Chapter 7 of this thesis.

5.3.2 Dry Etching of Si and SiGe

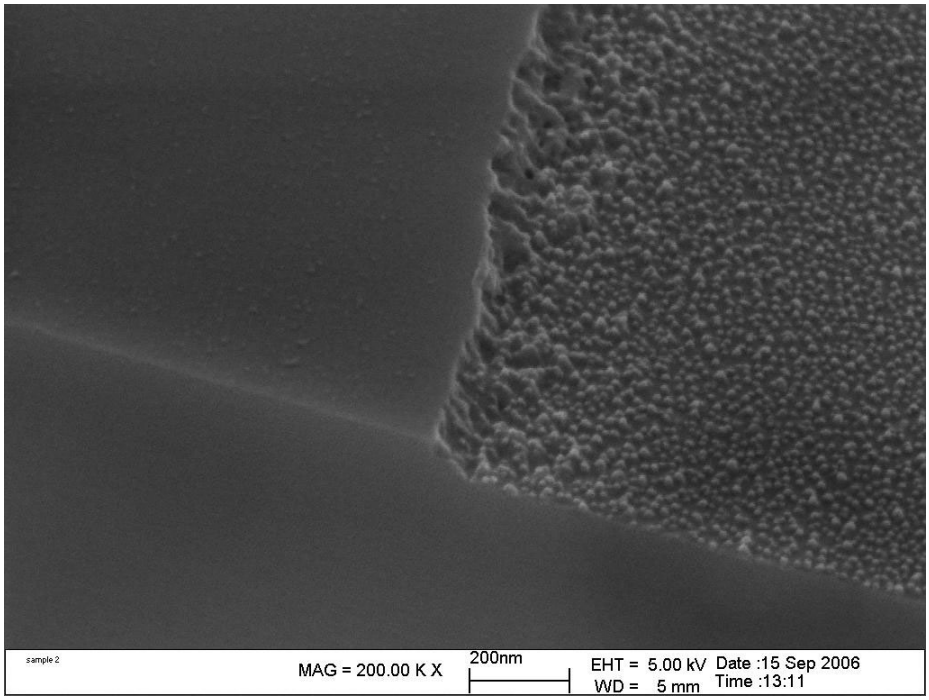
Dry etching is the second class of semiconductor etching methods. Reactive ion etching (RIE) is a form of dry etching that involves a plasma of reactive gases as

the etchant. High-energy ions from the plasma reach the substrate and physically or chemically react with it, which can lead to a product that is volatile. Unlike many of the wet etching methods, the fundamental dry etching process is anisotropic, or directional. There are several mechanisms which can lead to anisotropy. The first is the formation of thin polymer coating on the sample's surface, which can be from the fluorocarbon etch gases themselves and/or the erosion of the photoresist in the plasma. In flat areas this is physically removed by the bombardment of positive ions from the plasma in the vertical direction. The coating is not removed on the sidewalls of etched feature as they are not bombarded. The etching process from the neutral radicals is masked by the polymer and thus only occurs on horizontal surfaces, not vertical ones. This leads to preferential etching in the vertical direction. In other words, the etch is anisotropic. The modern CMOS industry has long since adopted dry etching to achieve small features and vertical sidewalls with high precision.

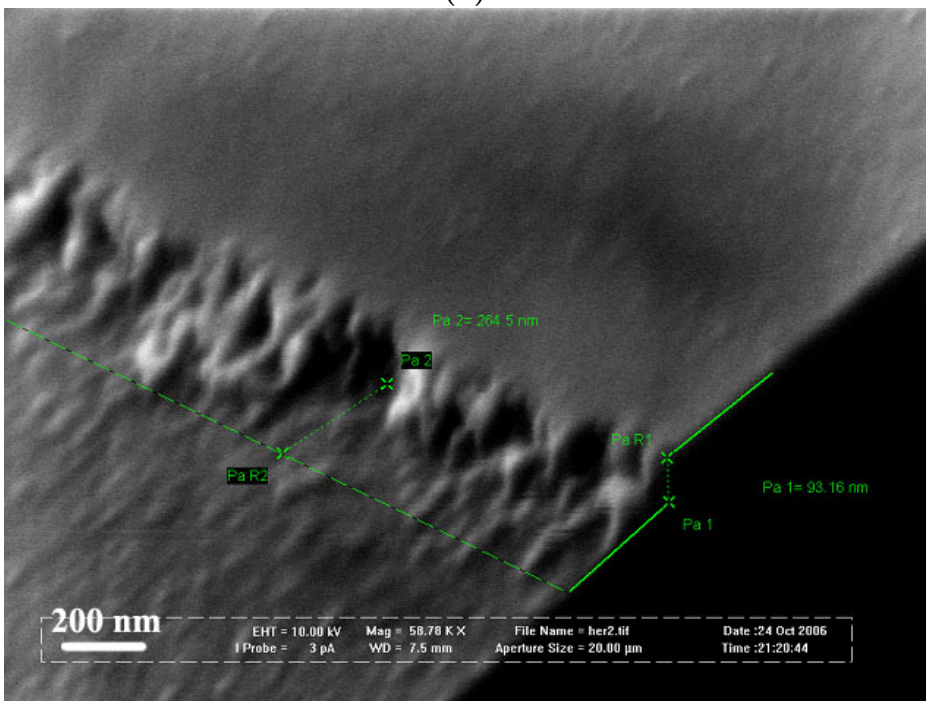
An ideal RIE recipe for quantum dot applications is sought to have the following properties: highly anisotropic for vertical sidewalls, steady and slow etch rate for precise control of the etched depth, and low Si/SiGe etch selectivity to avoid the need for multiple etches. Since anisotropic dry etching of Si-based materials is usually carried out with either chlorinated or fluorinated gases, we characterized common Cl or F-based gases by performing a shallow etch on planar Si substrates and subsequent SEM imaging.

All RIE were performed in a PlasmaTherm 720 SLR Series RIE system. It is a single-chamber system with a load lock and a turbo pump. For highly anisotropic etch we chose very low system pressures (< 10 mTorr) for low ion collisions and high ion energies. For most gas mixtures that we tried, SEM images revealed some excess polymer buildup on either planar surfaces or vertical sidewalls. Fig. 5.11 shows two examples of formations of such polymer products.

Pure chlorine-based chemistry is not well suited for our purpose as the Cl contam-



(a)



(b)

Figure 5.11: SEM images of Si/SiGe structures etched by RIE using: (a) Cl_2/Argon gas mixtures; (b) SF_2/CCl_2F_2 gas mixtures.

inant increases the roughness of bottom surfaces, as shown in Fig. 5.11 (a). It is also hazardous and corrosive and thus require special safety-related processing equipment. Next, we investigated the mix of chlorine and other fluorinated gases and its effect on polymerization. In general, polymer residuals are composed of carbon-fluorine polymers, and a low fluorine/carbon ratio should lead to increased polymerization. Among all the difference gas combinations that we tried, the chlorine in any of the etch gases (as Cl_2 or CCl_2F_2) did not reduce the excess polymerization on the sidewalls. Therefore, our only choices seem to be the pure F-containing etchants, such as SF_6 or CF_4. Fluorocarbon gases have often been used to produce deposition inhibiting lateral etching, resulting in anisotropy [100, 101, 102]. Indeed our best etching result was obtained in CF_4/O_2 gas mixture. Fig. 5.12 shows a SEM image of an etched Si/SiGe quantum dot structure. Compared to previous etched structures, both a straight sidewall profile and a clean bottom surface were achieved. It also shows an undercut of SiGe below Si layer in the heterostructure, which is due to faster plasma etching of SiGe than that of Si. Fluorocarbon gases with lower fluorine/carbon ratio such as C_4F_8 can produce more sidewall protection compared to CF_4 hence lead to a more straight sidewall profile through the different Si/SiGe layers [103].

Table 5.2 summarizes the dry etching characteristics of Si/SiGe heterostructures using different etch gases. The fluorocarbon plasma etching is clearly the most promising choice despite its preferential etching of SiGe. However, one inconvenience of the CF_4/O_2 gas chemistry is that it noticeably attacks PMMA or other polymer resist due to the presence of O_2 plasma, at an etch rate about the same as that of Si. Using pure CF_4 or CF_4/H_2 mixture does not improve the selectivity, since the etch rates of Si and SiGe also decrease proportionally. Therefore, for nanopatterning Si/SiGe heterostructures with CF_4-based gases, it is important that the patterned resist mask is at least as thick as the etch depth. The use of resists more resistant to dry etching, such as ZEP-520, is desirable for future work.

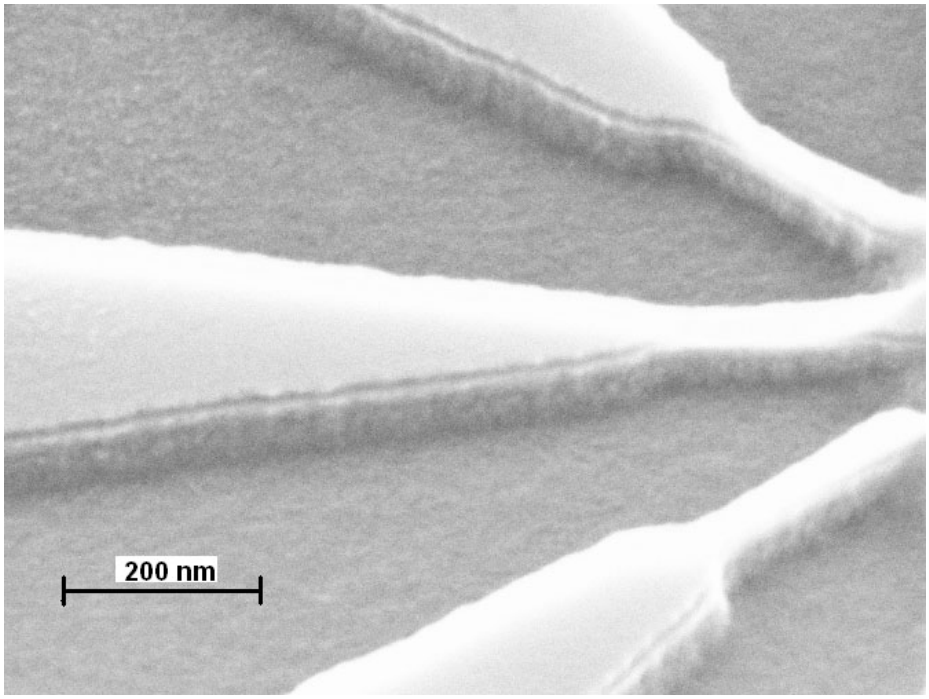


Figure 5.12: A SEM image of Si/SiGe quantum dot structure etched by RIE using CF_4/O_2 gas mixture showing a straight sidewall profile and a clean bottom surface.

Table 5.2: Properties of Si/SiGe RIE using different etch gases on planar substrates.

Gas flow rate (sccm)	RF Power (W)	Etch rate ratio ($Si_{0.7}Ge_{0.3}$/Si)	Sidewall	Bottom surface
SF_6/CCl_2F_2=20/2	50	1.07	very rough	rough
SF_6/Cl_2=10/10	50		rough	rough
CCl_2F_2/O_2=50/5	100	1.09	rough	rough
Cl_2/Ar=10/20	100	1.47	vertical	very rough
CF_4/O_2=50/5	100	1.6	vertical	smooth

The typical dry etch rate we used for Si/SiGe quantum dot applications is about 50 nm/min, which is about one to two orders magnitude slower than the wet etching. It is easier for fine tuning the dry etch rate by changing plasma source power and gas flow rates. So we chose RIE over wet etching for more complex device features such as multiple quantum point contacts and quantum dots.

5.3.3 Mix of Dry and Wet Etching of Si/SiGe

One potential worry when using dry etching methods is that the crystal surface is bombarded by ions and defects could be generated. This ion-induced damage could result in the deterioration of the device characteristics, especially in the high mobility 2DEG structures [104]. The bombardment damage induced in the material may occur both at top surfaces and at sidewalls. For unmasked top surfaces the mechanism for damage penetration is the accidental channelling of the incoming ion flux creating defects as they dissipate their final energy [105, 106]. For the sidewall case the damage channeling may occur from both ion bombardment and ricochet particles and materials ejected during etching [106, 107]. Penetration depths of over tens of nanometers may occur for some high-energy etch processes. The possible diffusion of defects in following fabrication steps can also modify the final defect distribution.

Much work has been devoted to minimize the dry etch damage, especially in III-V semiconductor systems since they cannot subsequently be anneal-treated. Here we propose a simple method using wet etching to remove potential sidewall defects created during dry etching. The Si/SiGe heterostructures were first etched by RIE to the desired depth, then immersed in HF/HNO_3 or $HF/H_2O_2/CH_3COOH$ for about 5 - 10 seconds to remove a thin sacrificial layer of Si/SiGe on the sidewalls and bottom surfaces of the trenches. This would remove etch-induced defects and shallow damage at these surfaces due to bombardment. The wet etch clean-up step will increase the minimum feature size due to the undercut from isotropic etch, but with only a fraction of the undercut created by a pure wet etching, since the wet etching is intended to remove only a very thin layer.

As one example, Fig. 5.13 shows a SEM image of Si/SiGe heterostructures etched by mix of CF_4/O_2 RIE and $HF/H_2O_2/CH_3COOH$ wet etching. The uneven features on the top surface are PMMA residuals and were later cleaned in 1165 stripper and ozone. Compared to the SEM (Fig. 5.12) obtained after only dry etching, the

undercut feature is $\sim$ 40 nm, about twice as wide as before.

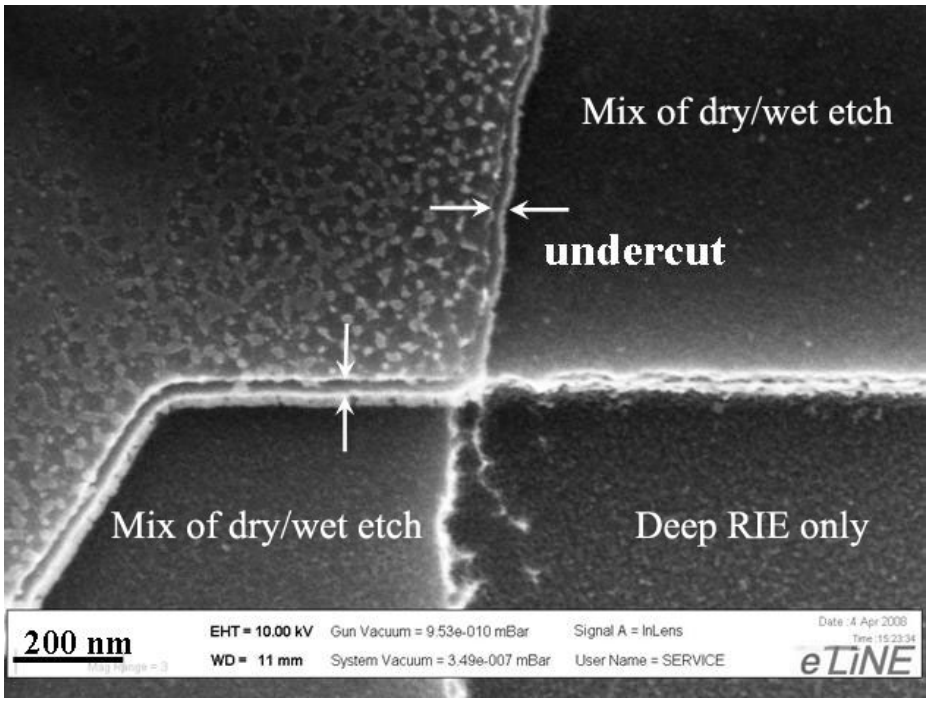


Figure 5.13: A SEM image of Si/SiGe heterostructures etched by RIE using CF_4/O_2 gas mixture and a subsequent 10-sec $HF:H_2O_2:CH_3COOH$ = 1:2:3 wet etching. The finished undercut features are marked by arrows.

5.4 Summary

With the demonstration of successful epitaxial growth of the 2DEG in strained Si and the enhanced electron mobility, realistic device applications will rely on fabrication techniques with a level of control consistent with quantum computing. For quantum dots using a lateral side-gating scheme, nanolithography and etching are the two most critical steps. In this chapter we discussed many options for each of the fabrication step. We focused on the advantages and limitations of each method, and an assessment of the possible role of each method in Si/SiGe heterostructure quantum dot applications is given.

Both e-beam lithography and AFM lithography directly write accurate nanopat-

terns on the substrate. E-beam lithography is commercially available and can provide high throughput with full compatibility with most etching techniques. AFM lithography by local anodic oxidation (LAO) represents a technological advance as a low-energy nanopatterning technique. The use of self-assembled monolayers such as PFOTS as a resist can improve the reproducibility of wet etching. It also extends the versatility of the technique by allowing the use of most of the wet etching methods.

As for the different etching methods for Si/SiGe systems, the main concerns are the minimum feature size and surface defects induced. A combination of successive selective wet etching can achieve precise control of etch stop in complicated multi-layer structures, but the undercut is still on the order of the total etched thickness and can be hard to control. Among the different dry etch plasma chemistries discussed, the fluorocarbon gas mixtures such as CF_4/O_2 yield the straightest sidewalls and clean bottom surfaces. We hypothesize that the use of a short wet etching as the finishing step can reduce dry etch induced surface damage by removing a thin sacrificial layer. The exact lateral undercut size will depend on the Si/SiGe heterostructure and the choice of etching method, and should be considered in nanolithography mask design.

Fig. 5.14 shows all the fabrication possibilities described in this chapter. For Si/SiGe quantum dot applications with feature size no smaller than 50 nm, our overall preference is e-beam nanolithography and the mix of dry and wet etching methods. This route adopts the standard CMOS fabrication technologies that offer high throughput and accurate control of all critical device profile dimensions, and adds a simple step to relieve defects associated with these high-energy processes.

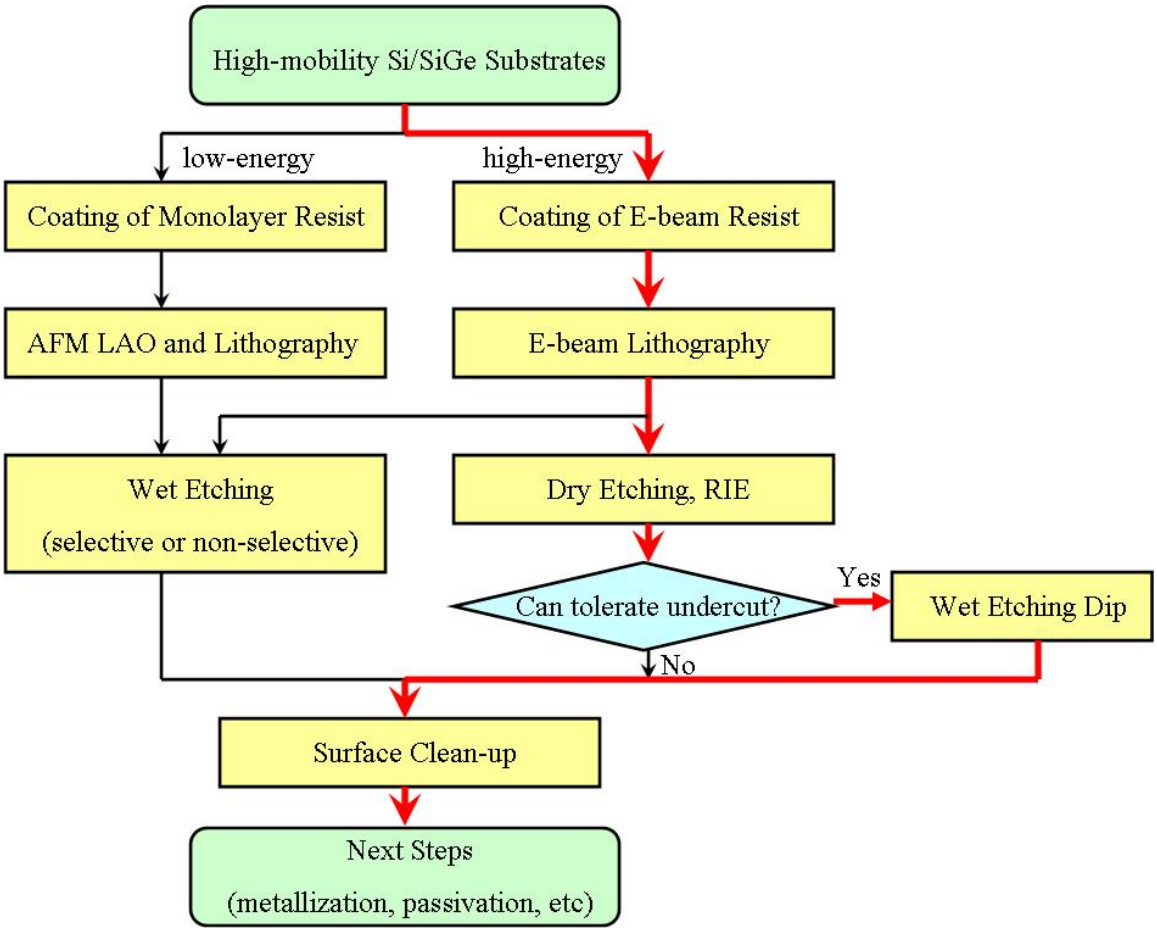


Figure 5.14: Flowchart of the fabrication possibilities for quantum dot applications combining different nanolithography and etching methods. Highlighted (thick red) line gives the overall preference for quantum dot device fabrication described in this thesis.

Chapter 6

Si/SiGe Epitaxial Regrowth

6.1 Introduction

In a quantum dot defined by etching, either by wet-chemical or reactive ion methods, the device surface is often left unpassivated. Single electron effects such as Coulomb blockade can be suppressed by trapping defects related to surface states. Even the best quality thermal SiO_2/Si interface has defect state density around 10^{11} cm^{-2} [108]. Considering the low thermal budget limited by the SiGe layer, the surface of such heterostructures, even with oxide passivation, is very vulnerable. As a result, unpassivated or poorly passivated Si/SiGe quantum devices often exhibit parasitic quantum dot characteristic and hysteresis [109], making it less desirable for the study of quantum computing.

To achieve better surface/interface control, we propose to use Si/SiGe epitaxial regrowth to cover the surface. Fig. 6.1 shows the passivated device structure. Since the overgrown interface is coherent, meaning that the lattice structure is continuous without dislocations or dangling bonds, the interface states due to the dangling surface bonds are therefore expected to be removed by such passivation. For strained Si/SiGe heterostructures on a SiGe relaxed buffer, the regrown layer is lattice-matched SiGe,

which will cause no strain if it has the same Ge content as in the buffer. Therefore, we can overgrow thick epitaxial layers so that surface effects can be minimized. A similar silicon epitaxial regrowth technique was first developed at Princeton and used in SiGe quantum dot single-hole transistor fabrication [110].

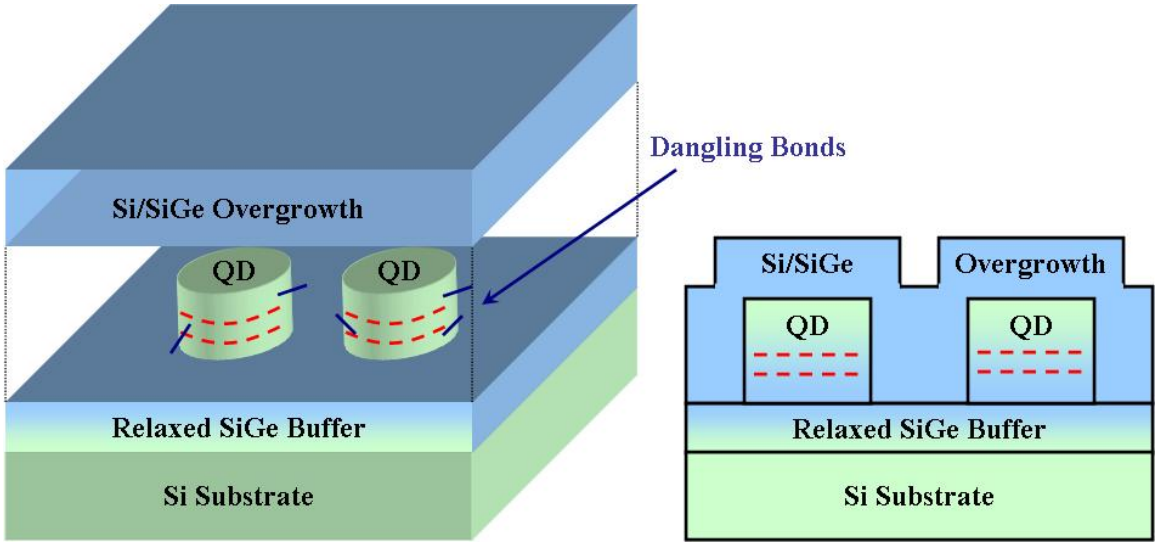


Figure 6.1: Schematic of Si/SiGe quantum dot devices with SiGe epitaxial regrowth. The regrowth ideally creates a coherent interface with no defect states.

The presence of the strained Si layer as well as dopants in the patterned Si/SiGe nano-structure requires a low thermal budget process, a major obstacle that prevents wide use of the epitaxial regrowth. Pre-cleaning processes with low thermal budgets have been studied by many groups [111, 112]. Recently, carbon-free and oxygen-free silicon surface with H_2 baking at 800 °C has been achieved with the Princeton RTCVD system [113]. As a novel alternative, thermal etching of silicon with chlorine is also capable of preparing smooth and contamination-free surface [114]. However, most work to date addresses silicon wafers other than nanopatterned quantum dot surfaces on SiGe relaxed buffers. We will conduct a thorough investigation of these specific issues.

6.2 Cleaning Processes for Si/SiGe Epitaxial Regrowth

6.2.1 Low-temperature Surface Cleaning by H_2 Bake

CVD epitaxial growth processes generally use an *ex situ* wet clean such as an RCA clean. In our system, for both growth and regrowth we use the same wet chemical clean of H_2SO_4/H_2O_2 solution (3:1) at room temperature for 15 minutes followed by a highly diluted HF (1:1000) dip for 2 minutes. In ultrahigh vacuum CVD (UHVCVD), no *in situ* cleaning step at all is required, but often residual carbon and oxygen contamination still are found at the interface [111]. Other conventional CVD methods have relied on high temperature *in situ* cleaning steps such as high pressure H_2 baking at above 1000 °C.

In our Princeton RTCVD system, the standard cleaning recipe is a 1000 - 1100 °C prebake at 250 Torr, with a H_2 flow of 4 slpm. Prebakes at or below 700 °C have not been effective at removing existing surface oxides and carbon, presumably because the temperature is too low for rapid enough desorption. Carroll et. al. [113] examined the pressure dependence of the interface cleaning at 800 °C and demonstrated that hydrogen bakes between 1 and 10 Torr can effectively remove contamination on the Si wafer surface. However, little work has been done to understand cleaning a Si/SiGe structure surface for further SiGe regrowth. For example, Fig. 6.2 shows a SIMS analysis for a regrowth with 800 °C H_2 bake on a modulation-doped Si/SiGe heterostructure. After the growth of the modulation-doped Si/SiGe layers, the wafer was removed from the RTCVD chamber and reloaded after a standard wet clean. The *in situ* clean of the regrowth was done by 2 minutes baking in H_2 at 800 °C. An oxygen peak is still present at the interruption interface between the original silicon cap and the regrown SiGe.

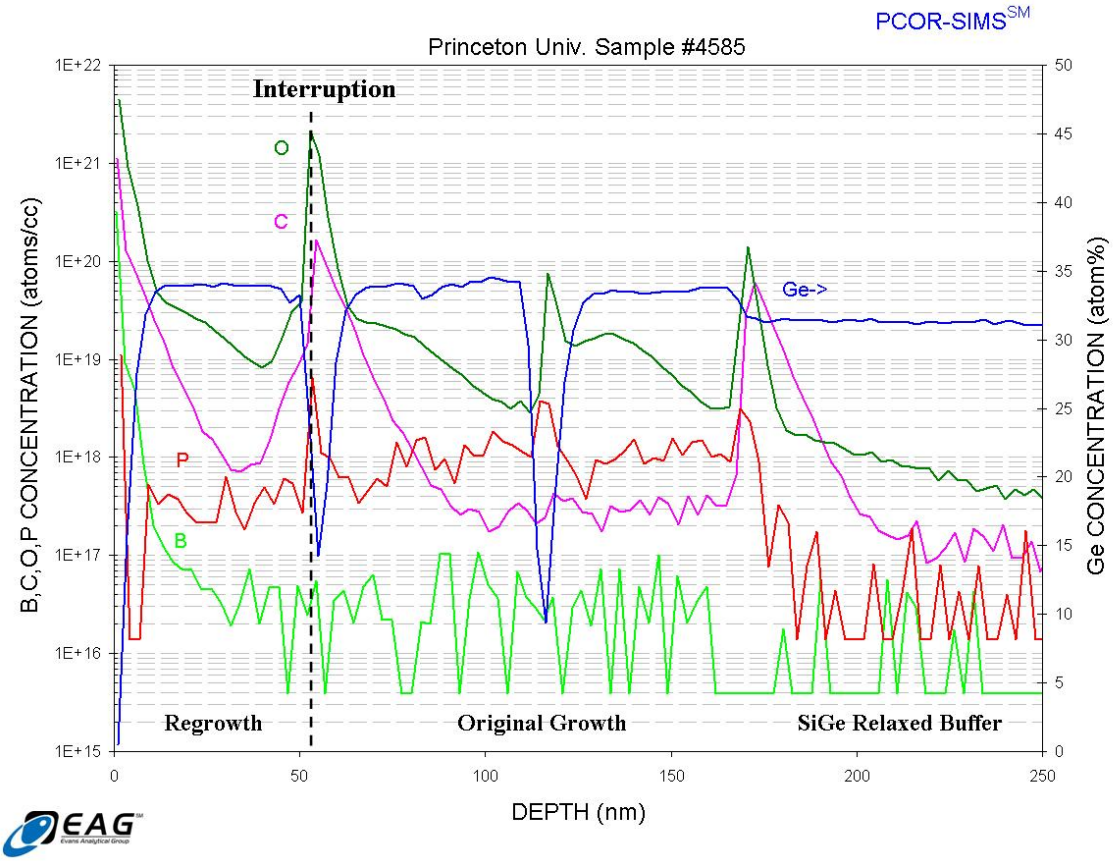


Figure 6.2: SIMS analysis of sample #4585 with epitaxial $Si_{0.7}Ge_{0.3}$ regrowth on a 2DEG in Si/SiGe on $Si_{0.7}Ge_{0.3}$ relaxed buffers. The *in situ* cleaning is a 800 °C 3 slpm H_2 bake at 6 Torr for 4 minutes.

In our modulation-doped Si/SiGe heterostructures, all SiGe layers are relaxed and the total strained Si thickness is well below the (metastable) critical thickness, so thus we could use slightly higher temperature to achieve regrowth of pristine interfaces without worrying about the relaxation of the strained silicon channel. To estimate the effect of phosphorus diffusion, we first note that the silicon intrinsic carrier density around 800 °C is already on the order of 10^{18} cm^{-3}, so we can use the diffusivity under intrinsic inert conditions. Recent measurements of the intrinsic diffusivity of phosphorus in silicon yield the following fit [115]:

$$D_p = 1.71 \times 10^{-3} exp\left(-\frac{2.81\ eV}{kT}\right)\ cm^2/s. \tag{6.1}$$

Unlike the arsenic diffusion in the relaxed SiGe buffers case as we discussed earlier in Chapter 3, the supply and spacer SiGe layers have very few dislocations and the phosphorus diffusion in relaxed SiGe was found to be enhanced by about a factor of three compared to in Si [117, 116]. For example, the reported P diffusivity in $Si_{0.74}Ge_{0.26}$ is about 2.5×10^{15} cm^2/s. Hence the diffusion length for 1 minute of 850 °C bake is $l_p = \sqrt{D_{p(sige)}t} = 3.9$ nm, an acceptable length considering our intrinsic supply layer is usually 10nm or thicker. Higher temperatures would be clearly not feasible.

6.2.2 Chlorine Etching for Low-temperature Surface Cleaning

Recently the use of a thermal step in chlorine as pre-clean before epitaxy has been proposed, as it could lead to a pristine surface (with low interfacial carbon and oxygen concentration) and hence allow a lower temperature prebake. Such *in situ* thermal etching of Si or SiGe with gaseous hydrogen chloride (HCl) or chlorine (Cl_2) removes a thin layer from the surface and substantially reduces reduces surface phosphorus, carbon and oxygen spikes. In a hydrogen ambient the temperature for such chlorine-based etching is still around 800 °C as the etch rate was negligible at lower temperatures.

However, the usefulness of the chlorine etching for regrowth on Si/SiGe nanostructures is severely limited by two factors. First, in practice it is difficult to achieve precise control of the etched surface layer thickness. Typical modulation-doped Si/SiGe heterostructures contains a thin silicon cap. The silicon may act as an etch stop for the SiGe layers, as the etch rate of SiGe in chlorine chemical vapor increases with Ge content and is much faster than that of Si [118]. The exact thickness of such a silicon cap will vary depending on the fabrication process. Second, for the quantum device area that was etched during the fabrication, all strained silicon

were removed and only SiGe was left. The chlorine etching in these area will result in over-etching and increased surface roughness. In fact, we observed very non-uniform epitaxial regrowth with *in situ* chlorine etching - some of the device area without the thin silicon cap was not covered by epitaxial regrowth. Fig. 6.3 shows a cross section TEM image of a gap near an etched Si/SiGe edge #4547. Poor crystalline quality would result from the regrowth on the bottom of trench.

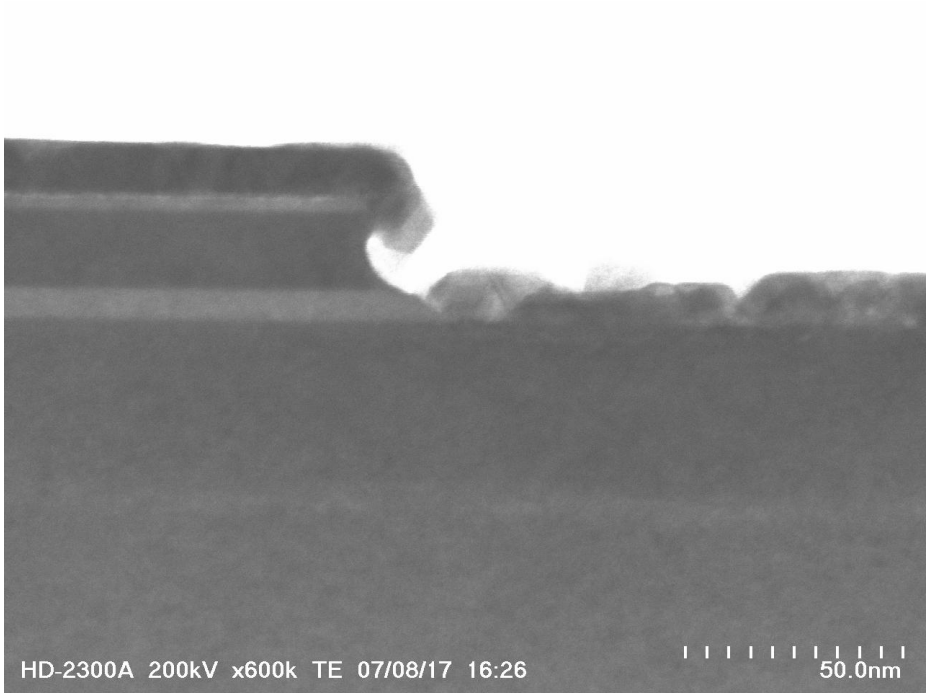


Figure 6.3: A cross section TEM image a narrow gap etched in a 2DEG in Si/SiGe on $Si_{0.7}Ge_{0.3}$ relaxed buffers with Si/SiGe regrowth using chlorine etching as a pre-clean step. The TEM was prepared by Dr. Nan Yao at Princeton and Hitachi laboratory, CA.

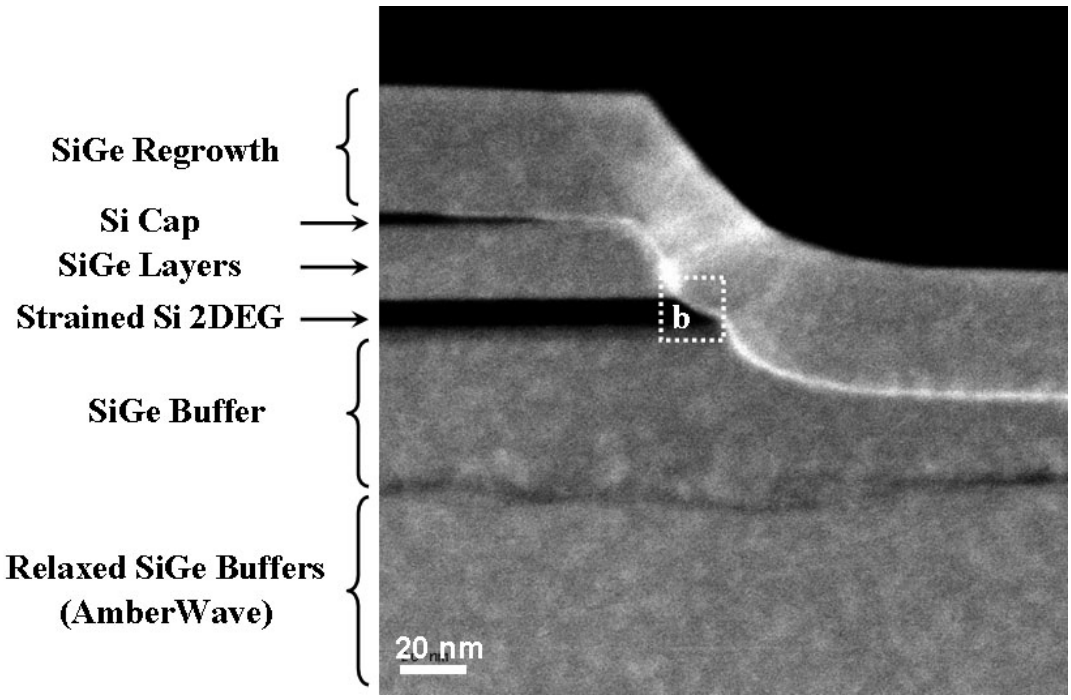
Therefore, the novel technique of etching a thin Si/SiGe layer with chlorine cannot be used prior to epitaxial regrowth on already patterned surfaces. Such etching will cause serious non-uniformity in the regrown layer and should be avoided unless the surface cap layers are very thick ($\sim$ a few tens of nanometers). Therefore this approach was ruled out for our critical device fabrications.

6.2.3 Conformal Epitaxial Regrowth on Sidewalls

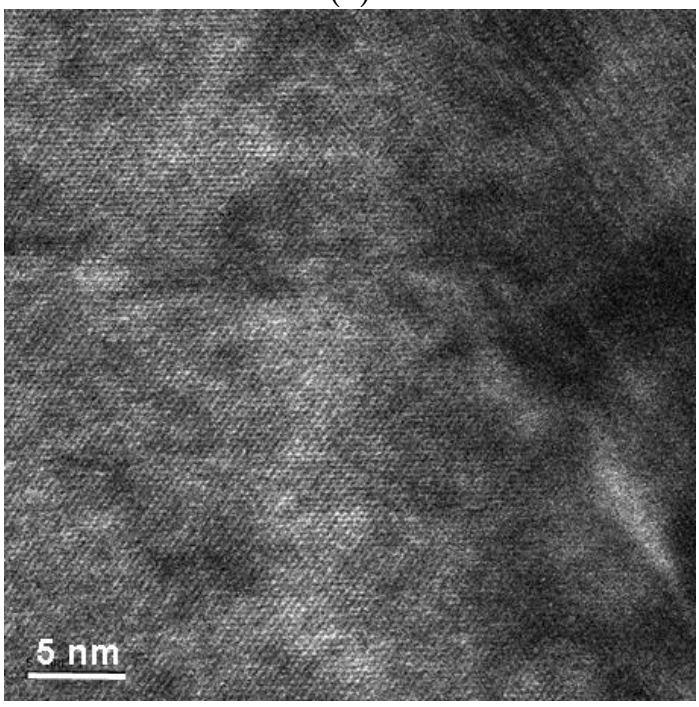
With a better understanding of the surface cleaning issues and the elimination of *in situ* chlorine etching on patterned heterostructure surfaces, we achieved conformal epitaxial regrowth on sidewalls at nano-scale and uniform coverage over the whole wafer. Dr. Nan Yao at the PRISM Imaging and Analysis Center at Princeton University and the Hitachi Labs of California performed high resolution cross section TEM on a patterned Si/SiGe sample with epitaxial regrowth.

The starting sample is a strained Si 2DEG on 30% SiGe buffers. A series of 600-nm-wide, 50-nm-deep lines were defined by E-beam lithography and etched in a CF_4/O_2 gas mixture by RIE. This was followed by epitaxial regrowth of 50 nm thick SiGe capped by a 4-nm Si layer at 625 °C and 700 °C, respectively. The *insitu* pre-clean of the regrowth was done by 5 slpm hydrogen baking at 800 °C for 2 minutes at 6 Torr. Fig. 6.4 shows the cross section TEM image of a narrow gap near an etched Si/SiGe edge #4607 with a zoom-in view of the sidewall. The first noticeable feature is that we clearly achieved crystalline regrowth of SiGe on such a structure. The atomic lattice is continuous at both sides of the interface. 3-D heterojunction confinement surrounding the whole nano-structure was achieved. Fig. 6.4 (a) represents dramatic improvement of the epitaxy uniformity on etched surfaces over the prior poor regrowth. However, the interface is not perfect. Some stacking faults can be observed in the regrown region near the vertical sidewalls. The horizontal interfaces at both the bottom and the top of the trenches appear to be defect-free.

The exact mechanism of defect formation during the regrowth is still unknown. One possibility that we suggest is the strain field induced by the presence of the strained silicon. For the thin tensilely strained silicon, its in-plane silicon lattice matches the SiGe lattice, therefore the regrown SiGe over either strained silicon or relaxed SiGe will bear no strain. On the other hand, when the SiGe regrowth matches



(a)



(b)

Figure 6.4: (a) A cross section TEM image of a narrow gap etched in a 2DEG in Si/SiGe on $Si_{0.7}Ge_{0.3}$ relaxed buffers with conformal epitaxial regrowth on sidewalls. (b) A high resolution TEM image of the sidewall coverage, showing that the regrowth over the sidewall is epitaxial. The TEM was prepared by Dr. Nan Yao at Princeton and Hitachi laboratory, CA.

the perpendicular lattice constant of the strained silicon on the sidewalls, to form a coherent interface the regrown SiGe has to be under compressive strain. Such a strain field effect will only affect the sidewalls.

While the overgrown interface is not perfect, the process shows a route to defect densities which are probably lower than that of the SiO_2/Si interface. Such defect state density is around 10^{10} cm^{-2} for the best quality thermal SiO_2/Si process on perfect (100) surfaces, and it is known to be much higher on other crystalline phases and on SiGe surfaces [119]. We believe that SiGe epitaxial regrowth on etched strained Si quantum dots has the potential to give the best interface control technique and passivation for Si/SiGe quantum dots and related quantum devices.

6.3 Electrical Properties of Si/SiGe Epitaxial Regrowth

6.3.1 The Effect of Si/SiGe Regrowth on 2DEG's

The first critical electrical property of Si/SiGe epitaxial regrowth for quantum dot applications is its effect on the 2DEG quality. As shown in previous calculation, the dopant diffusion during the regrowth is expected to be a few nanometers. The dopant segregation or diffusion towards the 2DEG channel will cause degradation in the electron mobility as well as an increase in the electron density.

We compared electron density and mobility on two sets of 2DEG samples before and after the regrowth. The first set of 2DEG were grown by Princeton RTCVD system with relatively low mobilities. The second set of high quality samples were grown by Dr. Ya-Hong Xie's research group at UCLA in MBE. Both regrowth were done in Princeton RTCVD with low-temperature surface cleaning by 5 slpm H_2 baking at 800 °C for 2 minutes at 6 Torr. Table 6.1 summarizes the results of the two sets of

samples from low-temperature Hall measurement. As a result of the dopant diffusion, the effective spacing between the 2-D electrons and their ionized dopants should be reduced. The electron density increases as more carriers can be transferred to the channel, and the mobility degrades due to the enhanced Coulombic scattering from remote doping. We observed 3% and 10% reduction in electron mobility for the low-mobility and high-mobility 2DEG samples, respectively.

Table 6.1: Effects of SiGe epitaxial regrowth on 2DEG.

Sample		#4478	LJ196
Growth		Princeton CVD	UCLA MBE
Ge content		30%	20%
Spacer thickness (nm)		10	20
Density (cm^{-2}))	Before regrowth	1.16×10^{12}	3.50×10^{11}
	After regrowth	1.47×10^{12}	4.0×10^{11}
Mobility ($cm^2V^{-1}s^{-1}$)	Before regrowth	6,500	290,000
	After regrowth	6,300	260,000

In general, one expects that regrowth has a more detrimental effect on the mobility for high-mobility samples in which remote doping scattering dominates. This can be seen from equation (3.20) and (3.22) in Chapter 3. Diffusion and segregation will reduce the effective spacing thickness h_{eff}. Therefore the mobility component μ_{remote} should decrease with a smaller h_{eff}; while $\mu_{background}$ remains unchanged approximately. From the device aspects even 10% degradation in mobility is acceptable considering the sample-to-sample variations over the wafer scale, other effects due to the later fabrication etc. In addition, the sheet resistance of the sample actually decreased in both cases as a net result because of the increased electron density.

6.3.2 The Leakage Across Si/SiGe Regrown Layers

The second concern of the regrowth is leakage. The regrown layer could add extra leakage paths for electrons. Fig. 6.5 shows an example for regrowth over a strained silicon 2DEG from a side gate to the quantum dot. In the original 2DEG structure,

electrons exist either in the strained silicon channel or in the doped SiGe supply layer due to excess dopants. These electrons can travel through the regrown material from a side gate to the quantum dot and cause extra leakage. In an ideal case both leakage paths would not be conducting at zero temperature. The excess electrons in the supply layer should freeze out if their doping level is below the Mott-transition level. The free electrons in the Si channel should not tunnel through the SiGe due to the barrier from the conduction band discontinuity. However, with the possible defects at the interfaces, the band discontinuity might not suppress the current, which could be caused by the dislocation "pipes" similar to the substrate leakage issue that was addressed in Chapter 3. We will perform electrical measurement to test such leakage.

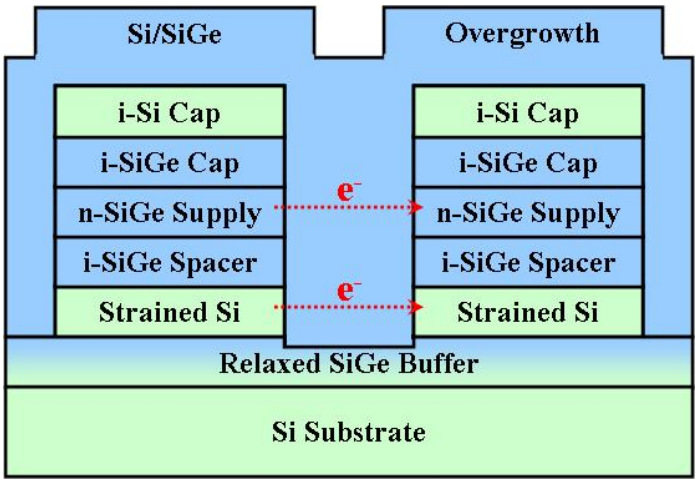


Figure 6.5: Schematic view of SiGe epitaxial regrowth over an etched 2DEG showing possible new leakage paths for electrons. (For example, from a side gate to a laterally adjacent quantum dot.)

We measured the leakage current after regrowth across narrow gaps of two different sizes etched into a conducting path of 2DEG. The first gap is about 2 μm wide, defined by optical photolithography. The second gap is only about 100 nm wide, defined by e-beam lithography. Fig. 6.6 shows the I-V characteristics across gaps of the two different sizes. The substrate was floating. More leakage was found at smaller gap sizes by comparing the leakage current from Fig. 6.6 (a) and (b). For the submicron scale that is more relevant for quantum dot applications, up to 0.5 V

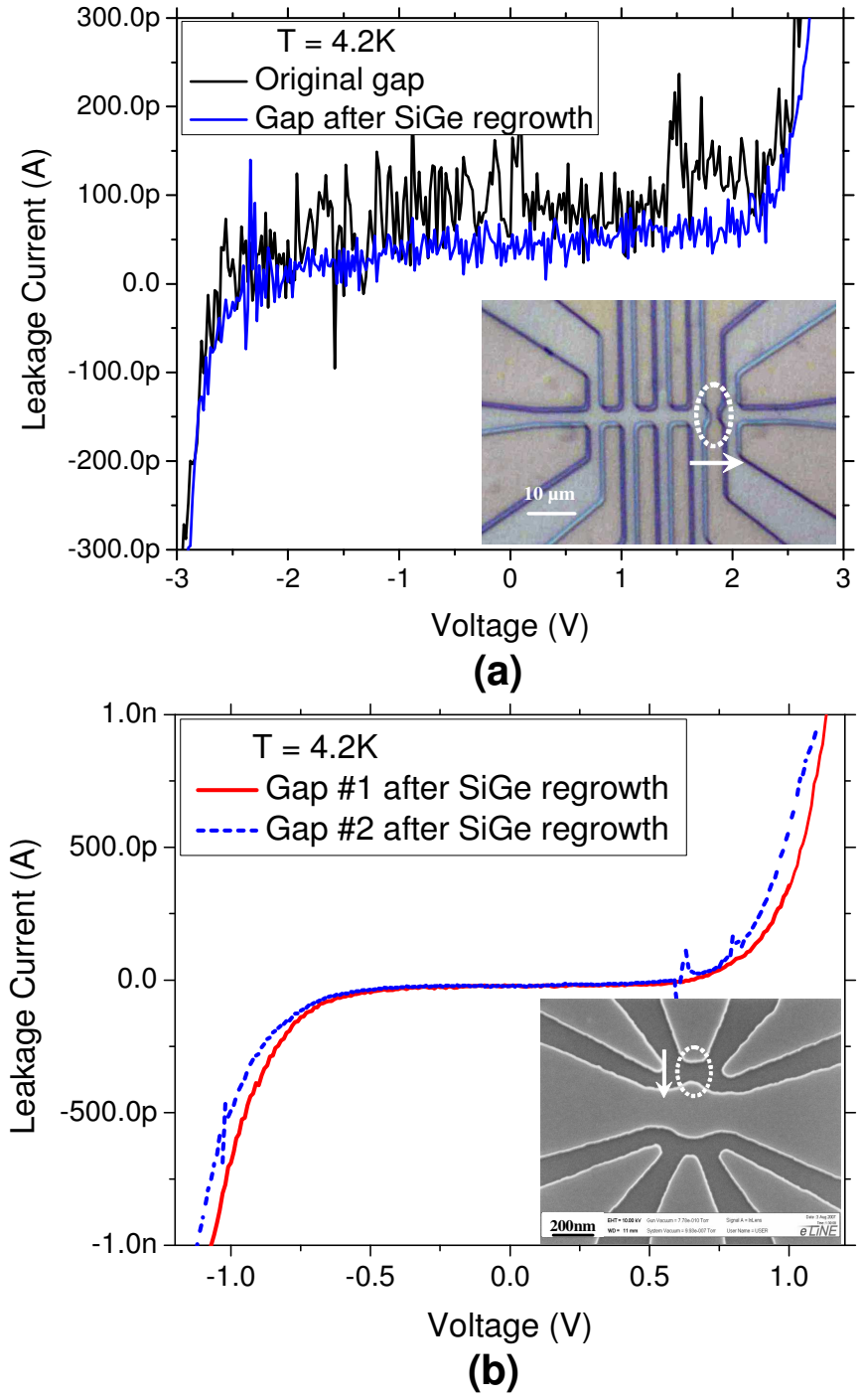


Figure 6.6: I-V curves of the leakage current vs. gate voltage across narrow gaps of (a) micron scale (2 μm defined by optical lithography); (b) sub-micron scale (100 nm defined by e-beam lithography).

of voltage can be applied on the side gate with the leakage current less than 100 pA, and current less than 1 nA for up to 1 V. From Fig. 6.6 (a) we can also see that the regrowth process does not significantly affect the leakage magnitude. Thus the dominant leakage should be from the strained Si 2DEG layers to the relaxed SiGe buffers, which was not affected by the regrowth process.

Therefore, with the regrowth technique the patterned nanostructures with narrow gaps can be used for side gating if the voltage applied is within ± 1 V. The gate leakage is sufficiently low. The gate voltage would be high enough for planar gates to be used to modulate the electrostatic potential and electron density of the strained Si 2DEG.

6.4 Summary

In this chapter we developed a novel Si/SiGe epitaxial regrowth technique for surface passivation on quantum dot devices. The motivation is to achieve perfect surface/interface control that can eliminate trapping/detrapping of carriers due to the presence of defects and surface states. Our approach is to regrow epitaxial Si/SiGe over the patterned devices.

We first investigated the growth issues related with the Si/SiGe epitaxial regrowth. A low-temperature bake in hydrogen (less than 850 °C) has shown success in reducing carbon and oxygen contamination without significant dopant diffusion in existing layer structures. Additional thermal etching of surface by chlorine can achieve cleaner surface/interface but will likely cause surface roughness. By choosing proper surface cleaning process, we achieved conformal epitaxial regrowth sidewalls over the whole wafer.

The interface quality and regrown crystalline structure were studied by TEM. We clearly confirmed the single crystalline nature of the regrowth by TEM. However, it

also shows some stacking faults at the vertical sidewall interfaces of regrown SiGe. This may be due to the strain around the strained Si 2DEG channel. By comparing the 2DEG density and mobility with and without regrowth, we found less than 10% degradation of the electron mobility, while the electron density increased slightly. The sample sheet resistivity was reduced as a net result. The leakage in regrown side-gating structure is negligible if the voltage applied is within ± 1 V, which is reasonabe for tuning the potential of the patterned quantum dot devices.

In conclusion we have demonstrated successful SiGe/Si epitaxial regrowth for surface passivation of Si/SiGe quantum dot applications to avoid potential defect states. Such passivation will hopefully reduce the undesirable surface effects, so that improvement in the device characteristics can be expected.

Chapter 7

Characterization of Quantum Dot Devices

7.1 Introduction

The quantum dot, as the name suggests, represents a tiny region of matter only a few atoms across, in which carriers are confined in all three spatial dimensions. The term "Quantum Dot" was coined by Texas Instruments scientists Mark Reed et al. [120], who is now a professor at Yale University. Semiconductor quantum dots provide highly tunable structures for trapping and manipulating individual electrons. Such quantum dots are proposed to function as "qubits" to achieve semiconductor-based quantum computation, which may eventually replace today's transistors, just as transistors replaced the vacuum tubes half a century ago. In the past several years, the development of Si/SiGe quantum dots have made significant progress.

So far in this thesis we have already addressed technology issues ranging from material growth and regrowth quality to fabrication techniques such as gating and nanopatterning. In this chapter, we will demonstrate simple quantum device applications of these technologies. Two types of devices are of special interest: the quantum

point contact (QPC) and the single-electron transistor (SET).

A QPC consists essentially of a short, narrow constriction connecting two conducting reservoirs. In a QPC, quantized conductance is observed as a result of the 1-D quantization, which directly proves the ballistic transport process. QPCs are often used as mesoscopic charge sensors adjacent to quantum dots for a noninvasive read-out of the spin state [121]. In Si/SiGe heterostructures, QPCs were first fabricated by a metal split-gate [122]. Wet-chemical etch-defined Si/SiGe QPCs have also been reported, in which the 1-D subband energy spacing was successfully extracted [123].

A single Si/SiGe quantum dot is a special type of SET with carrier confinement in all three dimensions. It consists of two tunnel junctions on both sides of a quantum dot. The electrical potential of the dot can be tuned by a coupled gate. The dot may contain zero, a few, to a few thousand carriers. The single electron tunneling effect is significant. The coulomb blockade effect will cause oscillations in the QD conductance as a function of the gate voltage. For the purpose of quantum computing, quantum dots are the key component at the heart of quantum information processing. For example, Loss and DiVincenzo themselves proposed to realize the qubit as the spin of the excess electron on a single-electron quantum dot [13]. SET development in Si/SiGe is not as established as those for III-V materials. The fabrication of Si/SiGe quantum dots using both Schottky top-gating [58, 59] and etch-defined side-gating [124] were reported recently, while there also exist more sophisticated schemes mixing of both trench isolation and Schottky gating [125, 126]. It is noteworthy, although most people propose to use a double-dot device of two laterally coupled single dots for spin exchange operations, with our proposed novel double quantum well structures described in Chapter 4, a single QD without any gate may be sufficient for such interaction functions.

7.2 Charactierizaton of Quantum Point Contact Devices

7.2.1 A Single Quantum Point Contact Device

We combined e-beam lithography, RIE and selective wet etching to fabricate single QPC devices on a Si/SiGe 2DEG. The 2DEG sample #4491 had a 2-D electron density of 1.5×10^{12} cm^{-2}, and a low-temperature mobility of $\mu = 6400$ cm^2/Vs. The details of the fabrication techniques were discussed in Section 5.3.1 of Chapter 5. A shallow RIE followed by $HF/H_2O_2/CH_3COOH$ and TMAH etching were used to etch the narrow gaps. After the lithography, the sample surface was passivated by epitaxial regrowth of 50 nm $Si_{0.7}Ge_{0.3}$ followed by a thin Si cap. Finally, ohmic contacts to the 2DEG were formed by lift-off of AuSb evaporation and forming gas anneal at 400 °C for 10 min.

Fig. 7.1 shows a SEM image of the completed QPC device. The confinement of the channel is about 200 nm wide. The 2DEG itself was also used for side-gating by etch-defined lateral gates that are placed about 200 nm away on both sides from the central channel area. Electrical measurements were conducted at 1 K in a dilution refrigerator by Professor Leonid Rokhinson's laboratory at Purdue University.

Our measurement of channel conductance with applied side-gate voltage is shown in Fig. 7.2. The side gates work well up to ±2 V with gate leakage less than 1 nA. At a gate voltage of –2.2 V pinch-off is reached, the channel constrictions become completely depleted and the channel is shut off.

In an ideal semiconductor QPC structure, one of the most striking features was the discovery of the conductance quantization in units of $2e^2/h$ as the gate voltage is swept in the absence of a magnetic field [127, 128]. The factor 2 comes from the spin degeneracy $g_s = 2$. In SiGe heterostructures, the additional valley degeneracy $g_v = 2$ will lead to a total conductance quantization in multiples of $4e^2/h$. In our

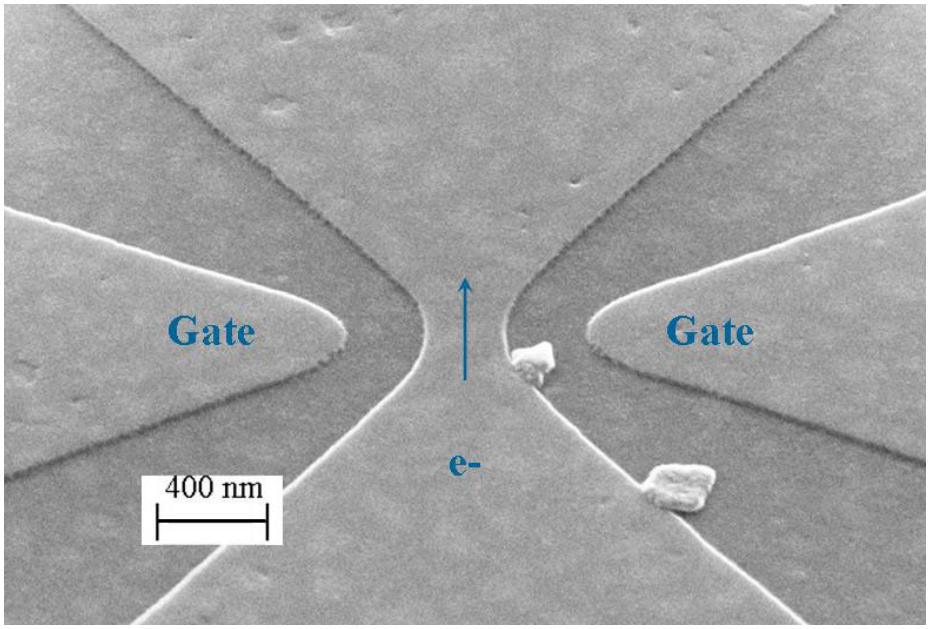


Figure 7.1: A SEM image of Si/SiGe QPC patterned by low-damage wet etch and epitaxial dot passivation.

QPC devices, the quantization of conductance at $G = 4e^2/h$ is missing, and a fairly flat plateau at $G = 2 \times 4e^2/h$ is observed. The discrepancy between the conductance quantization measure in our QPC and that from a high quality QPC is due to the low electron mobility, which can cause the electron transport in the confined QPC region to deviate from ballistic. We will evaluate the ballistic transport assumption by first calculating the electron mean free path.

In a 2DEG, the electron scattering rate can be derived from the measured mobility:

$$\mu = \frac{e\tau}{m^*} \Rightarrow \tau = \frac{\mu m^*}{e}. \tag{7.1}$$

An estimate of the elastic mean free path can then be calculated by assuming a Fermi velocity between scatterings:

$$\lambda_{elastic} = v_{Fermi}\tau = \frac{\hbar\mu}{e}\sqrt{\frac{4\pi n_{2D}}{g_s g_v}}. \tag{7.2}$$

For the 2DEG sample #4491, using parameters μ and n_{2D} as mentioned above,

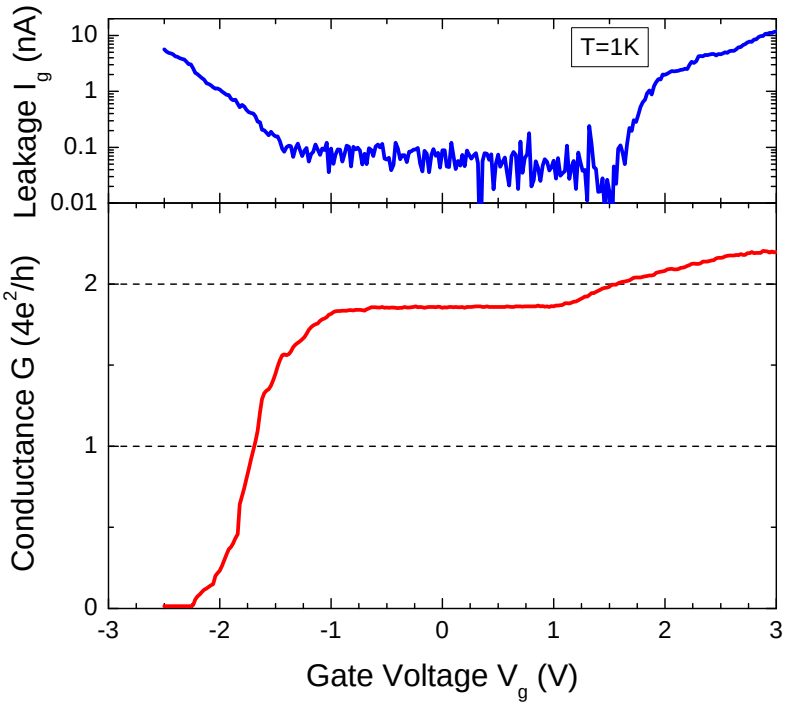


Figure 7.2: Channel conductance and leakage current through the gate in a quantum point device as a function of the applied gate voltage at zero magnetic field.

and $g_s = g_v = 2, m^* = 0.19\ m_0$, we found the electron mean free path $\lambda_{elastic}$ to be 92 nm, which is comparable but certainly smaller than the QPC feature size of about 300 nm. Therefore, the electron transport through our quantum point contact devices is not totally ballistic. To observe ballistic transport, higher mobility 2DEG or smaller QPC confinement size by a factor of at least three are needed, and will be a subject of future work.

7.2.2 Quantum Point Contacts Used as Tunnel Junctions in A Quantum Dot

The successful pinch-off of QPC has allowed us to fabricate more complicated quantum dot devices with etch-defined side gates in 2DEG itself. Fig. 7.3 shows a SEM

image of a single quantum dot confined with six etch-defined side gates. The quantum dot is fabricated on 2DEG sample #4811 with an electron density of 8×10^{11} cm^{-2}, and a low-temperature mobility of $\mu = 6800$ cm^2/Vs. We used only one dry etch (CF_4/O_2 RIE, see Section 5.3.2 of Chapter 5) to define the quantum dot area. The high etching anisotropy has enabled us to achieve a channel width as narrow as 150 nm and a gap width below 100 nm between the channel and gates. Epitaxial regrowth SiGe was done to passivate the dot surfaces.

In such a quantum dot structure, the two quantum point contacts (confined between gate 3 - 11, and 5 - 9, as labeled in Fig. 7.3) are intended to define tunnel junctions between the dot and the source/drain. The other pair of split gates 4 - 10 is used to tune the electrical potential of the dot. Before we move to more complicated quantum dot characteristics, each individual side gate was electrically tested independently, i.e., when a voltage is applied to one gate all other side gates are grounded.

Fig. 7.4 shows the channel conductance with applied gate voltage on each individual side gate at 4.2 K. First we noticed that all side gate are normally "off". When no voltage is applied the channel is pinched off. This can be attributed to the surface depletion induced by the ion damage during the dry etch. A positive gate voltage of a typical value of 0.4 V is required to remove such depletion regions. Second, since the tunneling junction area and even the central dot are small, we observed some channel conductance characteristics similar to the quantization in a single QPC. Especially when the channel is tuned by gate 3, a nice conductance plateau at $G = 4e^2/h$ is clearly present. Due to the low mobility and the presence of possible electrical damage near the edges, we do not expect the electron transport to be totally ballistic. The fact that all six side gates are working properly with complete pinch-off and sufficiently low leakage is very promising for our further pursue of quantum dot devices.

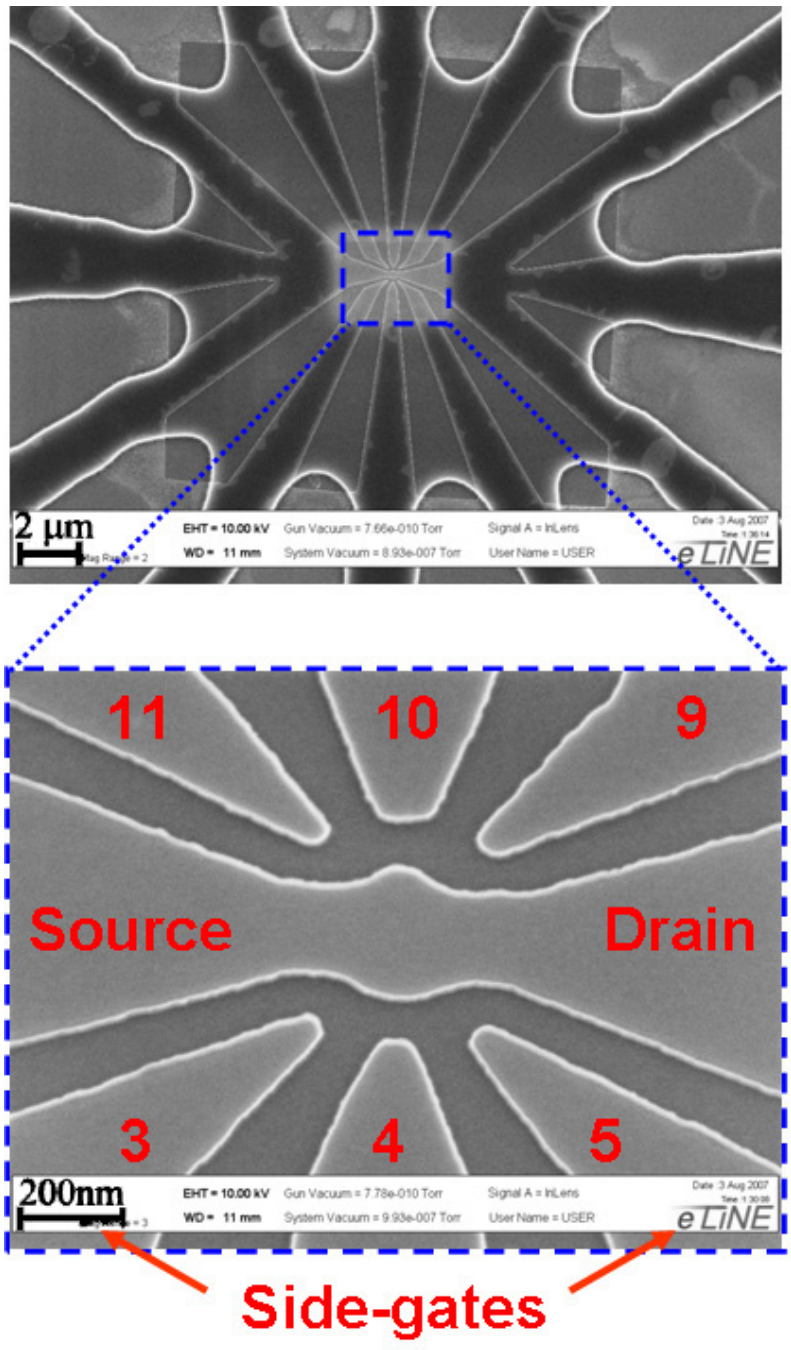


Figure 7.3: A SEM image of a single Si/SiGe quantum dot with six side gates patterned by RIE dry etch and epitaxial regrowth.

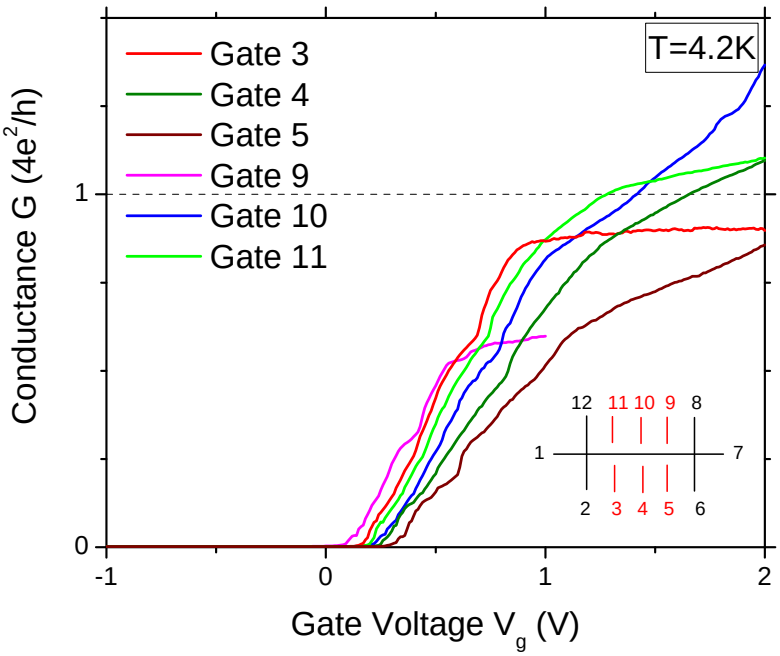


Figure 7.4: Channel conductance in a quantum dot device at T = 4.2 K as a function of the applied gate voltage at zero magnetic field. When a voltage is applied to each individual gate, all other five side gates are held grounded.

7.3 Characterization of Single Quantum Dot Devices

7.3.1 Coulomb Blockade and Quantum Dot Energies

Fig. 7.3 shows a single quantum dot, which contains a small island which is coupled to electron reservoirs through two tunneling junctions. Such a quantum dot is one of the simplest devices that exhibit Coulomb Blockade (CB), a single electron tunneling effects.

Fig. 7.5 describes the energy levels in a single quantum dot system. Assuming the energy spacing ΔE in the dot is greater than the thermal energy for low temperatures, electron transport through the dot is determined by Coulomb charging. When the

applied source-drain bias is small, in the blocking state, there are no accessible energy levels within tunneling range of electrons from the source to the drain. All energy levels on the dot with lower energies are occupied, as a result no current can flow.

When a gate voltage is applied so that the energy levels of the dot are lowered and a previous vacant level is brought within the source-drain bias, the electron can now tunnel onto the island then from there it can tunnel onto the drain. This is the transmitting state of the dot, and the conductance will become non-zero. Sweeping the gate will change the total number of occupied states of the dot and thus the conductance has periodic peaks rising from zero to a set of sharp peaks.

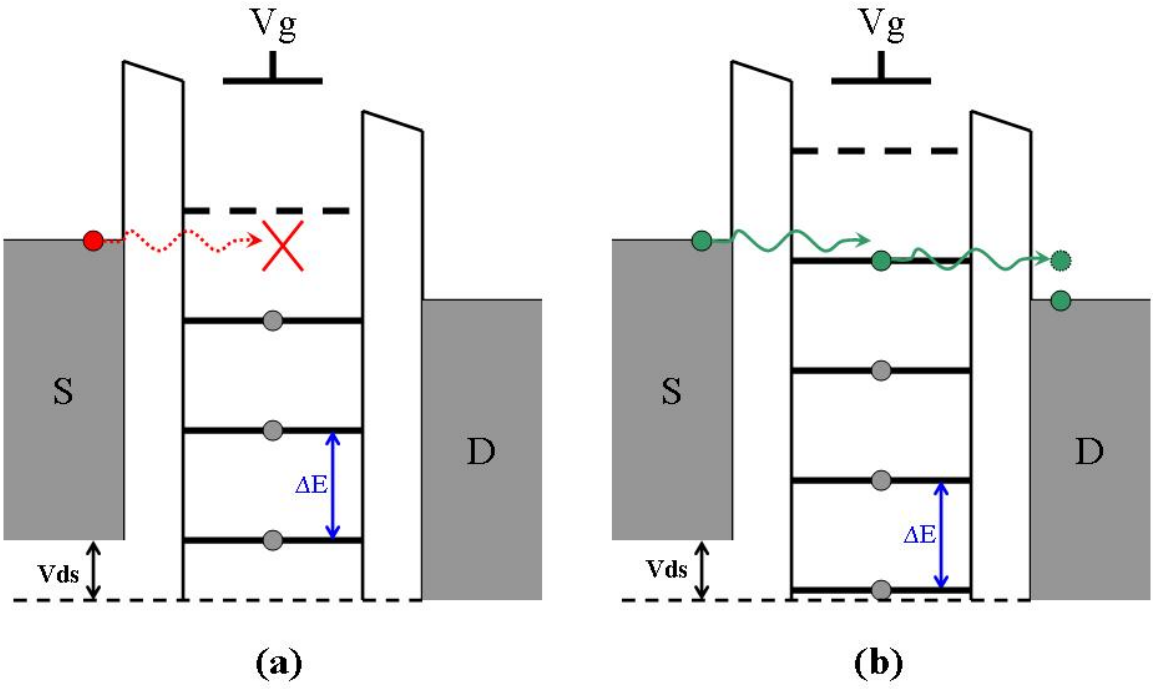


Figure 7.5: Energy levels of a single quantum dot for (a) the blocking state, and (b) the transmitting state.

The energy spacing of the levels in the quantum dot is defined as the "addition energy", and it can be estimated by the sum of the "charging energy" and the quantum well energy spacing. Since the dot has a finite capacitance C, to add one electron costs a charging energy of e^2/C. The second term $\Delta\epsilon$ origins from the splitting between the energy quantization in the quantum well itself, and can be computed from solving

the eigen-energies in a 2-D square potential well, for example. Therefore,

$$\Delta E = e^2/C + \Delta\epsilon. \tag{7.3}$$

The dot's self-capacitance can be estimated with a simplified isolated thin conducting disk model. If the disk has a radius of r in a dielectric-filled space, its capacitance is given by

$$C = 8\epsilon_r\epsilon_0 r. \tag{7.4}$$

For an estimate of $\Delta\epsilon$, since the energy levels for 2D-confined electrons are give by

$$E_{2D} = \frac{\hbar^2}{2m}\left[\left(\frac{2\pi n_x}{2r}\right)^2 + \left(\frac{2\pi n_y}{2r}\right)^2\right], n_x, n_y = 0, \pm 1, \pm 2, \ldots, \tag{7.5}$$

where 2r is the length of the 2D box. For a system that contains only a few electrons, the energy spacing can be assumed approximately to be a constant

$$\Delta\epsilon \approx \hbar^2/m^* r^2. \tag{7.6}$$

The total addition energy in a single quantum dot is now

$$\Delta E = \frac{e^2}{8\epsilon_r\epsilon_0 r} + \frac{\hbar^2}{m^* r^2}. \tag{7.7}$$

In a strained silicon dot the addition energy is very sensitive to the dot size, as shown in Fig. 7.6. From the graph we can see that the dominant component of the addition energy is the charging energy for a dot size over a few nm. For a dot size of r = 100 nm, the estimated addition energy is around 2 meV. In real quantum dot devices with complex structures and interfaces, the dot is coupled to nearby source, drain and gates rather than isolated. For side-gated devices surrounded by trenches, the interfaces also have a strong effect. The general form of the dot capacitance can

be written as

$$C_{dot} = C_{source-dot} + C_{drain-dot} + C_{gate}. \tag{7.8}$$

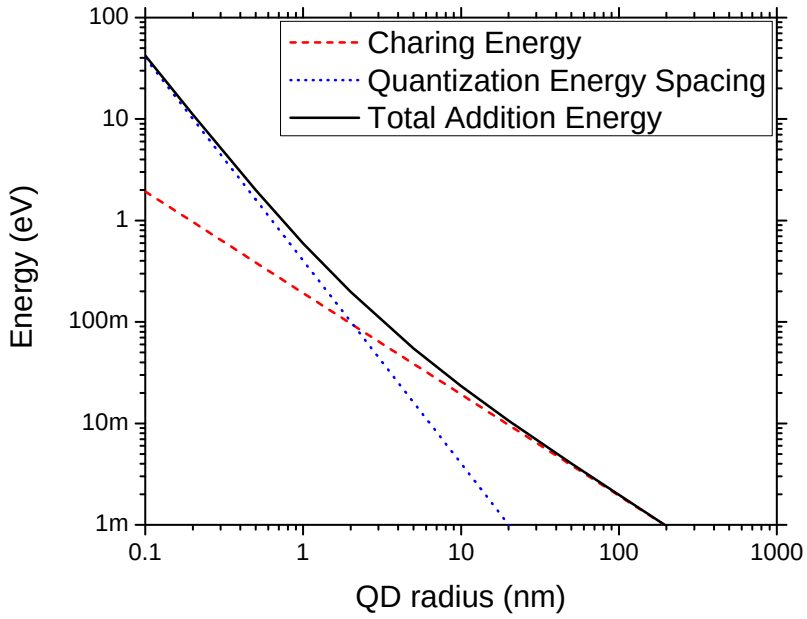


Figure 7.6: Addition energy in a silicon quantum dot and its components of charging energy and quantization energy spacing as a function of dot size.

Finally we list the three criteria that have to be met to achieve observable Coulomb blockade:

1. The source-drain bias voltage can't exceed the addition energy.

2. The thermal energy k_BT must be below the addition energy, or else electrons will be able to suppress blocking via thermal excitation.

3. The tunneling junction resistance should be greater than h/e^2, which is a result from the uncertainty principle.

7.3.2 A Single Quantum Dot Device

As the final quantum dot device application of this thesis, we will describe a single quantum dot device characteristics. The fabrication details and a SEM image were discussed in Section 7.2.2. Electrical measurements were conducted at 30 mK in a dilution refrigerator by Professor Leonid Rokhinson's laboratory at Purdue University.

In the original quantum dot design, the two pairs of split gates on the sides were intended to be used for controlling the tunneling junction and define the central dot area, with one pair each is placed on the source and drain sides. However, in the measurement we encountered great difficulties in locating the exact dot. When any of two pairs of the split gates were applied a fixed voltage, sweeping voltage on the remaining pair of split gate would show similar conductance oscillation behavior. We think this could be caused by three possible problems. First, as shown in Fig. 7.4, our tunneling junctions are normally "off". So there could be many possible tunnel junctions in the narrow etch-defined region even without the side gates, the tunnel barriers in these junction will be high enough. If this is true, any pair of the split gates could define a quantum dot if there are two tunneling junctions close enough on both the source and the drain sides. Second, our achieved mobilities in these samples are still low so that the electron mean free path is less than 100 nm. The inelastic scatterings may be significant within the quantum dot area and effectively alter the dot size. Third, this particular single quantum dot sample #4811 was etched only by RIE, the surface depletion and possible defects from the ion damage will form a lot of charge traps. Such traps could also change the dot geometry significantly. Moreover, the conductance blockade in our measurement showed a lot of parasitic patterns such as missing or extra peaks as well as hysteresis due to the existence of the excess electron traps.

Fig. 7.7 shows typical conductance oscillations through the quantum dot as the voltage on one pair of side split gates is varied. The source-drain bias was held

constant at V_{DS} = 10 mV. When the gate voltage on the dot is less than –0.5 V, we did not observe any channel conductance which suggests there is no electron on the dot. As the gate voltage increases, both scans exhibit a few initial oscillation peaks with similar positions and linewidths. We believe that these successive peaks correspond to an increment of one electron in the dot [129]. After passing about eight quantized electron states on the dot, we find many parasitic peaks and strong hysteresis from the two scans, presumably due to the increased electron interactions between the electrons on the dot with the surrounding environment as well as among themselves.

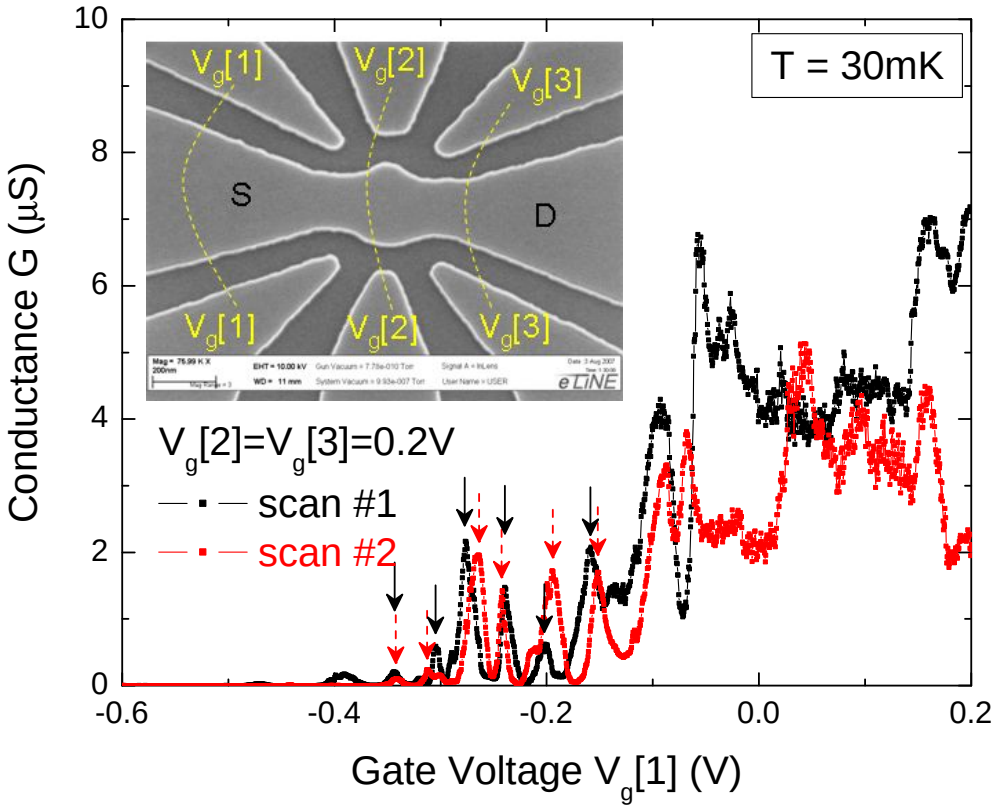


Figure 7.7: Quantum dot conductance oscillations as the gate voltage on split gate $V_g[1]$ is varied with zero magnetic field at T = 30 mK. The arrows indicate the positions of conductance peaks that were included to calculate the gate capacitance.

To further study the gate capacitance in our single quantum dot devices, we choose to fit the first six conductance oscillations from both scans with a Lorentz broadening model. The underlying equation for data fitting is

$$G = G_0 + \frac{2A_i}{\pi}\frac{w_i}{4(V - V_{ci})^2 + w_i^2}, i = 1, 2, \ldots, 6, \tag{7.9}$$

where G is the conductance axis and V is the gate voltage axis.

We assume $G_0 = 0$ for both curves. The fitted V_{ci} and w_i correspond to the peak positions and their full width at half magnitude (FWHM), respectively. Table 7.1 summarizes the numerical results. The average spacing between consecutive peaks ΔV_g is about 36 mV, which is governed primarily by the gate capacitance

$$C_{gate} = \frac{e}{\Delta V_g} = 4.4\ aF. \tag{7.10}$$

Table 7.1: Fitted curve parameters of quantum dot conductance oscillation peaks (All units are in Volts).

	Scan #1			Scan #2		
i	V_i	FWHM w_i	$\lvert V_i - V_{i-1}\rvert$	V_i	FWHM w_i	$\lvert V_i - V_{i-1}\rvert$
1	-0.3436	0.0052		-0.3415	0.0041	
2	-0.3043	0.0041	0.0393	-0.3115	0.0044	0.0300
3	-0.2754	0.0119	0.0289	-0.2659	0.0130	0.0356
4	-0.2383	0.0071	0.0371	-0.2418	0.0044	0.0241
5	-0.2020	0.0048	0.0363	-0.1952	0.0146	0.0466
6	-0.1568	0.0242	0.0452	-0.1510	0.0108	0.0442
Average	$\lvert\Delta x_i\rvert = 0.037 \pm 0.006$			$\lvert\Delta x_i\rvert = 0.036 \pm 0.009$		

The resulting gate capacitance is on the order of 11 aF reported in a similar etch-defined six side-gate dot by other groups [130]. Due to the charge noise and poor stability in this particular single quantum dot device, we were not able to further identify Coulomb blockade diamonds [129] by varying both side-gate voltages and the source-drain voltages simultaneously, which prevents us from experimentally extrapolating the total dot capacitance and the addition energy.

In the six-gate dot fabrication work [130], it was also noted that the CF_4 etch which we used as well can cause a higher density of trapping states, and a correspondingly larger depletion width. Although we performed regrowth and the work [130] did not, any etch damage defects below the surface would not be removed by passivation (excpet perhaps the thermal annealing effect of the pre-expitaxial cleaning step). We believe that the lack of precise surface control is our current limiting factor that led to suppression of Coulomb blockade. We anticipate that improvements in dry etching technique facilitated by a shallow wet-etch will enable continued progress towards clean quantum dot devices.

7.4 Summary

With respect to technology, we have developed a versatile side-gated strained Si/SiGe quantum dot devices fabrication process. Two rudimentary types of device applications are presented as prototype of functionality that exhibits significant quantum effects: the quantum point contact (QPC) and the single quantum dot.

A single QPC device was fabricated with selective wet etch and Si/SiGe epitaxial regrowth. The channel can be fully depleted with negative gate voltage beyond –2 V. Strong evidence of 1-D quantization in the QPC channel was identified, as more positive gate voltage applied the conductance showed steplike conductance characteristics. The poor electron mean free path in our 2DEG samples will require a fabrication resolution well below 100 nm to achieve ballistic transport. With the successful demonstration of the QPC, we can use multiple side-gates close to a quantum dot to tune the electrostatic potential on the dot as well as the tunnel couplings between the dot and its source and drain. Successful pinch-off of all side gating in a six-gate quantum dot geometry were demonstrated, while the source-drain transport conductance $< e^2/h$ can be maintained so that the dot was weakly coupled with

tunnel junctions to the source and drain.

In the six side-gate single quantum dot device, we observed channel conductance blockade behavior with periodic oscillation peaks while sweeping each pair of split gates and keeping all other gate voltages constant. This is a direct result of Coulomb blockade effect, in which the addition energy of the dot is much larger than the source-drain bias and the thermal energy so that single electron tunneling can only occur within certain energy level alignment. By calculating the gate voltage spacings between adjacent conductance peaks, we estimated a typical gate-to-dot capacitance of about 4.4 aF for each pair of side gates. The detailed Coulomb blockade diamond characteristics was suppressed by the excess parasitic charge noise and hysteresis of different scans. Thus the surface passivation by Si/SiGe epitaixal regrowth itself may not be sufficient to remove the ion damage and surface depletion arising from the use of RIE, low-damage dry etch chemistry and/or the use of a shallow wet etch is desirable for future quantum dot device applications.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

The motivation of this work is to explore the physical realization of a silicon-based electron spin-based quantum computer to meet the ever-growing computation and information processing needs. We focus on the epitaxial growth and nanofabrication technologies for modulation-doped Si/SiGe heterostructures because of their straightforward potential towards large-scale integration and manufacturing. The main contribution of this work is threefold. First, we developed a complete growth and fabrication flow for both mesoscopic physics studies and quantum dot device applications in Si/SiGe heterosturctures. Second, we experimentally fabricated and studied electron transport in double quantum well 2DEG structures. They are good candidates of quantum dimers for the physical implementation of a scalable architecture map of qubit devices. Third, we demonstrated the three-dimensional confinement and surface passivation of quantum dot devices with a novel Si/SiGe epitaxial regrowth technique. In addition, uniform high-κ gate dielectric deposition was developed for additional passivation and top-gating.

Three similar but distinctive Si/SiGe epitaxy cycles have been implemented and

optimized for their roles at different fabrication stages. The growth of SiGe relaxed buffers is optimized for low dislocation density while maintaining a high throughput by our collaborators at AmberWave Systems. At Princeton, the growth of the modulation-doped Si/SiGe heterostructures is optimized for 2DEG that allows meaningful transport properties without sacrificing electron density depending on specific desired quantum devices applications. The growth conditions for the final epitaxial regrowth passivation require minimal thermal treatment and deleterious interfacial effects. The main challenge for devices fabrication process remains in the development of a viable etching technique for high anisotropy and low damage. While existing reactive ion dry etching is the most prevalent and advanced choice, we feel the urgent need for a breakthrough with non-selective etch chemistry with regard to SiGe and possible inclusion of a shallow wet etching.

On the new scalable architecture map for implementation of the Loss-DiVicenzo silicon-base quantum computer, our key contribution is the proposed concept of 3-D confined "double quantum dot" dimers that can eliminate gating for precise control of exchange couplings in a qubit array. We presented a theoretical study of the band alignment and the interwell interactions in two possible double quantum well structures. A negative transconductance effect was observed experimentally in a top-gated asymmetric double quantum well to show a strong evidence of interactions between the delocalized electrons in the two wells. At present, more understanding of the double quantum well interactions and the transport properties is required before the dimers can be integrated in the arrangement of many qubits.

Finally, a pseudomorphic epitaxial step by Si/SiGe epitaxial regrowth is demonstrated for device surface passivation and 3-D confinement of quantum dot devices. Such a epitaxial regrowth can provide a conduction band discontinuity at the strained Si/regrown SiGe interfaces and in principle avoid surface states and electrically active defects. We also developed a low temperature atomic layer deposition of Al_2O_3 rou-

tine that enables final surface passivation and top gating in addition to existing side gating. Quantum dot devices applications such as quantum point contacts and single electron transistors based on nanolithography and Si/SiGe exitaxial regrowth were demonstrated. The observation of single electron tunneling effect certainly shows significant prospects for future fabrication of quantum computing circuits.

8.2 Future Work

We already addressed many of the possible future directions throughout this thesis. In the following section, we will list some of these aspects that are of considerable research interest.

8.2.1 Short-term Outlook

This thesis raised some specific issues concerning our Princeton RTCVD system. It is clear that background doping limits our achieved electron mobilities, we have to adapt improvements by modifying growth conditions, introducing new silicon/germanium gas precursors, and hardware upgrades such as additional gas purification. The *in situ* etching with chlorine-based gas chemistry is also worth closer investigations. With a better understanding of selectivity and the etching mechanism, it may be possible to overcome the roughness problem and develop a reproducible cleaning procedure for growth and regrowth with superior interfacial qualities.

Further assistance from experiments is needed to harness double quantum wells for exchange interactions of electrons. These experiments should follow and focus on magneto-transport measurement, from which the individual electron densities and mobilities in the double wells can be derived directly. In addition, by introducing a SiGe alloy with a small amount of Ge in one of the double quantum wells (Fig. 8.1), we hope to find extra signatures of electrons in the two quantum wells. The electrons

confined in the $Si_{0.95}Ge_{0.05}$ should have a much lower mobility, if the alloy scattering other than the Coulombic scattering limits the mobility. Therefore a larger negative transconductance effect can be expected. Also electrons in the double quantum wells should have very different g-factor shift with respect to the direction of external magnetic field, so electron spin resonance spectrum can also be a convenient tool to monitor electron occupancy in the two wells.

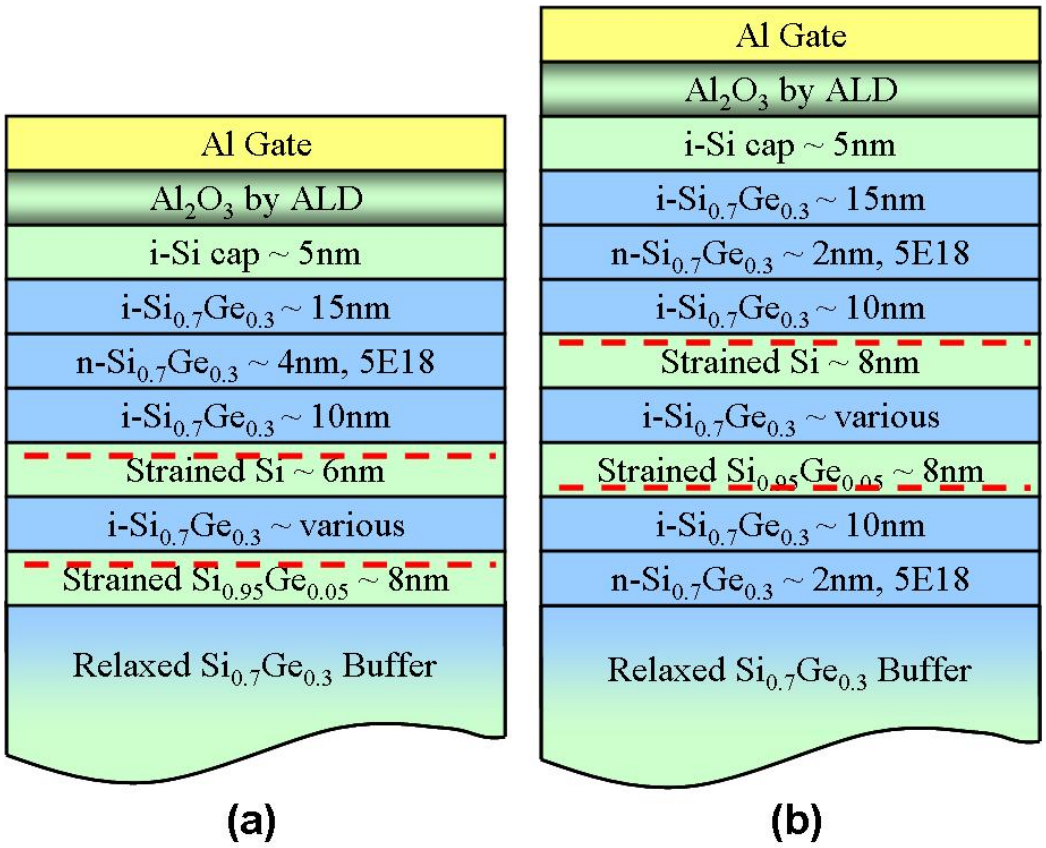


Figure 8.1: Schematic view of layer structures of two gated double quantum well systems with one SiGe alloy well: (a) asymmetric DQW with only one supply layer, (b) symmetric DQW with double supply layers.

The final concern is the successful fabrication of quantum dots, either based on single quantum well 2DEG (for qubit) or double quantum well 2DEGs (for interation dimer), as the implementation of our "flying qubit" architecture or essentially any silicon-based quantum computers will rely on such building blocks. Quantum point contacts or similar 1-D conducting wires with various width shall be first studied for

better control of edge depletion and any other surface effects. Consequently, we hope that we can remove the surface depletion and avoid the parasitic and hysteresis effects in quantum dot and observe Coulomb blockade diamonds.

Fig. 8.2 shows a prototype device of a more ambitious double quantum dot. The device consists of a central dot of vertical double quantum wells, a top gate for tuning the interaction between the two wells, and three side gates (or alternatively, using a more complicated six-gate geometry) for tuning the tunneling junctions and the electrostatic potential of the dot. For simplicity, the Si/SiGe epitaxial regrowth passivation is not shown. While either top-gating nor side-gating is not required for the interaction dimers for our "flying qubit", the versatility will be potential useful for study many-body physics, for example, the direct measurement of symmetric anti-symmetric splitting, and electron spin-relaxation times in such a two-level system.

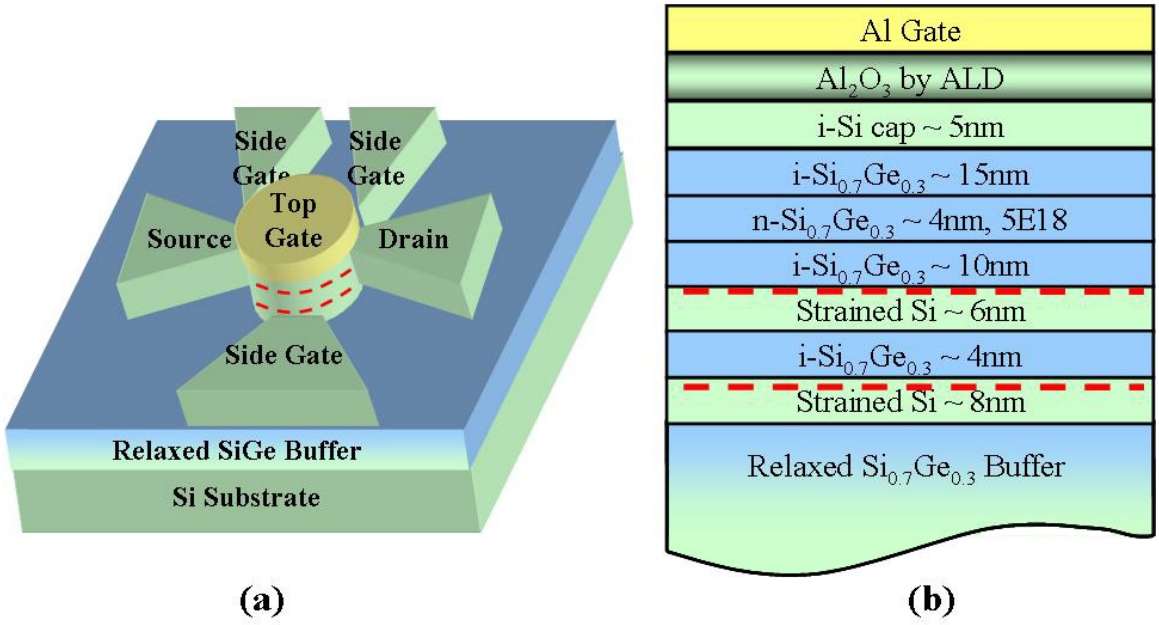


Figure 8.2: (a) Top-view of a double quantum dot based interaction dimer device. (b) Schematic, cross-sectional view of the central quantum dot in the interaction dimer device.

8.2.2 Long-term Outlook

In this thesis our emphases are on epitaxy and nanofabrication for the side gating of modulation-doped Si/SiGe heterostructures for implementation of silicon-based qubit and quantum devices. Meanwhile the other different, but similarly promising Schottky top-gating approach has made considerable progress. Our fabrication techniques, in particular, the Si/SiGe epitaxial regrowth and ALD Al_2O_3 passivation, could definitely be implemented in top-gated quantum dot devices as well. As one example, Fig. 8.3 shows a novel multiple quantum dots defined by Schottky gating across a nanowire of Si/SiGe modulation-doped heterostructures. The use of Si/SiGe epitaxial regrowth prior to the gate fabrication will provide a sharp 3-D confinement to electrons in the nanowire due to conduction band discontinuity, and also a surface passivation to eliminate defects and interface states. It might be simpler to implement than the quantum dot structures described in Chapter 7 because it does not depend on the properties of a narrow gap, making e-beam lithography and etching easier in practice because of a more tolerable process window.

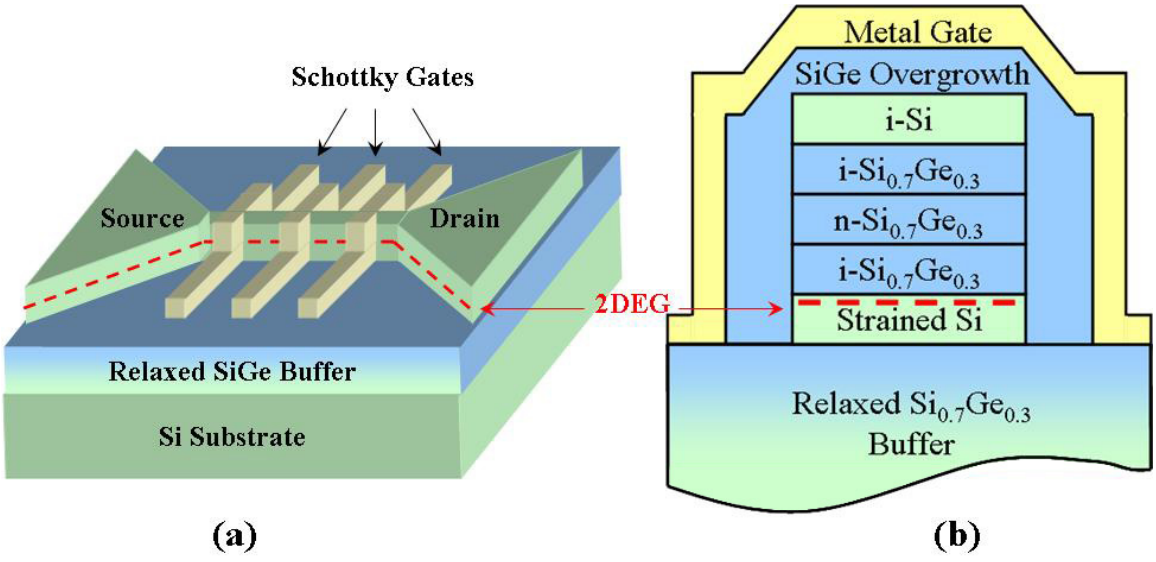


Figure 8.3: (a) A multiple quantum dots device defined by Schottky finger gates on a nanowire. (b) Schematic view of the Si/SiGe heterostructure nanowire with epitaxial regrowth passivation.

With the successful realization of two-level quits and the logic operations of these qubits, the experimental results should help us to answer two critical questions about the ultimate feasibility of electron spin-based quantum computing. The first one is a fundamental physics question: what is the quantum decoherence time in these Si/SiGe qubits? Given this much sought quantity, we can then turn to the second technology question: can we achieve an error rate low enough for precise control of exchange interactions of these qubits? The answer to the second question will depend on high-speed pulses and voltage amplitude control of the gates. For example, for a target rate error rate of 10^{-5} or less per gate, controlling the exchange will require pulse edges to be defined to better than 10^{-5} of the decoherence time with gate amplitude switched to approximately less than 50 dB of the peak. With favorable answers to both questions, we are confident that all of the five Loss-DiVincenzo's criteria can be met and quantum computing will no longer be a fantasy or mirage.

If indeed a quantum computer is fantasy or mirage beyond what we can currently envision, the rich variety of phenomena in the field is still sure to be a source of inspiration for the future.

> 'Would you tell me, please, which way I ought to go from here?'
>
> 'That depends a good deal on where you want to get to,' said the Cat.
>
> 'I don't much care where–' said Alice.
>
> 'Then it doesn't matter which way you go,' said the Cat.
>
> '– so long as I get SOMEWHERE,' Alice added as an explanation.
>
> 'Oh, you're sure to do that,' said the Cat, 'if you only walk long enough.'

Bibliography

[1] "World's First 2-Billion Transistor Microprocessor", www.intel.com/technology/architecture-silicon/2billion.htm

[2] Manek Dubash (2005-04-13). "Moore's Law is dead, says Gordon Moore". Techworld.

[3] P. W. Shor, SIAM J. Computing **26**, 1484 (1997); quant-ph/9508027v2 (1996).

[4] C. H. Bennett and D. P. DiVicenzo, Nature **404**, 247 (2000).

[5] J. I. Cirac and P. Zoller, Phys. Rev. Lett. **74**, 4091 (1995).

[6] Q. A. Turchette, C. J. Hood, W. Lange, H. Mabuchi, and H. J. Kimble, Phys. Rev. Lett. **75**, 4710 (1995).

[7] N. A. Gershenfeld and I. L. Chuang, Science **275**, 350 (1997).

[8] A. Shnirman, G. Schön, and Z. Hermon, Phys. Rev. Lett. **79**, 2371 (1997).

[9] Y. Makhlin, G. Schön, and A. Shnirman, Phys. Rev. Lett. **85**, 4578 (2000).

[10] D. V. Averin, Solid State Commun. **105**, 659 (1998).

[11] L. B. Ioffe, V. B. Geshkenbein, M. V. Feigel'man, A. L. Fauchère, and G. Blatter, Nature **398**, 679 (1999).

[12] T. P. Orlando, J. E. Mooij, Lin Tian, Caspar H. van der Wal, L. S. Levitov, Seth Lloyd, and J. J. Mazo, Phys. Rev. B **60**, 15398 (1999).

[13] D. Loss and D. P. DiVicenzo, Phys. Rev. A **57**, 120 (1998); cond-mat/9701055v3 (1997).

[14] D. P. DiVicenzo, quant-ph/0002077v3 (2000).

[15] E. Kasper, H. J. Herzog, and H. Kibbel, Appl. Phys. **8**, 199 (1975).

[16] M. V. Fischetti and S. E. Laux, J. Appl. Phys. **89**, 1205 (2001).

[17] R. Dingle, H. L. Störmer, A. C. Gossard, and W. Wiegmann, Appl. Phys. Lett. **33**, 665 (1978).

[18] J. W. Mattews and A. E. Blakeslee, J. Crystal Growth **27**, 118 (1974).

[19] F. Schäffler, Semicond. Sci. Technol. **12**, 1515 (1997).

[20] D. V. Lang, R. People, J. C. Bean, and A. M. Sergent, Appl. Phys. Lett. **47**, 1333 (1985).

[21] R. Braunstein, A. R. Moore, and F. Herman, Phys. Rev. **109**, 695 (1958).

[22] C. G. Van de Walle and R. M. Martin, Phys. Rev. B. **34**, 5621 (1986).

[23] L. Yang, J. R. Watling, R. C. W. Wilkins, M. Boriçi, J. R. Barker, A. Asenov, and S. Roy, Semicond. Sci. Technol. **19**, 1174 (2004).

[24] S. F. Nelson, K. Ismail, J. J. Nocera, F. F. Fang, E. E. Mendez, J. O. Chu, and B. S. Meyerson, Appl. Phys. Lett. **61**, 64 (1992).

[25] N. Sugii, K. Nakagawa, Y. Kimura, S. Yamaguchi, M. Miyao, Semicond. Sci. Technol. **13**, A140 (1998).

[26] S. F. Nelson, K. Ismail, J. O. Chu, and B. S. Meyerson, Appl. Phys. Lett. **63**, 367 (1993).

[27] J. C. Sturm, P. V. Schwartz, E. J. Prinz, and H. Manoharan, J. Vac. Sci. Tech. B **9**, 2011 (1991).

[28] P. V. Schwartz, "Oxygen incorporation during low-temperature chemical vapor deposition and its effects on the electronic properties of epitaxial Si and $Si_{1-x}Ge_x$ films", Ph.D. thesis, Princeton University (1992).

[29] J. C. Sturm, and C. M. Reaves, IEEE Trans. Electron Dev. **1**, 81 (1992).

[30] R. Westhoff, J. Carlin, M. Erdtmann, T. A. Langdo, C. Leitz, V. Yang, K. Petrocelli, M. T. Bulsara, E. A. Fitzgerald, and C. J. Vineis, in Electrochemical Society Proceedings, Honolulu, 2004, edited by D. Harame, J. Boquet, J. Cressler, D. Houghton, H. Iwai, T. J. King, G. Masini, J. Murota, H. Rim, and B. Tillack, Vol. 7, p. 589.

[31] F. Lukes, J. Phys. Chem. Solids **11**, 342 (1959).

[32] J. Weber and M. I. Alonso, Phys. Rev. B **40**, 5683 (1989).

[33] R. People, J. C. Bean, D. V. Lang, A. M. Sergent, H. L. Störmer, K. W. Wecht, R. T. Lynch, and K. Baldwin, Appl. Phys. Lett. **45**, 1231 (1984).

[34] G. Abstreiter, H. Brugge, and T. Wolf, Phys. Rev. Lett. **54**, 2441 (1985).

[35] H. J. Herzog, H. Jorge, and F. Schäffler, Thin Solid Films **184**, 237 (1990).

[36] G. Schuberth, F. Schäffler, M. Besson, G. Abstreiter,and E. Gornik, Appl. Phys. Lett. **59**, 3318 (1991).

[37] K. Ismail, B. S. Meyerson, and P. J. Wang, Appl. Phys. Lett. **58**, 2117 (1991).

[38] Y. J. Mii, Y. H. Xie, E. A. Fitzgerald, D. Monroe, F. A. Thiel, B. E. Weir, and L. C. Feldman, Appl. Phys. Lett. **59**, 1611 (1991).

[39] F. Schäffler F, D. Többen, H. J. Herzog, G. Abstreiter, and B. Holländer, Semicond. Sci. Technol. **7**, 26 (1992).

[40] A. Yutani and Y. Shiraki, J. Crystal Growth **175-176**, 504 (1997).

[41] H. J. Herzog, H. Jorke and E. Kasper, J. Electrochem. Soc. **136**, 3026 (1989).

[42] K. Sawano, H. Satoh, K. Nakagawa, and Y. Shiraki, Physica E **32**, 520 (2006).

[43] P. Laitinen, I. Riihimäki, J. Räisänen and the ISOLDE Collaboration, Phys. Rev. B **68**, 155209 (2003).

[44] S. Eguchi, C. N. Chleirigh, O. O. Olubuyide, and J. L. Hoyt, Appl. Phys. Lett. **84**, 368 (2004).

[45] J. G. Fiorenza, G. Braithwaite, C. W. Leitz, M. T. Currie, J. Yap, F. Singaporewala, V. K. Yang, T. A. Langdo, J. Carlin, M. Somerville, A. Lochtefeld, H. Badawi, and M. T. Bulsara, Semicond. Sci. Technol. **19**, L4 (2004).

[46] M. G. Howes and P. S. Dobson, Phys. Stat. Sol. (a) **6**, 611 (1971).

[47] E. M. Juleff, Solid State Electron. **16**, 1173 (1973).

[48] A. Antonelli, J. F. Justo, and A. Fazzio, J. Phys.: Condens. Matter **14**, 12761 (2002).

[49] D. J. Larson, K. Thompson, R. L. Alvis, D. F. Lawrence, R. M. Ulfig, D. A. Reinhard, P. H. Clifton, J. H. Bunton, D. R. Lenz, and T. F. Kelly, Microscopy and Microanalysis **14**, 324 (2008).

[50] Y. Bychkov and B. Rashba, J. Phys. C: Solid State Phys. **17**, 6039 (1984).

[51] H. Malissa, W. Jantsch, M. Mühlberger, F. Schäffler, Z. Wilamowski, M. Draxler, and P. Bauer, Appl. Phys. Lett. **85**, 1739 (2004).

[52] L. A. Blyumenfel'd and V. A. Benderskii, Journal of Structural Chemistry **4**, 370 (1964).

[53] D. Monroe, Y. H. Xie, E. A. Fitzgerald, P.J. Silverman, and G. P. Watson, J. Vac. Sci. Technol. B **11**, 1731 (1993).

[54] I.-H. Tan, G. L. Snider, L. D. Chang, and E. L. Hu, J. Appl. Phys. **68**, 4071 (1990). See also www.nd.edu/∼gsnider.

[55] K. H. Chung, "Chemical vapor deposition (CVD) using novel precursor neopentasilane (NPS)", Ph.D. thesis, Princeton University (2009).

[56] K. H. Chung, N. Yao, J. Benziger, J. C. Sturm, K. K. Singh, D. Carlson, and S. Kuppurao, Appl. Phys. Lett. **92**, 113506 (2008).

[57] R. B. Dunford, N. Griffin, D. J. Paul, M. Pepper, D. J. Robbins, A. C. Churchill, and W. Y. Leong, Thin Solid Films **369**, 316 (2000).

[58] T. Berer, D. Pachinger, G. Pillwein, M. Mühlberger, H. Lichtenberger, G. Brunthaler, and F. Schäffler, Appl. Phys. Lett. **88**, 162112 (2006).

[59] L. J. Klein, D. E. Savage, and M. A. Eriksson, Appl. Phys. Lett. **90**, 033103 (2007).

[60] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).

[61] K. Lai, P. D. Ye, W. Pan, D. C. Tsui, S. A. Lyon, M. Mühlberger, and F. Schäffler, Appl. Phys. Lett **87**, 142103 (2005).

[62] E. Bersch, S. Rangan, R. A. Bartynski, E. Garfunkel, and E. Vescovo, Phys. Rev. B **78**, 085114 (2008).

[63] J. Faist, F. Capasso, D. L. Sivco, C. Sirtori, A. L. Hutchinson, and A. Y. Cho, Science **264**, 553 (1994).

[64] G. Dehlinger, L. L. Diehl, U. Gennser, H. Sigg, J. Faist, K. Ensslin, D. Grützmacher, and E. Müller, Science **290**, 2277 (2000).

[65] A. Kurobe, I. M. Castleton, E. H. Linfield, M. P. Grimshaw, K. M. Brown, D. A. Ritchie, M. Pepper, and G. A. C. Jones, Phys. Rev. B **50**, 4889 (1994).

[66] S. Q. Murphy, J. P. Eisenstein, G. S. Boebinger, L. N. Pfeiffer, and K. W. West, Phys. Rev. Lett. **72**, 728 (1994).

[67] I. B. Spielman, J. P. Eisenstein, L. N. Pfeiffer, and K. W. West, Phys. Rev. Lett. **84**, 5808 (2000).

[68] I. B. Spielman, J. P. Eisenstein, L. N. Pfeiffer, and K. W. West, Phys. Rev. Lett. **87**, 036803 (2001).

[69] M. Kellogg, J. P. Eisenstein, L. N. Pfeiffer, and K. W. West, Phys. Rev. Lett. **93**, 036801 (2004).

[70] E. Tutuc, M. Shayegan, and D. Huse, Phys. Rev. Lett. **93**, 036802 (2004).

[71] G. Burkard, D. Loss, and D. P. DiVincenzo, Phys. Rev. B **59**, 2070 (1999).

[72] X. Hu and S. Das Sarma, Phys. Rev. A **61**, 062301 (2000).

[73] Nakul Shaji, C. B. Simmons, M. Thalakulam, L. J. Klein, H. Qin, H. Luo, D. E. Savage1, M. G. Lagally, A. J. Rimberg, R. Joynt, M. Friesen, R. H. Blic, S. N. Coppersmith, and M. A. Eriksson, Nature Physics **4**, 540 (2008).

[74] L. P. Rokhinson and J. C. Sturm, "Si/SiGe epitaxy for digital control of exchange interactions in a spin-based quantum computer", oral presentation,

ARO/NSA/IARPA Quantum Computing & Quantum Algorithms Program Review, Buckhead, USA (2008).

[75] S. T. Stoddart, P. C. Main, M. J. Gompertz, A. Nogaret, L. Eaves, M. Henini, and S. P. Beaumont, Physica B **256-258**, 413 (1998).

[76] A. Palevski, F. Beltram, F. Capasso, L. Pfeiffer, and K. W. West, Phys. Rev. Lett. **65**, 1929 (1990).

[77] Y. Ohno, M. Tsuchiya, and H. Sakaki, Appl. Phys. Lett. **62**, 1952 (1993).

[78] G. S. Boebinger, A. Passner, L. N. Pfeiffer, and K. W. West, Phys. Rev. B **43**, 12673 (1991).

[79] R. Fletcher, M. Tsaousidou, T. Smith, P. T. Coleridge, Z. R. Wasilewski, and Y. Feng, Phys. Rev. B **71**, 155310 (2005).

[80] N. C. Mamani, G. M. Gusev, T. E. Lamas, A. K. Bakarov, and O. E. Raichev, Phys. Rev. B **77**, 205327 (2008).

[81] S. Wiedmann, G. M. Gusev, O. E. Raichev, T. E. Lamas, A. K. Bakarov, and J. C. Portal, Phys. Rev. B **78**, 121301(R) (2008).

[82] A. R. Powell, S. S. lyer, and F. K. LeGoues, Appl. Phys. Lett. **64**, 1856 (1994).

[83] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, J. Vac. Sci. Technol. B **14**, 4129 (1996).

[84] M. Hatzakis, J. Electrochem. Soc. **116**, 1033 (1969).

[85] Mark A. McCord, Michael J. Rooks, in SPIE Handbook of Microlithography, Micromachining and Microfabrication, Volume 1, edited by P. Rai-Choudhury, 141 (1997).

[86] J. R. Vig, J. Vac. Sci. Technol. A **3**, 1027 (1985).

[87] G. Binnig, H. Rohrer, Ch. Gerber, and E. Weibel, Appl. Phys. Lett. **40**, 178 (1982).

[88] G. Binnig, H. Rohrer, Ch. Gerber, and E. Weibel, Phys. Rev. Lett. **49**, 57 (1982).

[89] G. Binnig, C. F. Quate, and Ch. Geber, Phys. Rev. Lett. **56**, 930 (1986).

[90] E. S. Snow and P. M. Campbell, Appl. Phys. Lett. **64**, 1932 (1994).

[91] X.-Z. Bo, "Advanced silicon-based materials and devices using chemical vapor deposition", Ph.D. thesis, Princeton University (2004).

[92] X.-Z. Bo, L. P. Rokhinson, H. Yin, D. C. Tsui and J. C. Strum, Appl. Phys. Lett. **81**, 3263 (2002).

[93] T. K. Carns, M. O. Tanner, and K. L. Wang, J. Electrochem. Soc. **142**, 1260 (1995).

[94] K. Bierbaum, M. Grunze, A. A. Baski, L. F. Chi, W. Schrepp, and H. Fuchs, Langmuir **11**, 2143 (1995).

[95] X.-Z. Bo, L. P. Rokhinson, H. Yin, D. C. Tsui, and J. C. Sturm, in Mater. Res. Soc. Symp. Proc. **686**, edited by W. G. En, E. C. Jones, J. C. Sturm, M. J. Chan, S. Tiwari, and M. Hirose, A6.5 (2001).

[96] D. J. Paul, J. M. Ryan, P. V. Kelly, G. M. Crean, J. M. Fernández, M. Pepper, A. N. Broers, and B.A. Joyce, Solid-State Electron., **41**, 1509 (1997).

[97] J. A. Liddle, G. M. Gallatin and L. E. Ocola, Mater. Res. Soc. Symp. Proc. **739**, H1.5 (2003).

[98] B. Schwartz and H. Robbins, J. ElectroChem Soc. **108**, 365 (1961).

[99] U. Wieser, D. Iamundo, U. Kunze, T. Hackbarth, and U. König, Semicond. Sci. Technol. **15**, 862 (2000).

[100] G. S. Oehrlein and Y. Kurogi, Mater. Sci. Eng.: R. **24**, 153 (1998).

[101] D. L. Flamm and V. M. Donnelly, Plasma Chem. Plasma Process. **1**, 315 (1981).

[102] T. E. F. M. Standaert, M. Schaepkens, N. R. Rueger, P. G. M. Sebel, G. S. Oehrlein, and J. M. Cook, J. Vac. Sci. Technol. A **16**, 239 (1998).

[103] R. Ding, L. J. Klein, M. A. Eriksson, and A. E. Wendt, J. Vac. Sci. Technol. B **25**, 404 (2007).

[104] S. Agarwala, M. Tong, D. G. Ballegeer, K. Nummila, A. A. Ketterson, and I. Adesida, J. Electron. Mater. **22**, 375 (1993).

[105] N. G. Stoffel, J. Vac. Sci. Technol. B **10**, 651 (1992).

[106] M. Rahman, J. Appi. Phys. **82**, 2215 (1997).

[107] M. Rahman, N. P. Johnson, M. A. Foad, M. C. Holland, and C. D. W. Wilkinson, Appl. Phys. Lett. **61**, 2335 (1992).

[108] B. E. Deal, J. Electrochem. Soc. **121**, 198C (1974).

[109] L. P. Rokhinson, L. J. Guo, S. Y. Chou, and D. C. Tsui, Appl. Phys. Lett. **76**, 1591 (2000).

[110] X.-Z. Bo, L. P. Rokhinson, N. Yao, D. C. Tsui, and J. C. Sturm, J. Appl. Phys. **100**, 094317 (2006).

[111] M. K. Sanganeria, M. C. Öztürk, K. E. Violette, G. Harris, C. A. Lee, and D. M. Maher, Appl. Phys. Lett. **66**, 1255 (1995).

[112] K. Oda and Y. Kiyota, J. Electrochem. Soc. **143**, 2361 (1996).

[113] M. S. Carroll, J. C. Sturm, and M. Yang, J. Electrochem. Soc. **147**, 4652 (2000).

[114] K. H. Chung and J. C. Sturm, ECS Transactions, Volume 6, Issue 1, 401 (2007).

[115] Y. M. Haddara, B. T. Folmer, M. E. Law, and T. Buyuklimanli, Appl. Phys. Lett. **77**, 1976 (2000).

[116] N. R. Zangenberg, J. Fage-Pedersen, J. Lundsgaard Hansen, and A. Nylandsted Larsen, J. Appl. Phys. **94**, 3883 (2003).

[117] J. S. Christensen, H. H. Radamson, A. Yu. Kuznetsov, and B. G. Svensson, J. Appl. Phys. **94**, 6533 (2003).

[118] Y. Bogumilowicz, J. M. Hartmann, R. Truche, Y. Campidelli, G. Rolland, and T. Billon, Semicond. Sci. Technol. **20**, 127 (2005).

[119] D. K. Nayak, K. Kamjoo, J. S. Park, J. C. S. Woo, and K. L. Wang, Appl. Phys. Lett. **56**, 66 (1990).

[120] M. A. Reed, J. N. Randall, R. J. Aggarwal, R. J. Matyi, T. M. Moore, and A. E. Wetsel, Phys. Rev. Lett. **60**, 535 (1988).

[121] J. M. Elzerman, R. Hanson, L. H. Willems van Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven, Nature **430**, 431 (2004).

[122] D. Többen, D. A. Wharam, G. Abstreiter, J. P. Kotthaus, and F. Schäffler, Semicond. Sci. Technol. **10**, 711 (1995).

[123] U. Wieser, U. Kunze, K. Ismail, and J. O. Chu, Appl. Phys. Lett. **81**, 1726 (2002).

[124] L. J. Klein, K. A. Slinker, J. L. Truitt, S. Goswami, K. L. M. Lewis, S. N. Coppersmith, D. W. van der Weide, Mark Friesen, R. H. Blick, D. E. Savage, M. G. Lagally, Charlie Tahan, Robert Joynt, M. A. Eriksson, J. O. Chu, J. A. Ott, and P. M. Mooney, Appl. Phys. Lett. **84**, 4047 (2004).

[125] M. R. Sakra, H. W. Jiang, E. Yablonovitch, and E. T. Croke, Appl. Phys. Lett. **87**, 223104 (2005).

[126] K. A. Slinker, K. L. M. Lewis, C. C. Haselby, S. Goswami, L. J. Klein, J. O. Chu, S. N. Coppersmith, Robert Joynt, R. H. Blick, Mark Friesen, and M. A. Eriksson, New J. Phys. **7**, 246 (2005).

[127] B. J. van Wees, H. van Houten, C. W. J. Beenakker, J. G. Williamson, L. P. Kouwenhoven, D. van der Marel, and C. T. Foxon, Phys. Rev. Lett. **60**, 848 (1988).

[128] D. A. Wharam, T. J. Thornton, R. Newbury, M. Pepper, H. Ahmed, J. E. F. Frost, D. G. Hasko, D. C. Peacock, D. A. Ritchie, and G. A. C. Jones, J. Phys. C: Solid State Phys. **21**, L209 (1988).

[129] L. P. Kouwenhoven, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen, in Mesoscopic Electron Transport, edited by L. L. Sohn, L. P. Kouwenhoven, and G. Schön (Kluwer, Dordrecht 1997).

[130] L. J. Klein, K. L. M. Lewis, K. A. Slinker, Srijit Goswami, D. W. van der Weide, R. H. Blick, P. M. Mooney, J. O. Chu, S. N. Coppersmith, Mark Friesen, and M. A. Eriksson, J. Appl. Phys. **99**, 023509 (2006).

Appendix A

Sample RTCVD Growth Sequences

A.1 Introduction

Our Princeton RTCVD system is controlled using the AzeoTech DAQFactory software. Each hardware input/output interface is defined as a channel in the software, be it analog I/O (AI, AO), or digital I/O (DI, DO). The channels are monitored and controlled by sequences, which are basically a scripting programming language for data acquisition. The sequences can also use PID loops to automatically control the process variables based on different set-points (SP). This appendix provides the RTCVD growth sequences for two sample structures discussed in this thesis (modulation-doped Si/SiGe asymmetric double quantum wells and Si/SiGe regrowth on patterned devices). All growth start with an initialization routine sequence 0 and end with a shut-down routine sequence 7. Only the actual growth sequences 1 and 6 are given.

A.2 Growth Sequences #4822: Asymmetric Double Quantum Well

intrinsic Si $\sim$ 4nm
intrinsic $Si_{0.7}Ge_{0.3}$ $\sim$ 12 nm
n-doped $Si_{0.7}Ge_{0.3}$ $\sim$ 4 nm, 5×10^{18} cm^{-3}
intrinsic $Si_{0.7}Ge_{0.3}$ $\sim$ 10 nm
intrinsic Si $\sim$ 7 nm
intrinsic $Si_{0.7}Ge_{0.3}$ $\sim$ 6 nm
intrinsic Si $\sim$ 8 nm
intrinsic $Si_{0.7}Ge_{0.3}$ $\sim$ 80 nm
relaxed SiGe buffers and substrate

for comments only

// Sequence_1

EndSeq SEQUENCE_0

// call for growth squence

SP2 = 0

BeginSeq Sequence_6

WaitFor SP2 > 0.5, 0.300

EndSeq Sequence_6

BeginSeq SEQUENCE_7

// Sequence_6

// cold transmission acquisition

STATUS_MESSAGE = "PRESS SOFT_GO for Cold Values"

WaitFor SOFT_GO > 0.5, 0.300

SP3 = 1

Wait 1

SP3 = 0

// raise pressure to max

AO00_MAIN = 1 — *H_2 flow = 5 slpm*

AO08_PRESS = 0 — *butterfly valve fully open*

// pre-flow process gases

STATUS_MESSAGE = "Pre-flow Process Gases"

AO06_DCS = 0.534 — *DCS flow = 26 sccm*

DO07_DCS_SEL = 1

AO02_GeH4 = 0.45 — *GeH_4 flow = 225 sccm*

DO03_GeH4_SEL = 1

AO05_PH3_LOW = 0.2 — *PH_3 flow = 2 sccm*

DO05_PH3_SEL = 1

// 900C clean

STATUS_MESSAGE = "Ramp Up Lamp"

SP4 = 0

RAMP_GOAL = 0.24 — *Lamp power = 24%*

RAMP_RATE = 0.1

BeginSeq RAMP_SP7

WaitFor SP1 > 0.5, 0.300

STATUS_MESSAGE = "Baking"

Var.wait_time = 300

Wait 300 — *5 minutes baking*

// pump down and ramp down

STATUS_MESSAGE = "Pump Down and Ramp Down Lamp"

AO00_MAIN = 0.618 — *H_2 flow = 3 slpm*

AO08_PRESS = 0.6 *main pressure = 6 Torr*

Wait 15

SP1 = 0

RAMP_GOAL = 0.16

RAMP_RATE = -0.2

BeginSeq RAMP_SP7 WaitFor SP1 > 0.5, 0.300

Wait 5

// grow SiGe

SP5 = 2.941 *set point for $T = 625\,^{\circ}C$*

SP4 = 1

STATUS_MESSAGE = "Press SOFT_GO for 625C Growth"

WaitFor SOFT_GO > 0.5, 0.300

STATUS_MESSAGE = "Growing SiGe buffer"

DO13_DCSandSi2H6_INJ = 1 *DCS inject on*

Wait 10

DO10_GeH4_INJ = 1 *GeH_4 inject on*

Var.wait_time = 400

Wait 400 *400 seconds SiGe growth*

DO10_GeH4_INJ = 0 *GeH_4 inject off*

Wait 15

// grow Si

SP5 = 4.294 *set point for $T = 750\,^{\circ}C$*

STATUS_MESSAGE = "Growing Si channel"

Var.wait_time = 50

Wait 50 *50 seconds Si growth*

// grow SiGe

SP5 = 2.941 *set point for $T = 625\,^{\circ}C$*

STATUS_MESSAGE = “Press SOFT_GO for 625C Growth”

WaitFor SOFT_GO > 0.5, 0.300

STATUS_MESSAGE = “Growing SiGe spacer”

DO10_GeH4_INJ = 1 *GeH_4 inject on*

Var.wait_time = 30

Wait 30 *30 seconds SiGe growth*

DO10_GeH4_INJ = 0 *GeH_4 inject off*

Wait 10

// grow Si

SP5 = 4.294 *set point for $T = 750\,^\circ C$*

STATUS_MESSAGE = “Growing Si channel”

Var.wait_time = 40

Wait 40 *40 seconds Si growth*

// grow SiGe

SP5 = 2.941 *set point for $T = 625\,^\circ C$*

STATUS_MESSAGE = “Press SOFT_GO for 625C Growth”

WaitFor SOFT_GO > 0.5, 0.300

STATUS_MESSAGE = “Growing SiGe spacer”

DO10_GeH4_INJ = 1 *GeH_4 inject on*

Var.wait_time = 50

Wait 50 *50 seconds SiGe growth*

STATUS_MESSAGE = “Growing n+SiGe supply”

DO12_PH3_INJ = 1 *PH_3 inject on*

Var.wait_time = 20

Wait 20 *20 seconds n-doping*

DO12_PH3_INJ = 0 *PH_3 inject off*

STATUS_MESSAGE = “Growing i-SiGe cap”

Var.wait_time = 60

Wait 60 *60 seconds SiGe growth*

DO10_GeH4_INJ = 0 *GeH_4 inject off*

Wait 15

// grow Si

SP5 = 4.294 *set point for $T = 750\,^{\circ}C$*

STATUS_MESSAGE = "Growing Si cap"

Var.wait_time = 20

Wait 20 *20 seconds Si growth*

// close process gases

STATUS_MESSAGE = "Shutting Down Growth Squence"

DO13_DCSandSi2H6_INJ = 0 *DCS inject off*

SP4 = 0

// ramp down

STATUS_MESSAGE = "Ramp Down Lamp"

SP1 = 0

RAMP_GOAL[0] = 0.0

RAMP_RATE[0] = -0.3

BeginSeq RAMP_SP7 WaitFor SP1 > 0.5, 0.300

DO05_PH3_SEL = 0

DO03_GeH4_SEL = 0

STATUS_MESSAGE = "Done with Growth Squence"

SP2 = 1 *return to SEQUENCE_1*

A.3 Growth Sequences #4827: Epitaxial regrowth on #4811-Quantum Dot

intrinsic Si $\sim$ 4 nm
intrinsic $Si_{0.7}Ge_{0.3}$ $\sim$ 60 nm
#4811 Quantum Dot Patterns
relaxed SiGe buffers and substrate

for comments only

// Sequence_1

EndSeq SEQUENCE_0

// call for growth squence

SP2 = 0

BeginSeq Sequence_6

WaitFor SP2 > 0.5, 0.300

EndSeq Sequence_6

BeginSeq SEQUENCE_7

// Sequence_6

// cold transmission acquisition

STATUS_MESSAGE = "PRESS SOFT_GO for Cold Values"

WaitFor SOFT_GO > 0.5, 0.300

SP3 = 1

Wait 1

SP3 = 0

// raise pressure to max

AO00_MAIN = 1 *H_2 flow = 5 slpm*

AO08_PRESS = 0 *butterfly valve fully open*

// pre-flow process gases

STATUS_MESSAGE = "Pre-flow Process Gases"

AO06_DCS = 0.534 *DCS flow = 26 sccm*

DO07_DCS_SEL = 1

AO02_GeH4 = 0.45 *GeH_4 flow = 225 sccm*

DO03_GeH4_SEL = 1

// 800C clean

STATUS_MESSAGE = "Ramp Up Lamp"

SP4 = 0

RAMP_GOAL = 0.23 *Lamp power = 23%*

RAMP_RATE = 0.1

BeginSeq RAMP_SP7

WaitFor SP1 > 0.5, 0.300

STATUS_MESSAGE = "Baking"

Var.wait_time = 120

Wait 120 *2 minutes baking*

// pump down and ramp down

STATUS_MESSAGE = "Pump Down and Ramp Down Lamp"

AO00_MAIN = 0.618 *H_2 flow = 3 slpm*

AO08_PRESS = 0.6 *main pressure = 6 Torr*

Wait 15

SP1 = 0

RAMP_GOAL = 0.16

RAMP_RATE = -0.2

BeginSeq RAMP_SP7 WaitFor SP1 > 0.5, 0.300

Wait 5

// grow SiGe

SP5 = 2.941 *set point for $T = 625\,^{\circ}C$*

SP4 = 1

STATUS_MESSAGE = “Press SOFT_GO for 625C Growth”

WaitFor SOFT_GO > 0.5, 0.300

STATUS_MESSAGE = “Growing SiGe cap”

DO13_DCSandSi2H6_INJ = 1 *DCS inject on*

Wait 10

DO10_GeH4_INJ = 1 *GeH_4 inject on*

Var.wait_time = 300

Wait 300 *5 minutes SiGe growth*

DO10_GeH4_INJ = 0 *GeH_4 inject off*

Wait 15

// grow Si

SP5 = 3.554 *set point for $T = 700\,^{\circ}C$*

STATUS_MESSAGE = “Growing Si cap”

Var.wait_time = 90

Wait 90 *90 seconds Si growth*

// close process gases

STATUS_MESSAGE = “Shutting Down Growth Squence”

DO13_DCSandSi2H6_INJ = 0 *DCS inject off*

SP4 = 0

// ramp down

STATUS_MESSAGE = “Ramp Down Lamp”

SP1 = 0

RAMP_GOAL[0] = 0.0

RAMP_RATE[0] = -0.3

BeginSeq RAMP_SP7 WaitFor SP1 > 0.5, 0.300

DO03_GeH4_SEL = 0

STATUS_MESSAGE = “Done with Growth Squence”

SP2 = 1 *return to SEQUENCE_1*

Appendix B

Sample Structures Numerically Solved by 1D Poisson Program

B.1 Introduction

In this appendix we provide input files for two sample structures that were numerically solved by the 1D Poisson Program: the top-gated modulation-doped Si/SiGe heterostructure (solve for Poisson's equation only) and the symmetric double quantum well (solve Poisson and Schrödinger equations self-consistently). The FreeWare program we used is PC version beta 8c. The following three new materials must be added to the original materials datafile before the sample input files can run (all band offset parameters are relative to the $Si_{0.7}Ge_{0.3}$ bulk):

	SiGe	s-Si	Al2O3
	$Si_{0.7}Ge_{0.3}$ bulk	strained Si	Al_2O_3
Energy gap (eV)	1.04	0.92	7.00
Conduction band offset (eV)	0	-0.18	2.50
Relative dielectric constant	13.13	11.7	9.0
Electron effective mass (m_0)	0.328	0.19	1
Conduction band degeneracy	6	2	6
Heavy hole effective mass (m_0)	0.49	0.49	1
Light hole effective mass (m_0)	0.16	0.16	1
Donor level (eV)	0.003	0.003	0.003
Acceptor level (eV)	0.01	0.01	0.005

B.2 Top-gated Modulation-doped Si/SiGe heterostructure Input File

Al_2O_3 = 90 nm
Si = 5 nm, background 10^{17} cm^{-3}
$Si_{0.7}Ge_{0.3}$ = 15 nm, background 10^{17} cm^{-3}
n-doped $Si_{0.7}Ge_{0.3}$ = 2 nm, 5×10^{18} cm^{-3}
$Si_{0.7}Ge_{0.3}$ = 15 nm, background 10^{17} cm^{-3}
Si = 10 nm, background 10^{17} cm^{-3}
$Si_{0.7}Ge_{0.3}$ = 100 nm, background 10^{17} cm^{-3}
intrinsic $Si_{0.7}Ge_{0.3}$ = 1μm
substrate

surface schottky=0 v1

Al2O3 t=900 no electrons dy=1

s-Si t=50 Nd=1e17 dy=1

SiGe t=150 Nd=1e17 dy=1

SiGe t=20 Nd=5e18 dy=1

SiGe t=150 Nd=1e17 dy=1

s-Si t=100 Nd=1e17 dy=1

SiGe t=1000 Nd=1e17 dy=1

SiGe t=1um dy=10

substrate

fullyionized

v1 0.25 -2.25 -.25

temp=0.1K

B.3 Symmetric Si/SiGe Double Quantum Well Input File

$Si_{0.7}Ge_{0.3}$ = 27 nm
Si = 8 nm
$Si_{0.7}Ge_{0.3}$ = 4 nm
Si = 8 nm
$Si_{0.7}Ge_{0.3}$ = 27 nm
substrate

surface schottky=0 v1

SiGe t=150

SiGe t=20

SiGe t=100

s-Si t=80

SiGe t=40

s-Si t=80

SiGe t=100

SiGe t=20

SiGe t=150

substrate

fullyionized

v1 -1 0.2 0.1

dy=10

schrodingerstart=20

schrodingerstop=720

find quantized states

temp=4K

Appendix C

Publications and Presentations Resulting From This Thesis

C.1 Journal Articles and Conference Papers

1. K. Yao, M. Gaevski, J. C. Sturm, A. Chernyshov, L. P. Rokhinson, C. Mike, J-S. Park, J. G. Fiorenza, and A. Lochtefeld, "Effect of leakage in relaxed SiGe buffer layers on Si/SiGe quantum devices", manuscript in preparation.

2. K. Yao, J. C. Sturm, and A. Lochtefeld, "Strained silicon two-dimensional electron gases on commercially available $Si_{1-x}Ge_x$ relaxed graded buffers", in SiGe and Ge: Materials, Processing, and Devices, ECS Transactions, Volume 3, Issue 7, pp. 313-315 (2006).

3. K. Yao and J. C Sturm, "Nanopatterning of Si/SiGe two-dimensional hole gases by PFOTS-aided AFM lithography of carrier supply layer", in Nanomanufacturing, Mater. Res. Soc. Symp. Proc. **921E**, 0921-T02-08 (2006).

C.2 Conference Presentations

4. K. Yao, M. Gaevski, J. C. Sturm, A. Chernyshov, L. P. Rokhinson, C. Mike, J-S. Park, J. G. Fiorenza, and A. Lochtefeld, "Effect of substrate doping in relaxed SiGe buffers on strained Si 2DEG quantum devices", American Physical Society March Meeting, Pittsburgh, USA (2009).

5. K. Yao, M. Gaevski, A. Chernyshov, L. P. Rokhinson, and J. C. Sturm, "Si/SiGe epitaxy for digital control of exchange interactions in a spin-based quantum computer", ARO/NSA/IARPA Quantum Computing & Quantum Algorithms Program Review, Buckhead, USA (2008).

6. K. Yao, M. Gaevski, A. Chernyshov, L. P. Rokhinson, and J. C. Sturm, "Epitaxially passivated strained silicon quantum dots", ARO/NSA/IARPA Quantum Computing & Quantum Algorithms Program Review, Minneapolis, USA (2007).

7. K. Yao, J. C. Sturm, and A. Lochtefeld, "Strained silicon two-dimensional electron gases on commercially available $Si_{1-x}Ge_x$ relaxed graded buffers", 210th Meeting of The Electrochemical Society (2nd International SiGe & Ge: Materials, Processing, and Device Symposium), Cancun, Mexico (2006).

8. K. Yao, L. P. Rokhinson, and J. C. Sturm, "Digital control of exchange interaction in a spin-based silicon quantum computer, – strained silicon two-dimensional electron gases and clean epitaxial regrowth", Quantum Computing & Quantum Algorithms Program Review, Buckhead, USA (2006).

9. K. Yao and J. C Sturm, "Nanopatterning of Si/SiGe two-dimensional hole gases by PFOTS-aided AFM lithography of carrier supply layer", Materials Research Society Spring Meeting, San Francisco, USA (2006).

C.3 NASA New Technology Report

10. E. M. Dons, G. S. Tompa, J. C. Sturm, and K. Yao, "Silicon germanium alloy photovoltaics for 1.06 Micron wireless power transmission", submitted and approved by NASA in 2006.