# Amorphous silicon TFT based non-volatile memory

Memory devices based on amorphous Silicon (a-Si) thin film transistors (TFTs) have the potential to greatly expand the functionality of a-Si TFT circuitry. If designed to be compatible with the existing TFT fabrication process, they could provide a low-cost and efficient way to integrate memory capabilities into large area electronics. In this chapter, a brief overview of the various different non-volatile memory technologies is presented. Then, the structure and principle of operation of the a-Si TFT based floating gate non-volatile memory is described. The shortcomings of the a-Si floating gate TFT are analyzed and discussed. Finally, a new non-volatile memory TFT structure that overcomes the limitations associated the floating gate device is presented. The work presented in this chapter was described in references [1] through [4].

## 5.1. Overview of non-volatile memory technology

All information processing can be broken down into three sequential steps of data acquisition, computation/analysis and action. As such, memory is an indispensable part of any information processing system, for the data must be stored so that appropriate computation can be performed and the results must be recorded so that the desired action can be completed. Because of this, memory has become ubiquitous in our daily lives, inside of computers, mobile phones, USB drives, mp3 players, etc. These memories come in two different flavors – volatile and non-volatile. Volatile memory requires constant power input to retain the stored data, the data is lost as soon as the energy source is removed. Non-volatile memory, on the other hand, retains the data without any input power, and typically retains data over much longer periods of time than its volatile counterpart. We will focus our discussion on the non-volatile memories.

At the core of any non-volatile memory, there is an element that can be changed between different physical states by the application of an external stimulus. The state of the element represents the stored information. This information is accessed, by “reading” the state, with the

application of a different external stimulus. There are four main metrics by which a memory element is characterized:

Write/erase time: the time it takes the element to change between states under the influence of external stimulus

Read time: the time it takes to determine the state of the element.

Retention: the amount of time the element can hold its current state without significant changes.

Endurance: the number of cycles of write/erase the element can withstand without significant degradation to its other characteristics.

Modern non-volatile memory can be segmented into four main categories based on mechanisms by which the bi-stable states are established: charge trapping memory, ferroelectric memory, phase change memory, and magneto-resistive memory. Note that older forms of non-volatile memory, such as magnetic disk drives and optical disks are excluded from discussion for the sake of brevity.

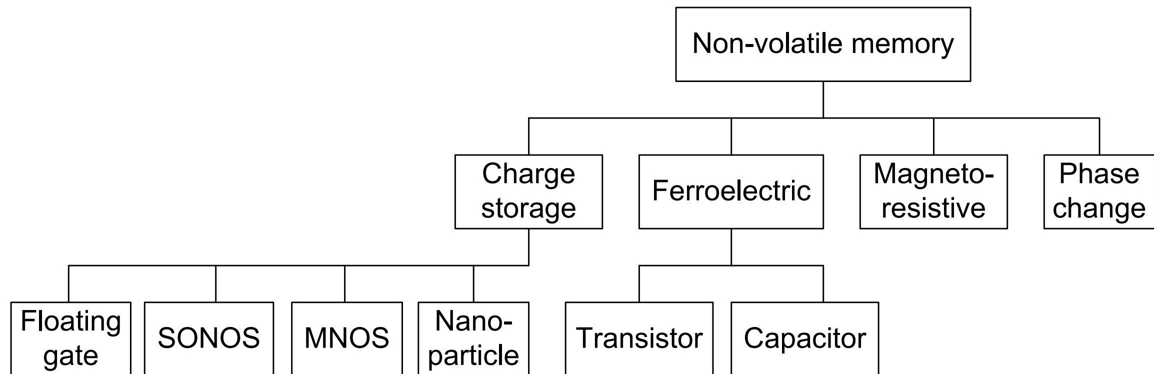


**Figure 5.1. Non-volatile memory technologies.**

### 5.1.1. Charge trapping memory

Charge trapping memories are the dominant form of non-volatile memory on the market today. They are almost entirely based MOS transistor technology. As such, they are compatible with many pre-existing VLSI fabrication process and they owe much of their success to this fact. This class of memory uses charge trapping in the gate dielectric of the MOS transistor to change

the threshold voltage of the transistor, which represents the memory state of the device. There are various different implementations, each with its own advantages and disadvantages.

Proposed by Khang and Sze in 1967, the floating gate transistor is the first implementation of a charge-trapping memory based on the MOS transistor [5]. It is also the most prevalent form in today's products. As can be seen in Figure 5.2a, its structure is very similar to that of a conventional MOS transistor, except for the floating gate that is inserted into the gate dielectric between the channel and the standard poly-Si control gate. The floating gate is typically made of heavily doped poly-Si and is sandwiched between the gate $SiO_2$ (tunnel oxide) layer and the interpoly dielectric (IPD) $SiO_2$ (blocking oxide) layer. The floating gate is electrically insulated by $SiO_2$ layers that surround it, and as such any excess charge that is injected onto the floating gate is trapped there. The trapped charge alters the potential distribution in the gate stack, and therefore the threshold voltage of the transistor, which is the memory state of the device.

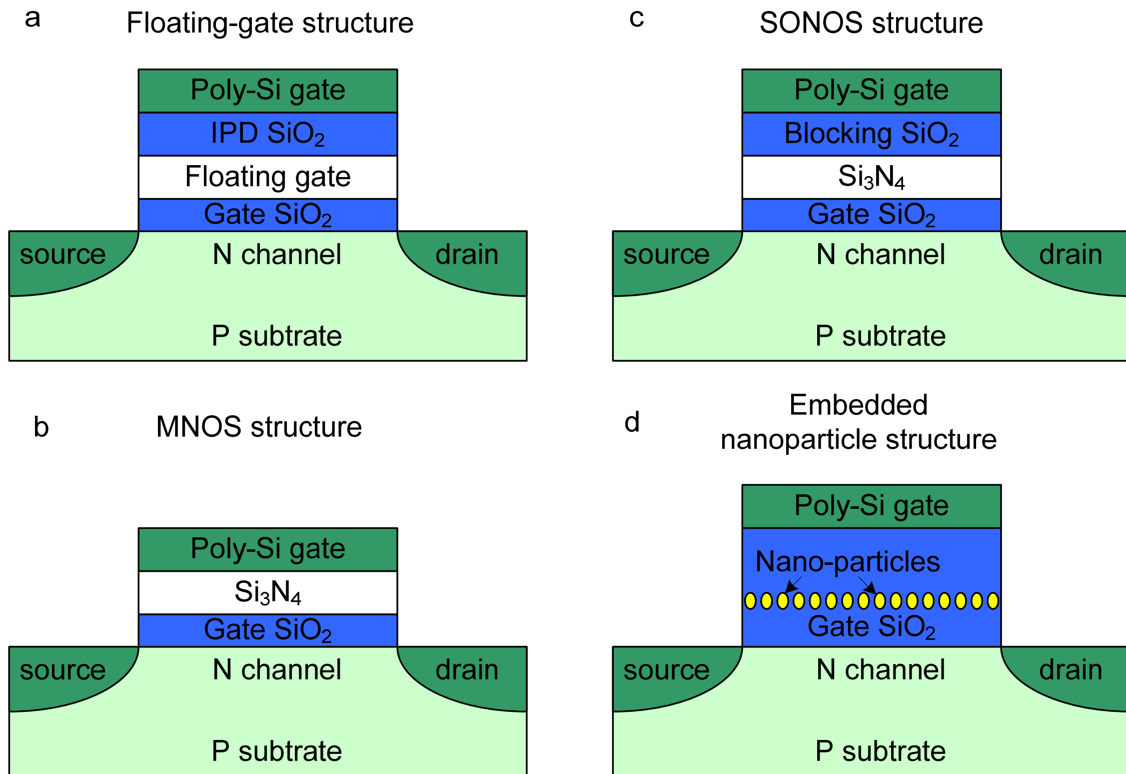


**Figure 5.2. Structures of the charge-trapping based nonvolatile memory transistors.**

Another implementation of the memory transistor is metal-nitride-oxide-silicon (MNOS) transistor, which was also first demonstrated in 1967 by Wenger et al [6][7][8]. This device, shown in Figure 5.2b, does not use the floating gate to trap charge, instead the charge is injected and stored in the defects of the $Si_3N_4$ film, which is sandwiched between gate $SiO_2$ and the poly-Si control gate. Note that the name of the structure calls for metal gates, but in more modern implementations poly-Si is often used, which is reflected in the illustration. It was quickly discovered that the MNOS structure was prone to charge loss through leakage from the $Si_3N_4$ to the gate, so a modified structure called the silicon-oxide-nitride-silicon (SONOS) transistor was developed [9]. This structure, illustrated in Figure 5.2c, differs from the MNOS structure by having an additional $SiO_2$ layer between the $Si_3N_4$ charge storage layer and the poly-Si gate. The purpose of this layer is to block the charge in the $Si_3N_4$ from leaking into the gate and prevent the memory state loss resulting from this leakage. Often this $SiO_2$ layer is referred to as the blocking oxide, while the gate $SiO_2$ is referred to as the tunnel oxide.

As dimension of the memory devices was scaled down in an effort to improve density and reduce cost, problems that were previously insignificant started to plague the floating gate memory. As the device length was reduced, the drain-to-floating-gate capacitive coupling began to have a pronounced effect on the device characteristics [10][11]. This made it increasingly difficult to accurately read the memory state of the device. Additionally, as the dielectric thickness was reduced, the $SiO_2$ became more prone to defects that created leakage pathways. Since the floating gate is conductive, if there were a leakage path in the $SiO_2$ that allowed charges to escape, all of the charge on the floating gate would be lost along with the memory state [11]. To remedy these potential problems, a new structure based on nano-particles was developed [12]. This structure, illustrated in Figure 5.2d, had a layer of nano-particles which was embedded within the gate dielectric $SiO_2$. These nano-particles were typically a few nm in diameter, and were electrically insulated from each other. In effect, they acted as discrete floating gates that store charges separately. Because of the discreteness of these particles, the device was not prone to failure due to a single leakage path and the drain coupling effect is significantly reduced. It must

be noted here that the implementations based on $Si_3N_4$ as the charge trapping medium offered similar benefits as the nano-particles devices, because the charge-trapping $Si_3N_4$ is an insulator film and the charge-trapping defects were also discrete in nature.

*Write (program) mechanisms*

In all the different implementations of the charge-trapping non-volatile memories, charge must be injected into the charge trapping media (floating gate, $Si_3N_4$ and nano-particles) in order to change the memory state of the device. This process is called writing or programming, these two terms will be used interchangeably throughout the rest of the discussion. Two major mechanisms have been shown to be viable programming methods: Fowler-Norhdheim (FN) tunneling [13] and hot carrier injection (HCI) [14].

As shown in Figure 5.3, FN tunneling method of programming works based on carriers tunneling, through the thin tunnel oxide, from the substrate to the charge-trapping medium (floating gate, $Si_3N_4$ and nano-particles), under applied electric field. Because of the smaller effective mass and the lower barrier height, electron tunneling is much more efficient than hole tunneling. This is why the majority of charge trapping non-volatile memory is based on electron trapping in n-type transistors. From this point forward, all discussions and illustrations will be referring to non-volatile memory based on electron trapping in n-type transistors, unless otherwise noted.

In practice, FN programming is achieved by grounding the source, drain and body electrodes and applying a large positive voltage pulse to the control gate electrode. As such, the vertical electric field is uniform throughout the length of the device and the injection of electrons is uniform (Figure 5.3b). The tunneling probability or rate of electron injection into the floating gate determines the speed at which the device can be programmed, or the program time. This rate is a function of the distribution of occupied states in the gate, the distribution of unoccupied states in the charge-trapping medium, the thickness of the oxide ($t_{ox}$), the potential barrier height ($\varphi_B$), and the applied electric field (which determines the shape of the oxide potential barrier). Using the WKB approximation, the tunneling rate can be analytically expressed as [15]:

$$J_{FN} = \alpha E_{pro}^{2} e^{\left(-\frac{\beta}{E_{pro}}\right)} \qquad (5.1)$$

Where $\alpha = \frac{q^3}{8\pi h \phi_B} \frac{m_0}{m^*}$, $\beta = 4\sqrt{2m^*} \frac{\phi_B^{3/2}}{3\hbar q}$ and $E_{pro} = \frac{V_{tox} - V_{FB}}{t_{ox}}$. $V_{tox}$ is the portion of the applied programming voltage across the tunnel oxide and $V_{FB}$ is the flatband voltage.

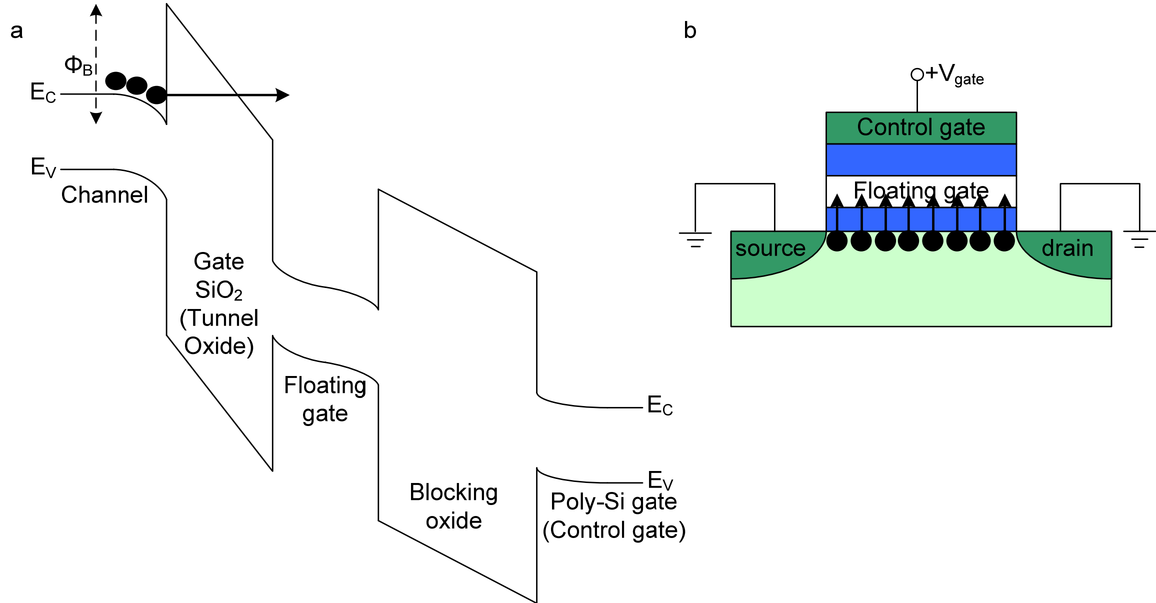


**Figure 5.3. a) Band diagram of a charge-trapping nonvolatile memory device during programming using Fowler-Norhdheim tunneling. b) Uniform electron injection across the entire length of the gate. (Floating gate implementation shown, but applicable to all other implementations as well).**

One of the main benefits of FN tunnel programming is its low power consumption. The gate tunnel currents involved are very low, and there is no source-to-drain current because the source and drain electrodes are both grounded. Therefore, this method is quite attractive for low power applications. However, the low tunneling current also means that the programming takes a relatively long time (~ms) [18]. The exponential dependence of the tunnel current on the programming field creates significant constraints on device-to-device uniformity. A small variation in tunnel oxide thickness can result in a large variance in the programming tunnel current and therefore a big spread the resulting threshold voltages. As a result, thickness of the tunnel oxide is an important parameter to be designed and controlled. There is a fundamental trade-off

between thinner oxides, which provide lower voltage programming and shorter programming time, and thicker oxide, which provides better uniformity and reliability.

HCI programming can be used to overcome some of the difficulties associated with FN programming. As shown in Figure 5.4, HCI works based on “hot” (higher energy) carrier overcoming the energy barrier between the silicon channel and the tunnel oxide, and drifting into the charge trapping medium under the applied gate electric field. For reasons similar to the case of FN tunneling, hot electron injection is much more efficient than hot hole injection. As a result, most charge-trapping based non-volatiles devices use hot electron injection in n-type transistors.

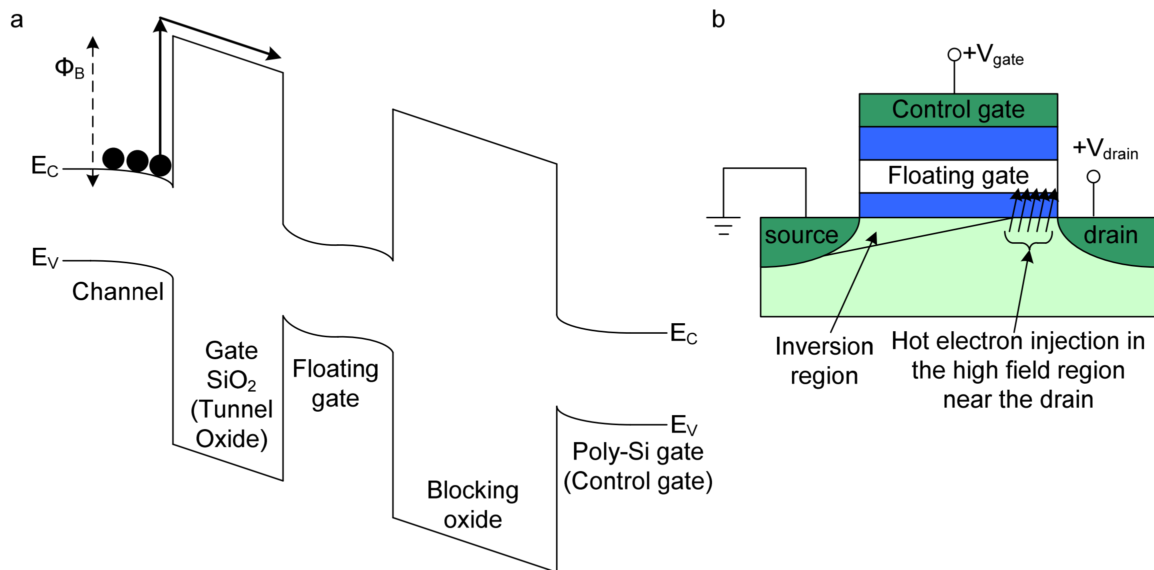


**Figure 5.4. a) Band diagram (near the drain region) of a charge-trapping nonvolatile memory device during programming using channel hot electron injection. b) Selective injection near the drain terminal of the device (floating gate implementation shown, but applicable to all other implementations).**

In practice, hot electrons injection programming is done by applying large positive voltage pulses to the gate and drain electrodes while grounding the source and body electrodes. The source-drain electric field imparts kinetic energy to the electrons in the channel, and electrons attain their highest energy in the high field region near the drain terminal of the device. Some of the electrons gain enough kinetic energy to overcome the potential barrier to get into the

conduction band of the tunnel oxide, where they are swept into the charge trapping medium by the applied gate field. Electron injection happens locally near the drain terminal of the device because of the high energy required to surmount the potential barrier (Figure 5.4(b)). To first order, the magnitude of the drain voltage determines the rate of injection or the programming time and the magnitude of the gate voltage determines amount of the charge injected or the threshold voltage shift. This process may be described using the "lucky electron" model first introduced by Shockley [16], which says the probability of injection is the lumped probability of three statistically independent events:

1. The electron gains sufficient amount of energy to surmount the potential barrier
2. Sufficient amount of the momentum of the "hot" electron is redirected, via collision, towards the Si/SiO2 interface
3. The hot electron does not suffer additional collision that prevent it from surmounting the barrier and drifting to the charge trapping medium

Using this model, the injection gate current maybe expressed as the following [16]

$$I_{HCI} = I_{DS} \int_{0}^{L_{eff}} \frac{P_1 P_2 P_3}{\lambda_r} dx \qquad (5.2)$$

Where $I_{DS}$ = drain-source current, $L_{eff}$ = effective channel length of the transistor, $\lambda_r$ = momentum-redirecting scattering mean free path, $P_1$, $P_2$ and $P_3$ are probabilities associated with the above events 1, 2 and 3, respectively.

HCI is less dependent on the applied gate voltage pulse than FN tunneling. As a result, it is less sensitive to variations in the tunnel oxide thickness and there is less spread in the threshold voltage of the programmed state. HCI is also a significantly faster programming method (~ μs) than FN tunneling due to the nature of its injection mechanism [18]. However, it also consumes a lot more power because of large amount of drain-source current that is associated with programming. Furthermore, because the charge injection is concentrated in region near the drain terminal, HCI puts more stress on the tunnel oxide. Consequently, the tunnel oxide tends to degrade faster creating defects that leads device failure [17]. This is especially problematic for

floating-gate type devices, where all the trapped charge may be lost through a single defect due to the high conductivity of the floating gate.

The non-uniform charge injection of HCI can be exploited to improve memory density. Specifically, in the MNOS, SONOS, nano-particle type devices, two bits can be stored within a single device [19]. Due to the discrete nature of the charge traps in these devices structures, the charge injected via HCI stays localized near the drain end of the device. As such, if the programming process were repeated with the source and drain terminals interchanged, the injection would occur near the new drain (previously the source) terminal. Note that since HCI also requires a drain-to-source bias, programming of individual cells can be achieved with simpler circuits than that of the FN method.

*Read mechanism*

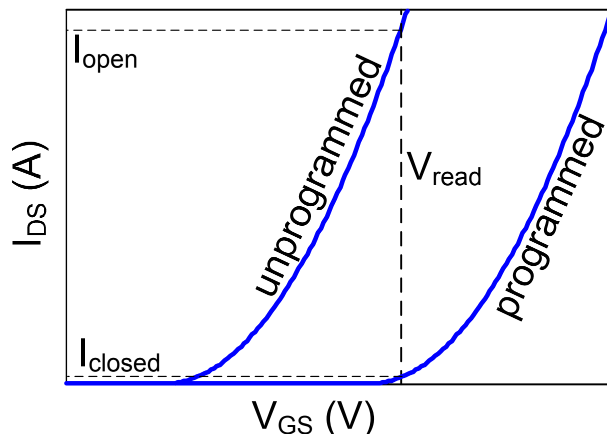


**Figure 5.5. $I_{DS}$ vs $V_{GS}$ of a programmed and an un-programmed non-volatile memory transistor. Note that $V_{GS}$ refers the voltage applied to the control gate. $V_{read}$ is the voltage applied to the control gate during reading, $I_{close}$ and $I_{open}$ are the drain-source currents corresponding to $V_{read}$ in a programmed and an un-programmed device, respectively.**

Reading of the bit (whether or not there is charge stored in the charge-trapping medium) is performed by checking if the transistor is “open” or “closed” when operating under gate and drain-source voltages much smaller than the programming voltages. Since the stored electrons in the charge-trapping medium causes a parallel shift in the device threshold, the same applied $V_{GS}$ will result to different drain-source current in a programmed vs an un-programmed device. This is

illustrated in Figure 5.5, when the same gate voltage $V_{read}$ is applied to a programmed and an un-programmed transistor, the un-programmed transistor yields $I_{open}$, which is much larger than that of the programmed transistor, $I_{close}$.

*Erase mechanism*

In order to return a programmed device back to its initial state, the trapped charge must be ejected from the gate stack. This process is called erasing, and there are three different mechanisms that may be used to erase a programmed device – UV radiation, FN tunneling, and HCI.

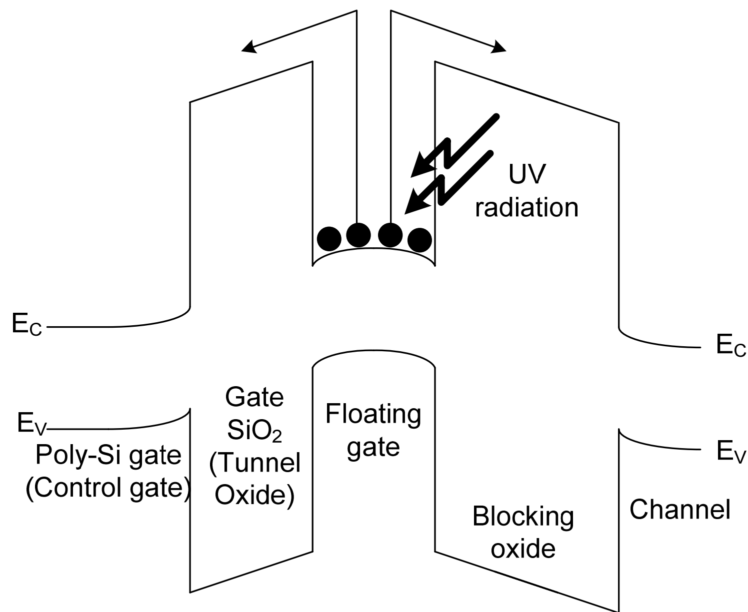


**Figure 5.6. Band diagram of a charge-trapping nonvolatile memory device during erase via UV radiation. (Floating gate implementation shown, but applicable to all other implementation as well).**

As shown in Figure 5.6, UV radiation imparts sufficiently large amounts of energy to electrons to surmount the energy barrier presented by the surrounding oxides. The field resulting from the trapped charge then sweeps the high energy electrons into either the control gate or the substrate. As trapped electrons escape, the threshold voltage is reduced towards its initial value. This process is rather slow and can take up to 10 minutes. In addition to the speed disadvantage, this method is also limited by the lack of selectivity. All devices must be erased at the same time,

and there is no way to erase one transistor while keep the threshold voltage of the neighboring transistors unaffected. Furthermore, the requirement of a UV light source makes this impractical outside of the laboratory setting.

FN tunneling mechanism can be used to erase the device in a manner similar to that used to program it, the only difference is the polarity of the applied control gate voltage. When a sufficiently large negative voltage is applied to the control gate, trapped electrons tunnel through the thin tunnel oxide into the channel in a process that is the inverse of when they tunneled in during programming (Figure 5.7). As the trapped electrons tunnel out, the threshold voltage is reduced towards its initial value. The erasing process is physically very similar to the programming process, and as such the advantages and disadvantages discussed for programming apply to erasing as well. This technique is significantly faster than UV radiation and offers the capability to erase devices individually in an active matrix circuit.

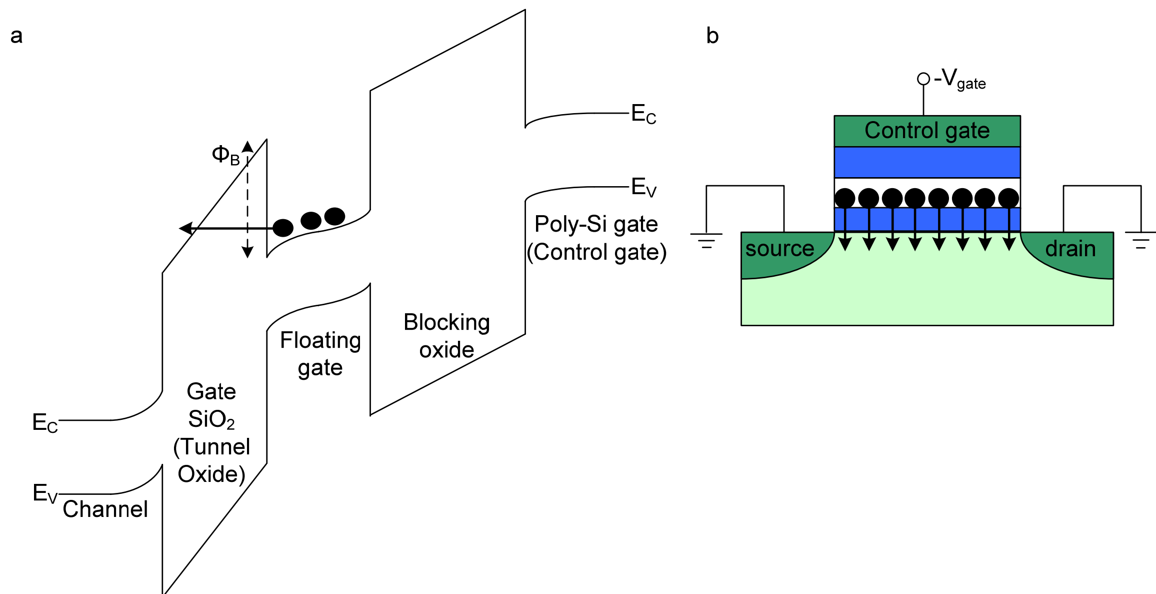


**Figure 5.7. a) Band diagram of a charge-trapping nonvolatile memory device during erasing using Fowler-Norhdheim tunneling. b) Uniform electron injection across the entire length of the gate. (Floating gate implementation shown, but applicable to all other implementations as well).**

As shown in Figure 5.8, HCI can also be used to erase the programmed device, by injecting hot holes into the charge-trapping medium. The injected holes neutralize the injected

electron and reduce the net charge in the gate stack. As the trapped electrons are neutralized, the threshold voltage is reduced towards its initial value. Hot holes are generated in the same way the hot electrons are generated during programming, by applying a large negative gate, and drain-to-source voltage. The holes acquire enough kinetic energy, in the high field region near the drain, to surmount the tunnel oxide barrier, and then they are swept into the charge-trapping medium by the gate field. Similar to the case with programming, this technique is faster and uses lower erasing voltages than the erasing with FN tunneling.

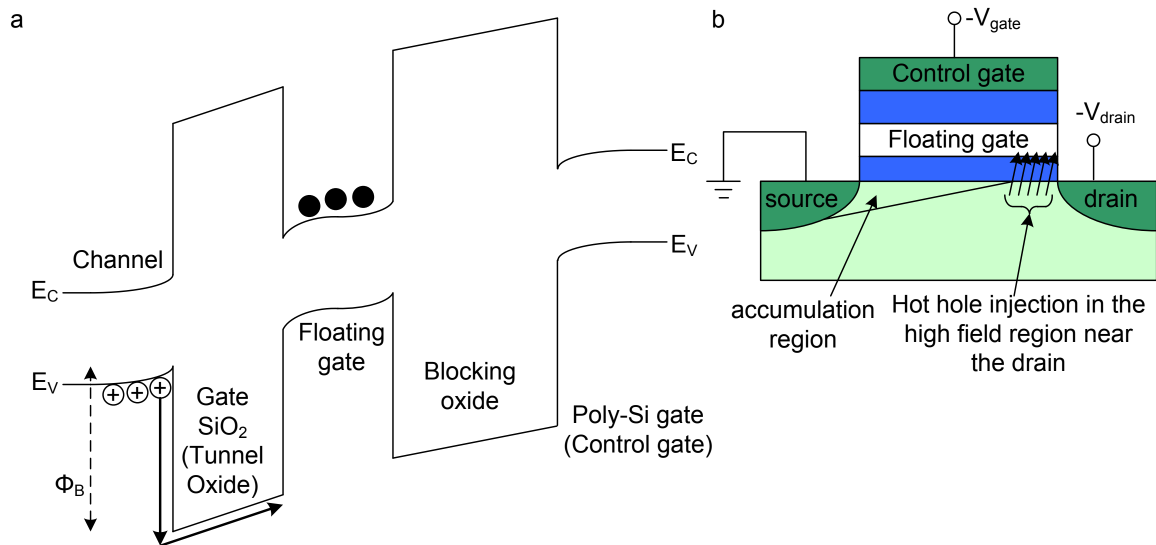


**Figure 5.8. a) Band diagram (near the drain region) of a charge-trapping nonvolatile memory device during erasing using channel hot hole injection. b) Selective injection near the drain terminal of the device (floating gate implementation shown, but applicable to all other implementations as well).**

*Retention*

Retention in charge-trapping memory is determined by the rate at which the trapped charge (electrons in the case of an electron-trapping n-type non-volatile transistor) leak out of the charge-trapping medium. As shown in Figure 5.9, the overall rate is determined by the sum of the different leakage mechanisms, which are thermal emission, trap-to-band tunneling, band-to-trap tunneling, and trap-assisted tunneling.

Thermal emission: trapped electrons are thermally excited from the charge-trapping medium to the conduction band of the tunnel oxide (or blocking oxide). They then drift into the substrate (or

the poly-Si gate) under the influence of the internal electric field from the remaining trapped charge. Because it requires thermal energy, this process is strongly temperature dependent.

Trap-to-band tunneling: trapped electrons tunnel from the charge-trapping medium, through the tunnel oxide, to the conduction band of the poly-Si gate.

Band-to-trap tunneling: holes tunnel from the valence band of the poly-Si gate, through the tunnel oxide, to the charge-trapping medium, where they recombine with the trapped electrons.

Trap-assisted tunneling: trapped electrons tunnel from the charge-trapping medium to a intermediary defect state in the tunnel oxide, then tunnel from the intermediary defect state to the conduction band of the poly-Si gate.

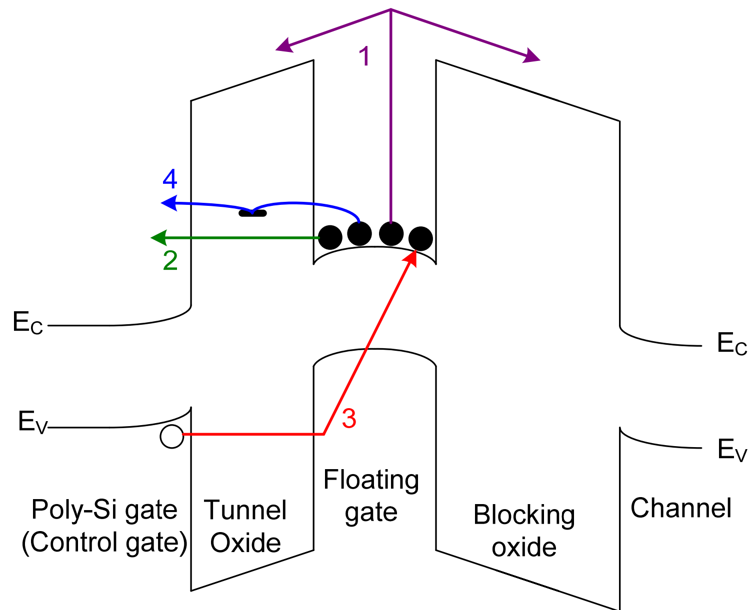


**Figure 5.9. Band diagram of a programmed charge-trapping memory transistor, with all the different leakage paths for trapped electrons to escape from the charge-trapping medium. 1: thermal emission, 2: trap-to-band tunneling, 3: band-to-trap tunneling, 4: trap-assisted tunneling (floating gate transistor shown, applicable to other implementations as well).**

*Endurance*

As the memory device is subjected a large number of program/erase pulses during operation, the difference between the threshold voltages of the two states (or memory window) begins to shrink, and the retention time also shortens. This is a manifestation of tunnel oxide degradation, caused by the high writing/erasing electric field applied to the device [20][21]. The

high electric fields create high energy carriers that collide with the tunnel oxide lattice and break bonds. The broken bonds serve as trapping sites and defects which mediate leakage. In devices that use FN tunneling for programming and erasing, defect creation is uniform across the device and in devices that use HCI for programming and erasing, the defect creation is clustered near the drain terminal [21]. Typical tunnel oxides in charge-trapping non-volatile memory can withstand up to $10^5 – 10^6$ cycles, before the memory window becomes undetectable to the external circuitry or the retention time becomes unacceptably short.

### 5.1.2. Ferroelectric memory

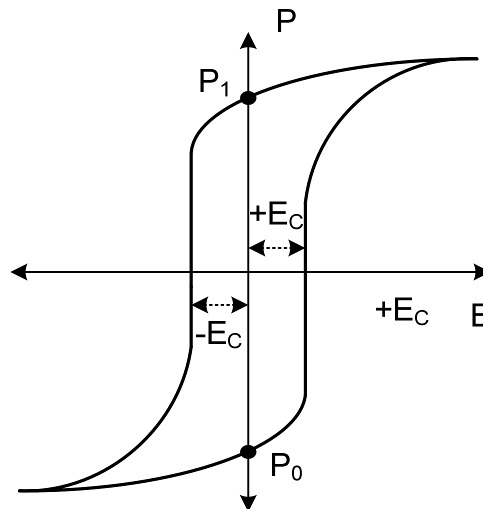


**Figure 5.10. A typical hysteresis curve of an FE capacitor. $P_0$ and $P_1$ represent the two state polarization states at zero applied bias. EC is the critical electric field needed to switch between polarizations.**

Charge-trapping non-volatile memory has limited endurance, because the high voltage programming and erasing processes degrade the gate dielectric material. One potential alternative technology uses ferroelectric (FE) material to get around this problem. FE materials are characterized by a reversible spontaneous polarization in the absence of an electric field [22][23]. The spontaneous polarization arises from a noncentrosymmetric arrangement of ions in its unit cell, which combine to produce an electric dipole moment. These electric dipole moments are stable without external applied field to sustain them, and they are the basis for non-volatile

storage of information in FE-based memories. In the simplest form, a FE-based memory device is simply a thin-film capacitor with an FE material as the dielectric.

*Write/erase mechanism*

When a sufficiently large external voltage is applied to a FE capacitor, there is a net ionic displacement in the unit cell of the FE material. The unit cells interact constructively and form domains, which remain poled in the direction of the applied field even after the removal of the applied voltage. This polarization requires compensation charge to remain on the plates of the capacitor and it is this compensation charge which causes hysteresis in the polarization vs applied external voltage curve [24], as shown in Figure 5.10. At zero applied field, there are two stable states of polarization, which do not require external field to maintain. The memory device can be toggled between these two states, labeled $P_0$ and $P_1$ in Figure 5.9, by applying an electric field with the corresponding polarity, exceeding the critical field strength, $E_C$. The toggling of polarization in programming/erasing operations is less damaging to the FE material than FN tunneling and HCI are to the tunnel oxide in charge-trapping non-volatile memories. Therefore, FE memory has significantly better endurance performance.

*Read mechanism*

If a voltage is applied to a FE memory capacitor in a direction opposite of the current polarization, the domains will switch, requiring compensating charge to flow onto the capacitor electrodes. If the applied voltage is in the same direction as the current polarization, no change in compensating charge occurs and a smaller amount of charge flows to the capacitor. The different transient currents, as shown in Figure 5.11, are amplified and read by external circuitry to determine the state of the memory. Note that the read operation in this case is destructive, because it changes the memory state of the device if the current polarization is opposite the reading voltage pulse. Therefore, the memory must be re-programmed every time it is read.

The destructive nature of the read operation can lead to data loss if the power is lost during the read. The FE memory field effect transistor (FEMFET) remedies this shortcoming by offering a non-destructive method of the read out [25]. The FEMFET has a structure very similar

to that of the MNOS charge-trapping based non-volatile memory. Only instead of the nitride charge-trapping layer, the FEMFET has a layer of FE material. From an operation perspective, the FEMFET is very also very similar to the charge-trapping based non-volatile memories. The FEMFET is programmed/erased by applying large fields that set the remnant polarization in the layer of the FE material in the gate stack. The polarization alters the field distribution in the gate stack, which in turn changes the threshold voltage of the transistor. This change can be read out (using the drain-source current differential in the two different states) by using a lower applied gate voltage that does not disturb the polarization. As such, the FEMFET benefits from both the high endurance of FE material and the non-destructive readout of the charge-trapping based non-volatile memory. However, it suffers from poor retention time due to depolarization fields that are caused by charge trapping in the gate oxide and FE film [26].

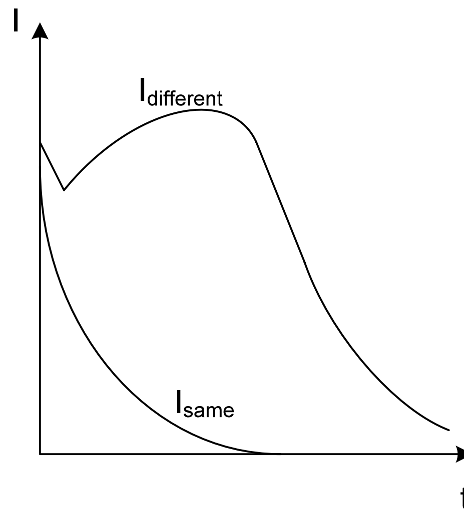


**Figure 5.11. Transient currents of the FE memory capacitor when a read voltage is applied to it. $I_{different}$ and $I_{same}$ represent the transient response when the current polarization has a different and same direction as the read voltage pulse, respectively.**

### 5.1.3.Phase change memory

There has been a great deal of interest in phase change memory (PCM) in recent years because of its potential to offer significantly better memory density through scaling of device dimensions. While the charge-trapping based non-volatile memories are limited by the scaling of the FET, no physical limits are known for PCM scaling [27][28]. In this type of memory, the

memory element is a layer of chalcogenide material (GeSbTe, AsTeGe, etc.) whose conductivity can be changed by changing its phase. When the chalcogenide material is in the amorphous phase, it has a very low conductivity. When it is in the crystalline phase, it has a very high conductivity. The difference in conductivities between the two states is typically many orders of magnitude. As such, PCM has the benefit of having a very large memory window.

*Write/erase mechanism*

The mechanism used to change the chalcogenide material between amorphous and crystalline states is Joule heating. To change the material from crystalline phase to amorphous, a large amount of current is applied to heat it above its melting point. This is followed by quick quenching to lock it into the amorphous state. To change the material from amorphous to crystalline, a smaller amount of current is applied to heat it to a critical temperature below the melting point, where crystallization can occur. The current is sustained over a longer period of time to allow for complete crystallization. As can be seen in Figure 5.12, in practice the PCM memory element is realized by using a small heating element, which only address a small volume of chalcogenide material. This reduces the current needed to induce phase change and the possible cross interference between neighboring elements.

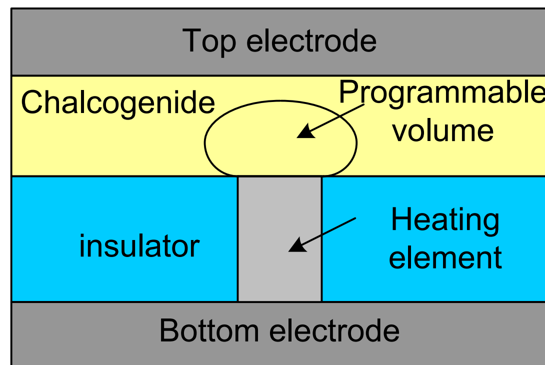


**Figure 5.12. Structure of a PCM memory element, after [27].**

The durations of current pulses used in write/erase are typically 500ns and 50ns for amorphous-to-crystalline and crystalline-to-amorphous transitions, respectively. The magnitudes of current pulses are typically larger than 1mA based on an 180nm lithography process. This

needs to be reduced for practical applications. Power consumption reduction can be achieved by further scaling down the memory element volume. Innovative methods such as edge contact [29] and increasing chalcogenide resistance through nitrogen doping [30] have been explored as well.

*Read mechanism*

PCM is read by measuring the conductivity of the memory element. This is done by passing very low levels of current, which do not result in joule heating or phase change, through the device and measuring the output voltage.

*Retention*

Retention is generally not considered an issue in PCM memory, because the phase of intrinsic chalcogenide material is stable in the normal operating temperature range of the material. Studies have shown retention times better than the industry standard of 10 years at 85°C [27]. However, impurities and extrinsic defects are expected to be limiting factor for retention in high volume manufacturing of PCM [27].

*Endurance*

PCM exhibits excellent endurance characteristics, no degradation is observed up to $10^{12}$ write/erase cycles [27][28]. This is one of the major advantages of PCM over other forms of non-volatile memories.

**5.1.4. Magneto-resistive memory**

Magneto-resistive memory (MRAM) has been extensively studied and developed over the past decade, because it offers much faster read, write/erase times and has much better retention characteristics than charge-trapping based non-volatile memory. Some suggest that it has the potential to be the universal memory that replaces all other implementations [31]. At the core of MRAM is the magnetic tunnel junction, which is a layered structure with a thin insulator layer separating two layers of ferromagnetic material. One of the ferromagnetic layers has a permanent polarization, while the other one has a free polarization that can be changed. The insulating layer is thin enough to allow electrons to tunnel through it. The tunneling resistance of

the junction is determined by the relative alignment of the magnetic polarization of the two ferromagnetic layers.

*Write/erase mechanism*

Writing and erasing the MRAM involves changing the magnetic polarization of the “free magnet”. In the simplest implementation, this is done by passing currents through the orthogonally oriented electrodes above and below the tunnel junction [32]. These currents induce a magnetic field at the junction, with which the free magnet aligns. This approach requires very high levels of current, making it unattractive for low power applications. Furthermore, as element density is increased, there is an increasing likelihood of the induced field affecting neighboring memory elements or false write.

Another approach, the toggle mode, uses a more complex multi-layered structure (called the synthetic antiferromagnet) to address the false write issue. The resulting memory element has only two stable states, which can be toggled by applying a “rotating” magnetic field. The “rotation” is achieved by applying currents to the orthogonally oriented electrodes asynchronously with a precisely controlled phase delay [33]. The phase delay is necessary to toggle the memory state of the junction. As a result, the likelihood of falsely changing the neighboring element is significantly reduced. However, this approach still requires a significant amount of current to achieve the toggling of memory states.

A new technique, spin-transfer torque, reduces the current level needed to change the state of the memory element. It does so by using spin-polarized electrical current to change the magnetic polarization of the free magnet through an exchange of spin angular momentum [34]. The difficulty with this technique lies in maintaining spin coherence in the electrical current.

*Read mechanism*

The memory state is determined by measuring the resistance of the magnetic tunnel junction. This is achieved by applying a small voltage to the junction and measuring the resulting current. However, because of the small magnitude of the read signal, the read time of the MRAM is relatively high [31].

*Retention*

MRAM data retention is inversely proportional to rate of polarization change of the free magnet under thermal excitation. Accelerated tests predict no observable thermal change rate under normal operating conditions [35]. Therefore, MRAM have excellent retention characteristics that far exceed that of charge-trapping nonvolatile memory.

*Endurance*

While the switching mechanism does not inherently degrade the MRAM memory element, other factors such as voltage stress on the thin dielectric tunnel layer during read and interdiffusion between magnetic layers may affect the long term reliability of the MRAM. However, accelerated tests show that over 10 years of use, these effects do not significantly degrade device performance [35].

#### 5.1.5.Summary and motivation for amorphous silicon non-volatile memory

Charge-trapping memory owes its dominance in the marketplace to its compatibility with existing device structure and manufacturing infrastructure. However, it suffers from limited retention and endurance due to the nature of its write/erase mechanism. Density scaling is also becoming an issue, as transistor length reduction is becoming more difficult. Various new technologies have emerged to address the disadvantages of the charge trapping memory. Ferroelectric memory offers significantly better endurance, but it also has retention and scaling problems. Phase change memory promises excellent retention, endurance and scaling, but it suffers from high power requirement for write/erase. Magneto-resistive memory provides great retention and endurance, but it also has the disadvantage of requiring high write/erase power and long read time. While there are challenges ahead for the new technologies, they have great potential to become real practical alternative to the charge trapping non-volatile memory.

None of these technologies, however, can be easily integrated with a-Si large area electronics applications such as large area x-ray image sensors [36], flexible AMOLED displays [37] and sensor skin [38]. To be used in an a-Si large area electronic system, they would need to

be incorporated as an external component, which can incur significant integration cost. This extra cost may be avoided, if there were a memory technology that is compatible with existing a-Si device structure and fabrication process. This technology would also have the potential to greatly extend the functionality of existing a-Si large area electronic systems and create novel applications.

## 5.2. Amorphous silicon non-volatile memory transistor

Much like the VLSI MOS transistor was the basis for VLSI charge trapping memory, the a-Si TFT can be the foundation for a-Si charge trapping memory. If designed to be compatible with existing TFT fabrication processes, memory devices based on a-Si TFT could provide a low cost and efficient way to integrate memory capabilities into large area electronics.

### 5.2.1. Initial demonstration and drawbacks

An amorphous silicon floating gate TFT (FGTFT) was first demonstrated by Kuo and Nominanda in 2006 [39]. Their FGTFT structure is identical to that of a conventional bottom-gate a-Si TFT, except the gate dielectric was a sandwich structure consisting of a $SiN_x$/a-Si/$SiN_x$ tri-layer, with the $SiN_x$ layers having equal thickness. The a-Si layer was not patterned. This initial demonstration had a rather small memory window of 0.5V and a short retention time of about 1 hour, making it not suitable for practical applications.

With a slight modification of the conventional a-Si TFT fabrication process, we designed a slightly different a-Si floating gate TFT memory device. The structure of our a-Si FGTFT memory device is shown in Figure 5.13 along with that of the standard TFT control device. The fabrication processes are identical up to the deposition of the gate dielectric, where, in the floating gate process, the deposition of the gate SiNx is interrupted to deposit a thin layer of a-Si to serve as the floating gate. After the a-Si floating gate is patterned with an additional lithography and RIE step, another layer of thin layer of gate $SiN_x$ is deposited on top to form the tunnel dielectric. From

this point forward, the floating-gate process proceeds the same way as the conventional a-Si TFT process. For a detailed description of the fabrication process refer to appendix C.

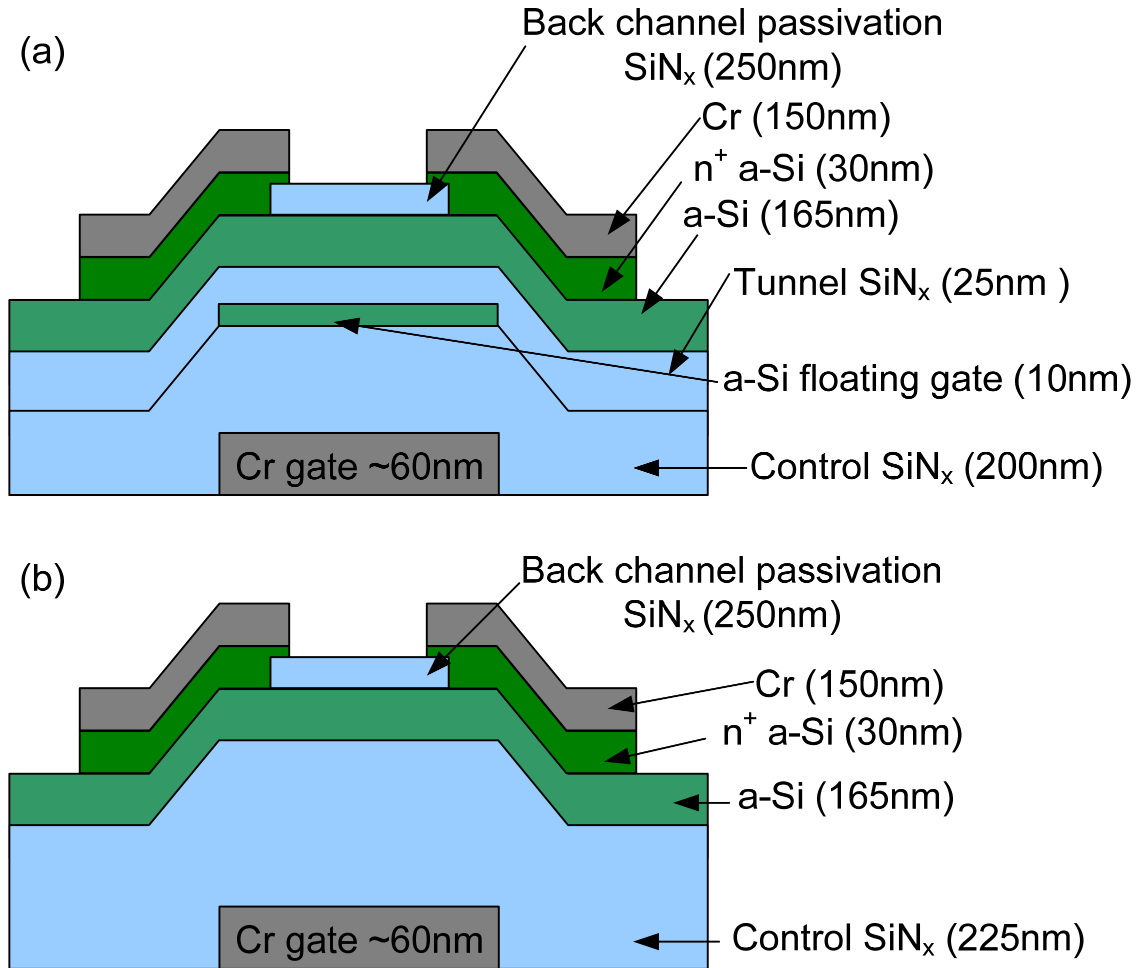


**Figure 5.13. (a) Structure of the a-Si floating gate transistor memory device. (b) Structure of the conventional bottom gate a-Si TFT control device.**

The a-Si floating gate TFT (FG-TFT) memory functions in the same way as the conventional VLSI floating gate transistor memory. Electrons tunnel, through the tunnel SiNx, into the floating gate from the a-Si channel or out to a-Si channel from floating gate via FN tunneling, depending on the sign of the applied gate voltage bias (Figure 5.14). HCI is not used in this structure, because the short scattering length in a-Si would make this method of write/erase

ineffective. The charge stored in the floating gate alters the threshold voltage of the FG-TFT, which serves as the memory state.

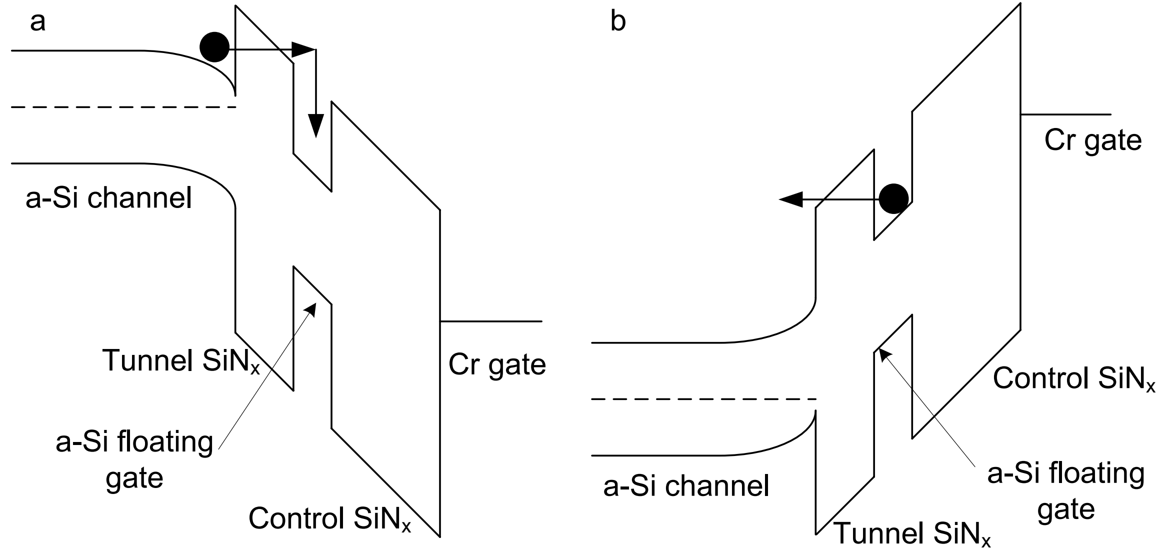


**Figure 5.14. Band diagram of FG-TFT under the programming condition (a) and the erasing conditions (b).**

The FG-TFT exhibits a $V_T$ shift of ~4V after the application of a programming voltage of 32V to the control gate terminal, with the source and drain (S/D) terminals grounded, for 10ms. An erasing voltage of -50V on the control gate (S/D grounded) for 10ms forces the trapped electrons out of the floating gate and $V_T$ returns to its pre-program value (Figure 5.15). When the control device is subjected to the same cycle, no appreciable $V_T$ shift is observed.

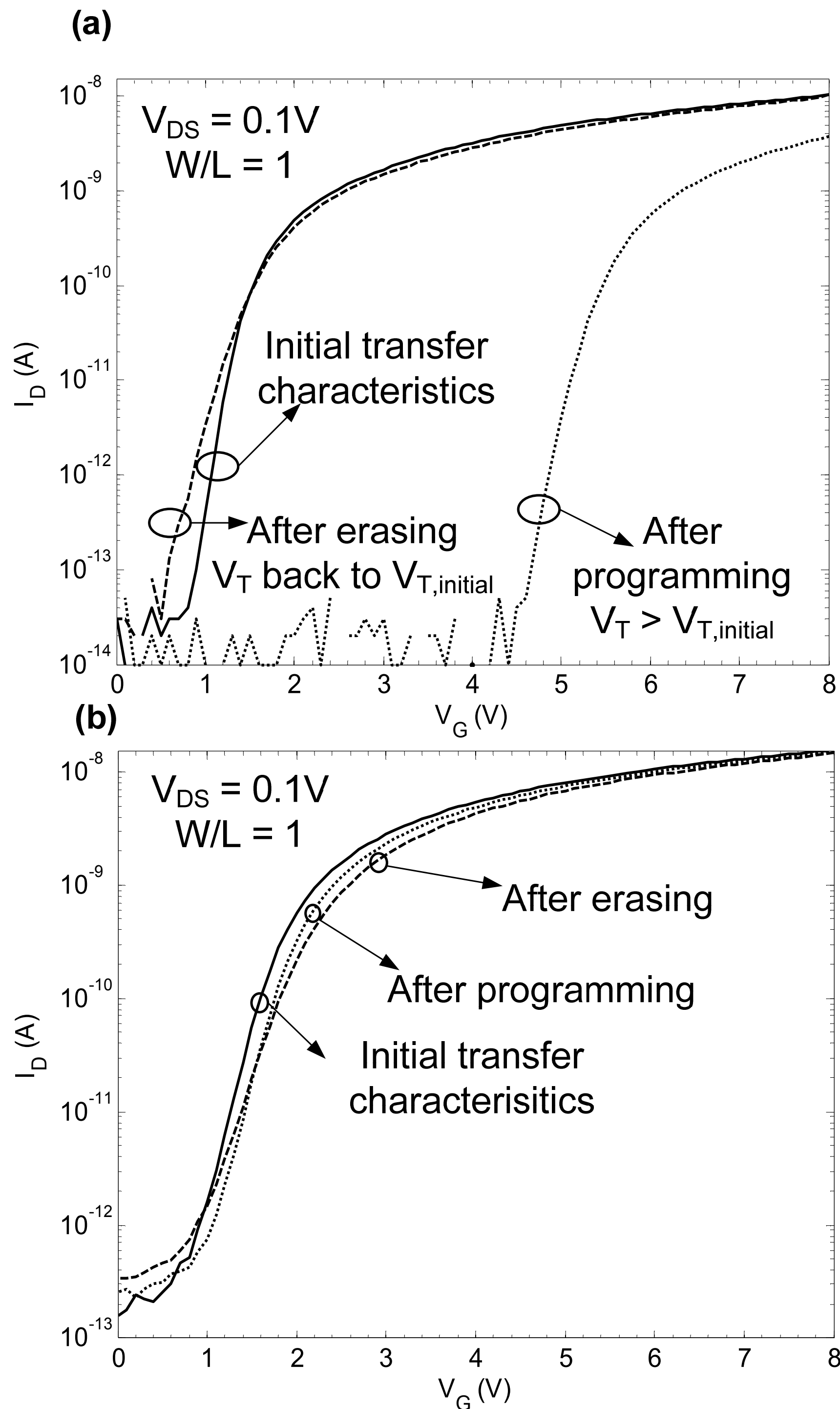


**Figure 5.15. The DC transfer characteristics ($V_{DS}$ = 0.1V & $V_{GS}$ swept from 8V to 0V in 0.1V increment) of the FG-TFT memory device (top) and control device (bottom) at various stages of the program/erase cycle. Program: gate held at 32V with S/D grounded for 10ms; erase: gate held at -50V with S/D grounded for 10ms.**

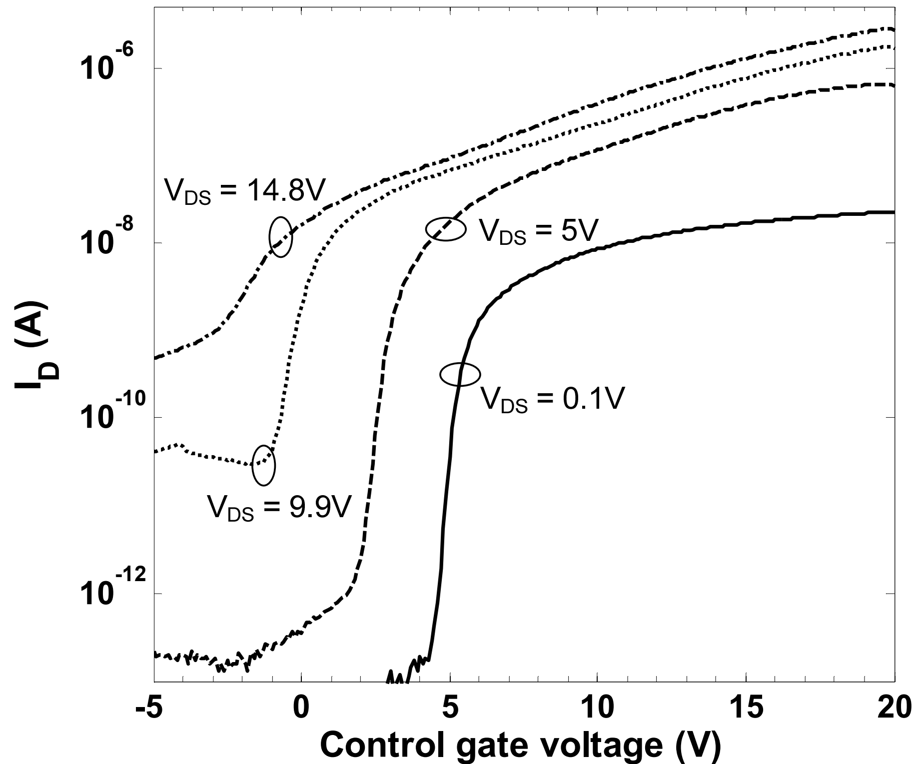


**Figure 5.16. $I_{DS}$ vs $V_{GS}$ (control gate voltage) characteristics of an a-Si floating gate TFT at three different drain bias conditions. Note the different apparent threshold voltage under each drain bias condition.**

This initial demonstration of the FG-TFT memory suffers from two major problems:

(i) strong dependence of threshold voltage and drain saturation current on applied drain bias

(ii) short retention time

The threshold voltage of the FG-TFT decreases with increasing drain voltage bias (Figure 5.16). This also means that the drain current in the saturation regime ($V_{DS} > V_{GS}$-$V_T$), which should (to first order) be independent of drain voltage according to conventional MOSFET theory, depends on the drain bias in the FG-TFT. This drain-voltage dependence is highly undesirable in applications, where a drain-voltage independent threshold voltage and saturation current are required. One such application is the organic light emitting diodes (OLED) driver in an active matrix OLED pixel, where the TFT converts a control voltage (gate voltage) into pixel current (drain-source current) to control the pixel brightness [40]. Therefore drain-voltage dependence must be eliminated for this memory device to be useful in these practical applications.

An extrapolation of the room temperature retention characteristic of the FG-TFT shows that it retains about 26% of the initial injected charge after 10 years of storage (Figure 5.17). This memory window is too small to be reliably detected by the readout circuit. Therefore the retention time must be improved for this device to serve as a practical non-volatile memory element.

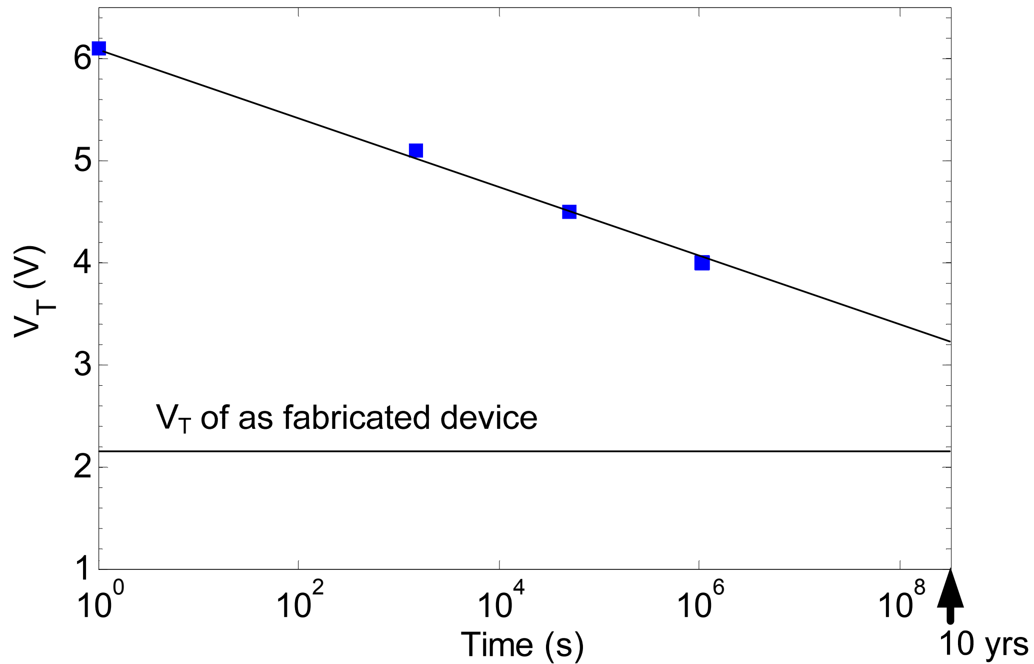


**Figure 5.17. Room-temperature retention characteristic of the FG-TFT.**

### 5.2.2. Eliminating the drain-voltage dependence

The drain-voltage dependence in the FG-TFT characteristics can be understood by examining the capacitive coupling effects. The device can be represented by its equivalent capacitive circuit model, where $C_{fc}$, $C_{fs}$, $C_{fd}$ and $C_{fg}$ are capacitances between the floating gate and channel, source, drain and control gate, respectively (Figure 5.18).

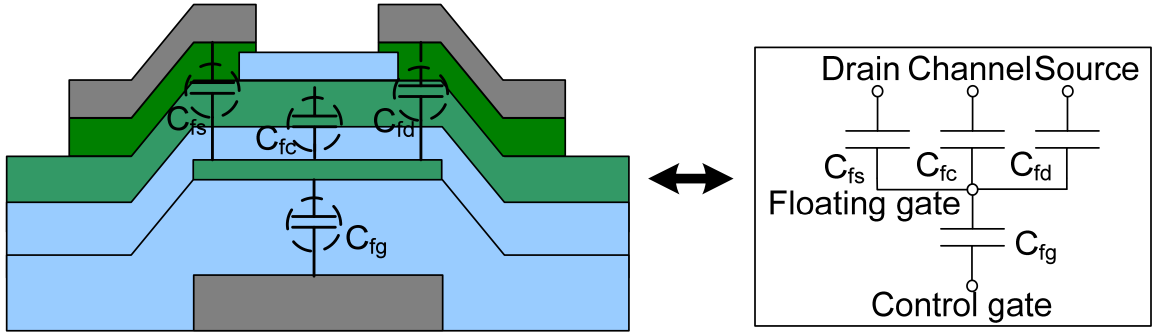


**Figure 5.18. Capacitive network model of the FG-TFT.**

Unlike a conventional a-Si TFT [41] or any other MOS transistor, in the FG-TFT the voltage on the control gate does not directly modulate channel carrier density. Instead, the voltage on the floating gate directly controls channel behavior because of its proximity to the MOS interface. Further, the voltage on the floating gate ($V_{FG}$) node is a combined function of the voltages on the control gate, drain and source electrodes. Assuming a grounded source electrode [42]:

$$V_{FG} = \frac{C_{fg}}{C_T}\left(V_G + fV_D\right) \tag{5.3}$$

Where

$$C_T = C_{fg} + C_{fs} + C_{fc} + C_{fd} \tag{5.4}$$

$$f = \frac{C_{fd}}{C_{fg}} \tag{5.5}$$

Substituting (1) into the equation for conventional MOS transistor saturation current yields [42]:

$$I_{DS} = \frac{\mu C_{CG}}{2}\frac{W}{L}\frac{C_{fg}}{C_T}\left(V_{GS} + fV_{DS} - V_T\right)^2 \tag{5.6}$$

Where $C_{CG}$ is the capacitance of the entire gate stack (between the channel and the control gate) and $V_T$ is threshold voltage with respect to the control gate, not the floating gate.

From (5.6), one can clearly observe that the device saturation current will not be independent of drain-source bias, as is the case in conventional MOS transistors model. This is because the

drain voltage capacitively controls the floating gate voltage. In fact, depending on the ratio *f*, defined in (5.5), the $I_{DS}$ vs $V_{DS}$ curves can have a large positive slope in the saturation regime. Furthermore, $I_{DS}$ vs $V_{GS}$ (control gate voltage) curves will show different apparent threshold voltages depending on the applied drain bias. This is illustrated in Figure 5.19(a), where $I_{DS}$ is shown as a function of control gate voltage at various different drain biases. Figure 5.19(b) shows the same set of current data with the x-axis transformed to floating gate voltage using (5.3). Since the voltage on the floating gate voltage is what the channel sees directly, the threshold voltage with respect to the floating gate is the intrinsic channel threshold. As a result, there are no differences in the observed $V_T$ of the various curves of Figure 5.19(b). This shows that the drain-voltage dependent $V_T$ and saturation current in the FG-TFT are indeed due to the fact that drain voltage affects the channel carrier density through capacitive coupling with the floating gate.

*New device structure*

The drain-voltage dependences of the FG-TFT on drain voltage can be eliminated if the overlap capacitance between the drain and the floating gate is eliminated. This can be done with careful lithographic alignment, but that is not amenable to low-cost manufacturing over large areas. A more elegant method is to replace the floating gate with a charge trapping medium that is not conductive (Figure 5.20). In the new approach, a high defect density interface is used as the charge storage medium. Because the discrete traps are separated spatially, stored electrons cannot move around in the charge-trapping medium. Therefore the charge-trapping medium is effectively an insulator. As such, any capacitive coupling from the drain to the traps cannot affect the electric field from the control gate and cannot produce a change in the potential distribution in the gate stack, and will therefore not affect the channel carrier density.

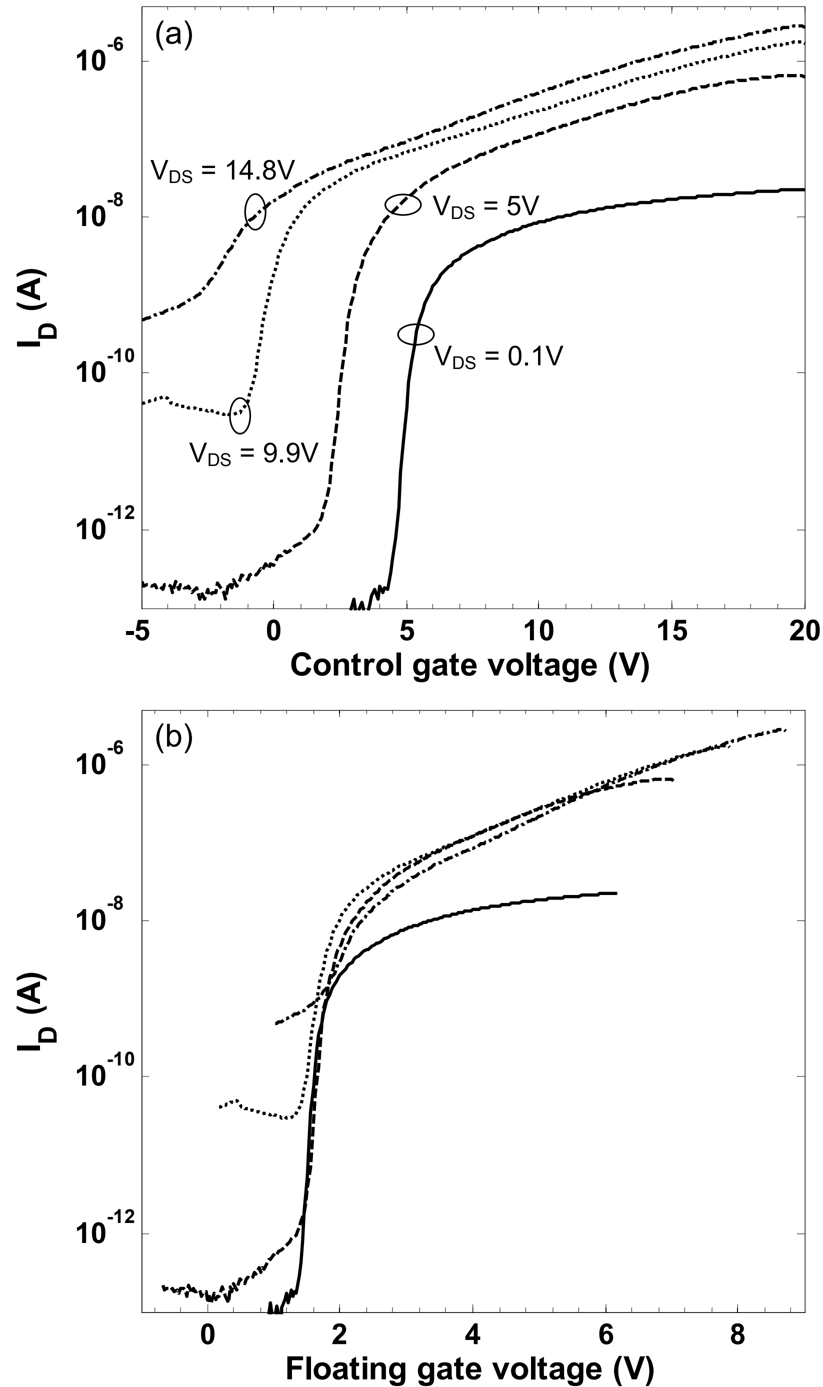


**Figure 5.19. (a) $I_{DS}$ vs $V_{GS}$ (control gate voltage) characteristics of an a-Si floating gate TFT at three different drain bias conditions. Note the different apparent threshold voltage under each drain bias condition. (b) same $I_{DS}$ data as (a) plotted vs $V_{FG}$ (floating gate voltage). Floating gate voltages are calculated via equation (5.3). With respect to the floating gate, $V_T$ of the different curves are the same.**

The fabrication process of the new device structure is nearly identical to that of the standard a-Si TFT, except that the gate nitride deposition is interrupted to deposit a thin layer (~10nm) of a-Si. The a-Si is immediately etched away using reactive ion etch. The overetch damages the top nitride surface, resulting in the traps responsible for charge storage. A thin layer of nitride is then deposited over the traps as the tunnel gate dielectric. The fabrication process then proceeds in the same way as that of the conventional a-Si TFT. See appendix C for more detail on the fabrication process. Our proposed structure, which we will refer to as the $SiN_x$ trap TFT (ST-TFT), is very similar the VLSI SONOS type non-volatile memory transistors, in which electrons tunnel through the tunnel gate oxide layer to be trapped in the defects at the $SiO_2/Si_3N_4$ interface.

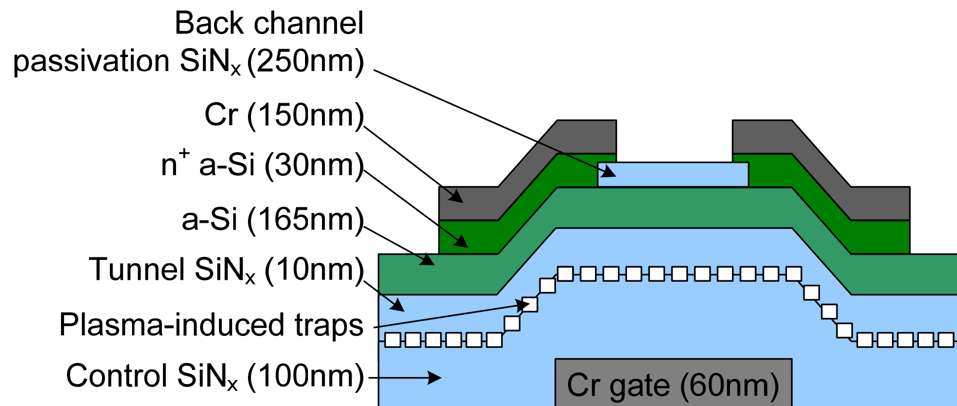


**Figure 5.20. Structure of the ST-TFT.**

The drain-source current vs gate-source voltage characteristics of a $SiN_x$ trap TFT memory device, at three different drain-source bias conditions, are shown in Figure 5.21(a). Unlike the FG-TFT, $V_T$ is not dependent on the applied drain bias. This is because any capacitive coupling from the drain to the traps does not affect the number of carriers in the channel and the control gate directly modulates channel behavior. The drain-source current vs drain-source voltage characteristics of a $SiN_x$ trap TFT memory device are shown along with that of a floating gate memory device with the same aspect ratio, dielectric thickness, and process conditions (Figure 5.21(b)). The two devices were on the same wafer, sharing all the process steps except the floating gate device did not have the floating gate etched away. The $SiN_x$ trap device has a clear saturation regime, where the drain current is nearly independent of the drain voltage. The

floating gate device, on the other hand, has drain current that increases with increasing drain bias, which results from capacitive coupling between the drain and the floating gate.

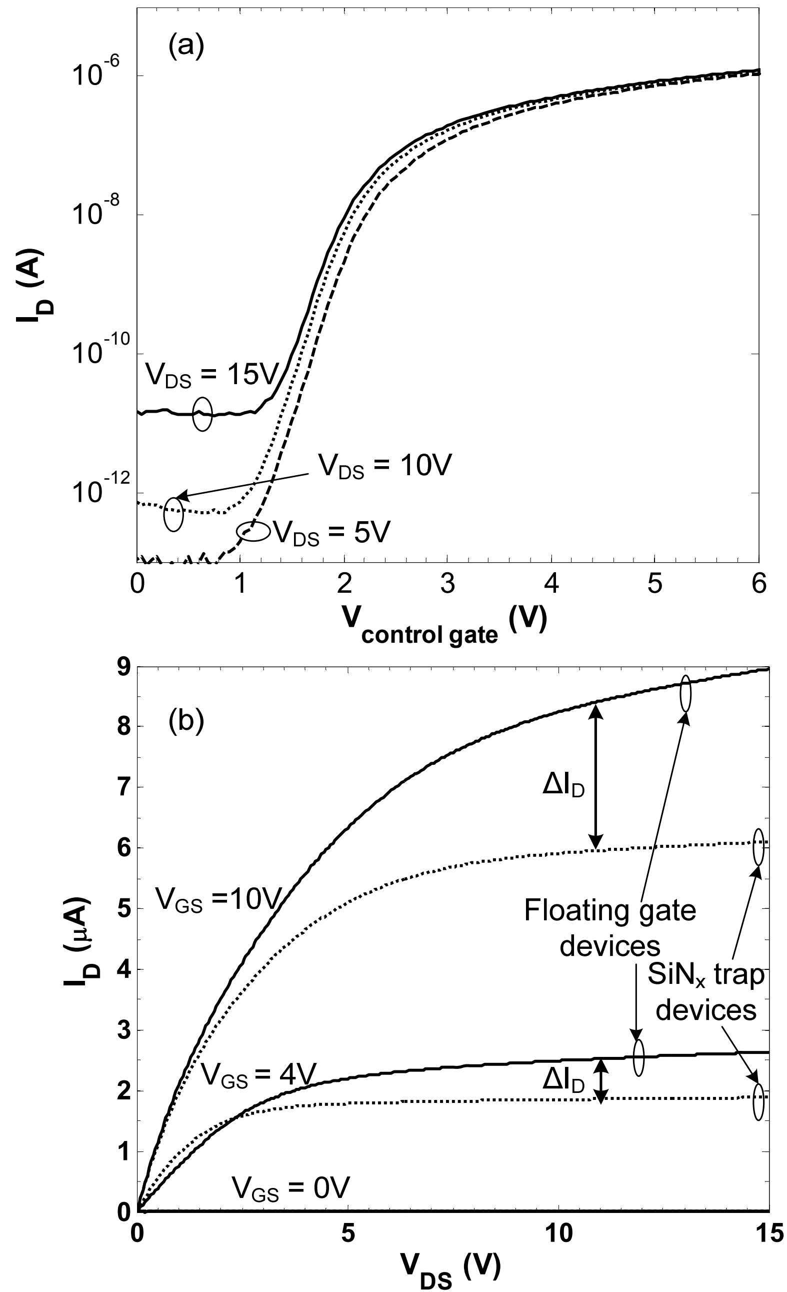


**Figure 5.21. (a) $I_{DS}$ vs $V_{GS}$ characteristics of an a-Si $SiN_x$ trap TFT at three different drain bias conditions. (b) $I_{DS}$ vs $V_{DS}$ characteristics of an a-Si $SiN_x$ trap TFT an a-Si floating gate TFT, at three different gate bias conditions. Note the difference in saturation drain current.**

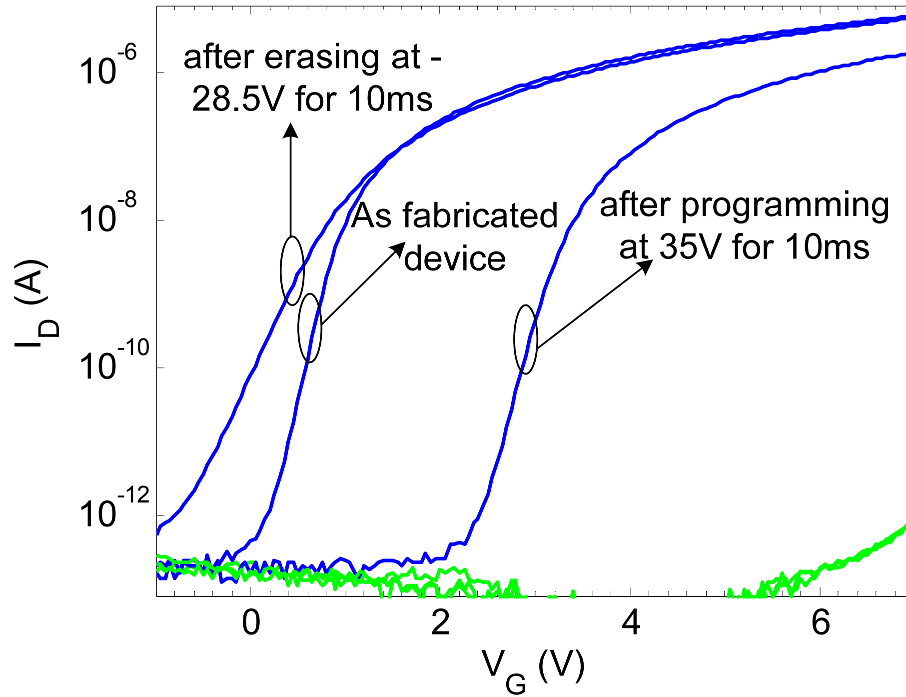


**Figure 5.22. $I_{DS}$ vs $V_{GS}$ characteristics of the $SiN_x$ trap TFT at various stages of the program/erase cycle. Program: $V_{GS}$ = 35V held for 10ms with S/D grounded; Erase: $V_{GS}$ = -28.5V held for 10ms with S/D grounded.**

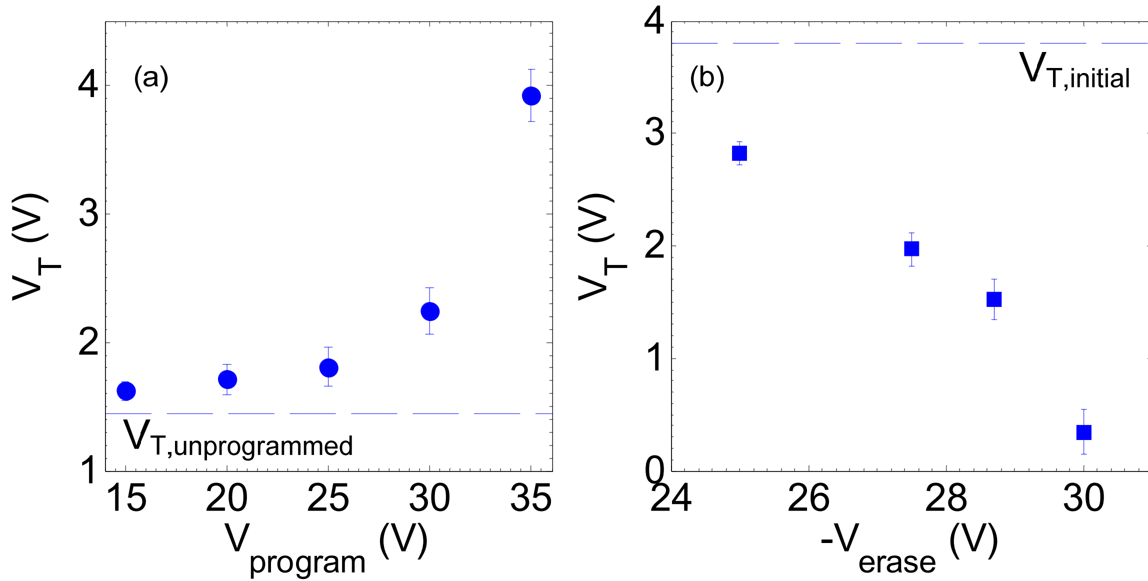


**Figure 5.23. (a) Programming characteristics of the ST-TFT. Devices are programmed with S/D grounded, and $V_{program}$ applied to the gate for 10ms. (b) Erasing characteristics of the ST-TFT. Devices are first programmed to $V_{T,initial}$ with S/D grounded, and 35V applied to the gate for 10ms. They are then erased by applying $V_{erase}$ to the gate for 10ms with the S/D grounded.**

The ST-TFT eliminates the undesirable drain-voltage dependences without compromising its memory functionality. Similar to the floating gate memory device, the non-volatile effect in the $SiN_x$ trap memory devices is based on electrons tunneling into the $SiN_x$ traps from the channel for programming, and out from the $SiN_x$ traps into the channel for erasing, under the applied gate field. Again, no drain field or hot electron effects are involved. Figure 5.22 shows the drain-source current vs gate-source voltage characteristics of a ST-TFT before programming, after programming and after erase. Reversible $V_T$ shifts can be clearly observed. The threshold voltage of the ST-TFT can be reliably tuned to high and low values by applying the corresponding programming and erasing voltage pulses to the gate. The resulting $V_T$ of the ST-TFT device depends on the magnitude of the positive and negative voltage pulses (Figure 5.23).

### 5.2.3.Improving the retention time

The short retention time of the FG-TFT is also related to the fact that the stored electrons are mobile in the conductive floating gate. If there were “weak” points in the tunnel $SiN_x$, where a pin hole or a cluster of defects created a leakage path, all the stored electrons can escape through these paths of lesser resistance. As result, the rate of threshold voltage decay will be much faster than that resulting from conventional charge loss mechanisms discussed in section 5.1.1. This is similar to the retention problems observed in aggressively scaled VLSI c-Si floating gate transistors, where the threshold voltages decay abnormally fast due to leakage through the defects in the thermal oxide. The ST-TFT, on the other hand does not suffer from this problem, because the electrons are stored in localized traps at the charge-trapping interface. This is manifested in a significant improvement in room-temperature retention characteristics of the ST-TFT compared to the FG-TFT (Figure 5.24). The FG-TFT was programmed with a 32V, 10ms gate voltage pulse and the ST-TFT was programmed with a 35V, 10ms gate voltage pulse. The ST-TFT exhibited a threshold voltage shift of about 2.4V and the FG-TFT exhibited a threshold voltage shift of about 4V. The threshold voltages after programming were measured at room temperature for both devices up to $10^6$s. Extrapolation of the data to longer time showed that the

ST-TFT retained about 52% of the injected charge after 10 years – twice the amount retained by the FG-TFT.

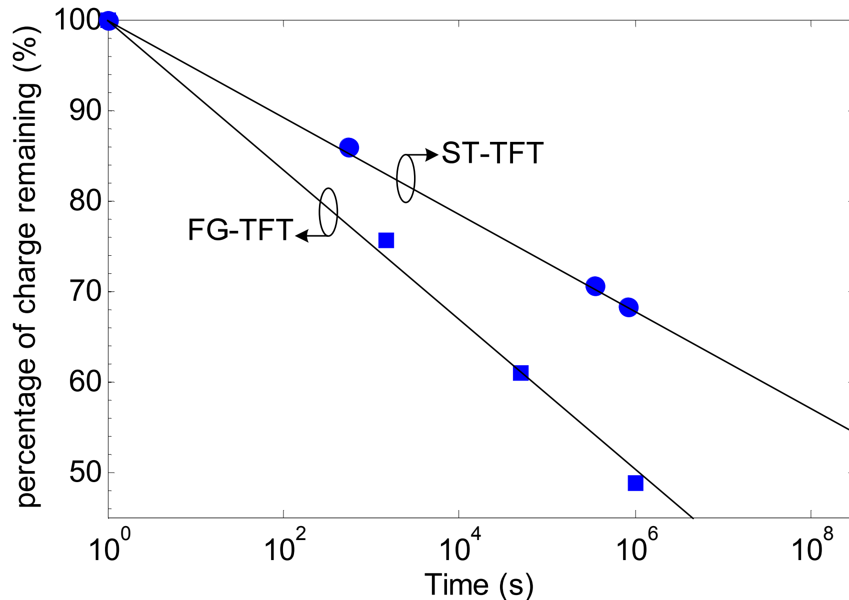


**Figure 5.24. Room temperature retention characteristics of the FG-TFT and ST-TFT. Both were programmed with a 35V, 10ms gate pulse. Lines represent linear fit extrapolation.**

Despite the improvement over the FG-TFT, ~50% charge loss in the ST-TFT still represents a significant decay of the memory window. As such, the retention performance of the ST-TFT needs further improvement. In order to improve the retention time, it is crucial to identify the dominant leakage mechanism(s) of the electrons stored in the $SiN_x$ traps. Of the four potential leakage mechanisms illustrated earlier in Figure 5.9, trap-to-band (T-B) and band-to-trap (B-T) are likely to be insignificant contributions to charge loss, because direct tunneling currents will be negligibly small at a tunnel $SiN_x$ thickness of 10nm [43]. As such, there are two charge-loss mechanisms that are potentially responsible for the short retention time of the ST-TFT. These two leakage pathways are schematically illustrated in a simplified band diagram of the ST-TFT in the programmed state (Figure 5.25), where it is assumed that: (1) there is a high density of defects at the charge trapping interface that is distributed in energy, (2) most of the injected electrons are trapped in the defects at the charge trapping interface so that most of the charge is localized at this interface, (3) defect levels exist in the adjacent tunnel $SiN_x$ films, but the density is much

smaller compared to that of the charge trapping interface and they are mostly uncharged in the programmed state, so that they do not disturb the band.

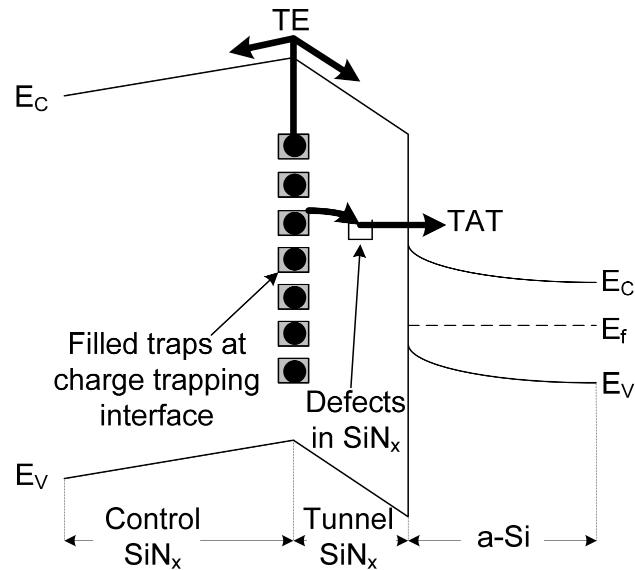


**Figure 5.25. Band diagram of the ST-TFT in the programmed state. Potential charge loss mechanisms include trap assisted tunneling (TAT) and thermal excitation (TE).**

Electrons stored at the charge trapping interface can escape by thermal emission (TE), where they are excited into the conduction of the $SiN_x$ by thermal energy and are then swept into the a-Si channel or metal gate by the built-in field from the trapped charges (Figure 5.25). They can also escape via trap-assisted tunneling (TAT), where they hop to an unoccupied defect state in the adjacent tunnel $SiN_x$ film, and then tunnel from the defect to the a-Si channel (Figure 5.25). The rate of charge loss due to the thermal emission process is expected to be highly temperature dependent, whereas that of the trap-assisted tunneling process is expected to be relatively insensitive to temperature. As such, the relative contribution of the two processes to the overall charge loss can be distinguished by examining the retention characteristics of the ST-TFT at different temperatures.

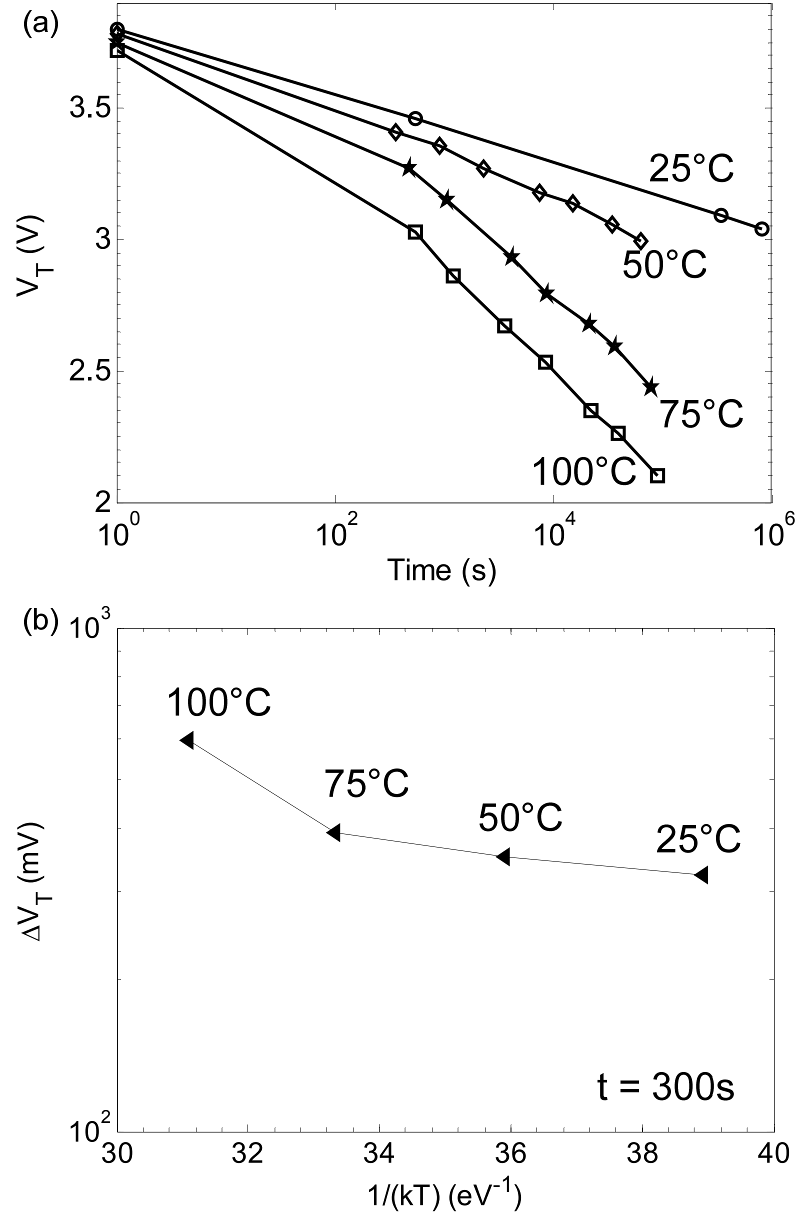


**Figure 5.26. (a) Retention characteristics of the standard ST-TFT at various temperatures (b) Arrhenius plot of $\Delta V_T$ (t = 300s) as a function of $(kT)^{-1}$.**

The ST-TFTs were first programmed using 35V, 10ms gate voltage pulse, to a threshold voltage of ~3.8V. The retention characteristics of the ST-TFTs were then measured at temperatures ranging from 25°C to 100°C (Figure 5.26(a)). An Arrhenius plot of the $V_T$ decay at different temperatures for a fixed time (300s) after programming, reveals two temperature

regimes (Figure 5.26(b)). At lower temperatures (25°C ~ 75°C), the $V_T$ decay is very weakly dependent on temperature (the slope of the Arrhenius plot is flat), and at higher temperatures (>75°C), the $V_T$ decay is much more strongly dependent on temperature (the slope of the Arrhenius plot is steeper). This suggests that the ST-TFT room-temperature retention characteristic is likely dominated by trap-assisted tunneling, which has a weak dependence on temperature. The charge loss contribution from the thermal emission process is insignificant compared to the trap-assisted tunneling process, until the temperature is elevated beyond at least 75°C.

The rate of charge loss due to trap-assisted tunneling is proportional to the density of tunnel-mediating defects in the tunnel $SiN_x$ [44]. Therefore, we can improve room-temperature retention performance of the ST-TFT by reducing the defect density in the bulk of the tunnel $SiN_x$ film. It is well known that in PECVD $SiN_x$, Si-Si and Si dangling bonds result in defect states in the bandgap [45]. The density of these defects can be reduced by using a high ammonia-to-silane precursor flow ratio to promote the formation of Si-N and Si-H bonds, which do not give rise to defects in the bandgap [46]. The addition of hydrogen as a precursor gas to the deposition plasma of $SiN_x$ is also known to promote a more energetically favorable bond configurations with fewer defects [47]. The standard $SiN_x$ was deposited with $SiH_4/NH_3$ flow rates of 14/130sccm. We fabricated an improved ST-TFT with tunnel $SiN_x$ recipe that incorporates a higher $NH_3/SiH_4$ flow ratio and $H_2$ dilution ($SiH_4/NH_3/H_2$ = 5/125/75sccm). The deposition temperature (300°C), plasma power density (22mW/cm$^2$) and the deposition pressure (500mT) remained unchanged.

The improved ST-TFT non-volatile device was programmed to a threshold voltage of ~3.8V and the threshold voltage after programming was measured at temperatures ranging from 25°C to 100°C. The improved device had retention performances that were superior to the standard device at temperatures ranging from (25°C – 100°C) (Figure 5.27). A comparison of the Arrhenius plots of the standard and improved $SiN_x$ ST-TFTs (Figure 5.28) shows a reduction of $V_T$ decay in the improved device from the standard device, and the magnitude of the reduction is relatively insensitive to temperature. This confirms that we have indeed reduced the charge loss

contribution from a weakly temperature-dependent process, such as trap-assisted tunneling. Extrapolation of the data to longer times showed the ST-TFT with standard tunnel $SiN_x$ retained about 52% of the initial injected charge after 10 years and the ST-TFT with the improved tunnel $SiN_x$ retained about 75% of the initial injected charge after 10 years (Figure 5.29).

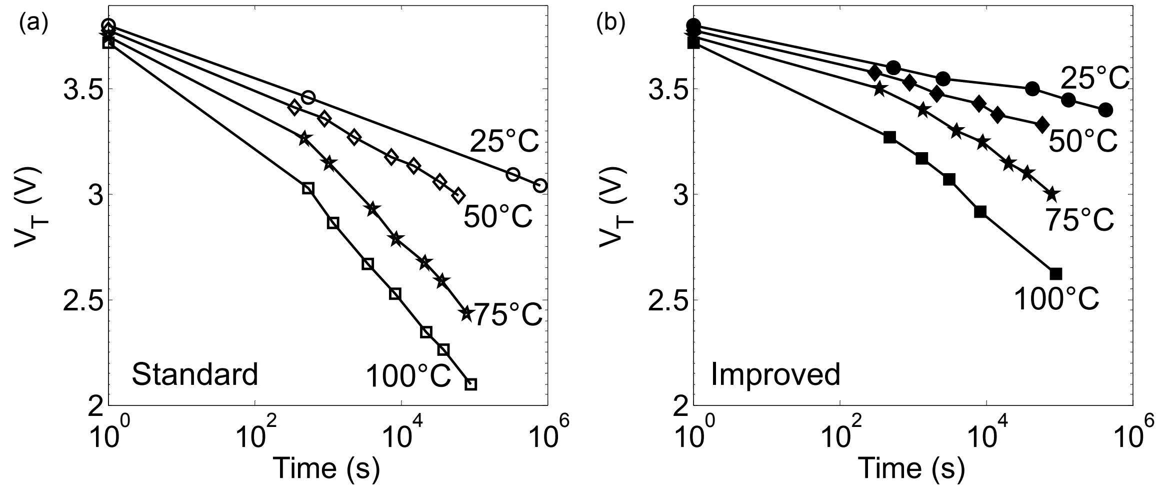


**Figure 5.27. (a) retention characteristics of the standard ST-TFT (b) retention characteristics of the improved ST-TFT.**

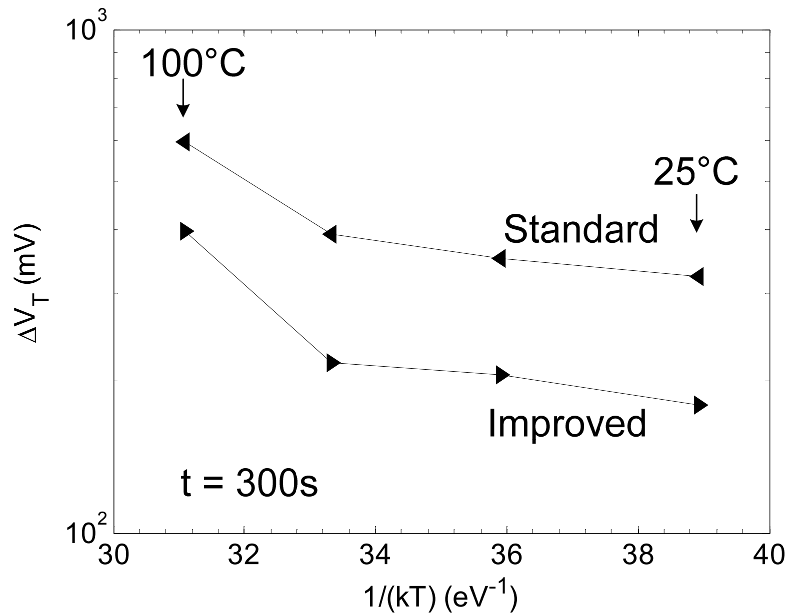


**Figure 5.28. Arrenhius plot of $\Delta V_T$ (t = 300s) as a function of $(kT)^{-1}$ for the ST-TFT with the standard tunnel SiNx and the ST-TFT with the improved tunnel $SiN_x$ from temperatures of 25°C to 100°C.**

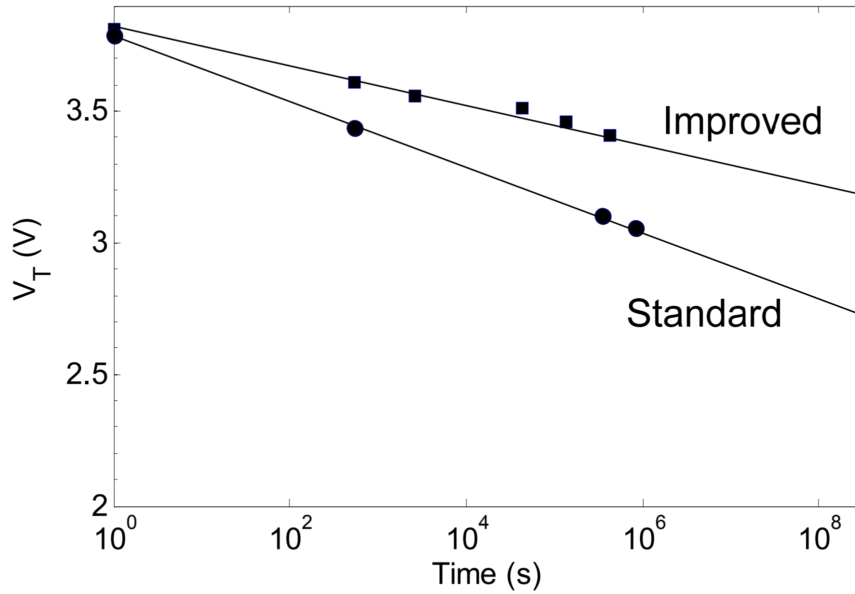


**Figure 5.29. Retention characteristics of the standard and improved ST-TFT at 25°C. Lines represent linear extrapolations to 10 years (the right y-axis of the graph).**

### 5.2.4. Extracting trap density

As can be seen from Figure 5.28, at elevated temperatures (>75°C), the charge loss mechanism is dominated by the strongly temperature-dependent thermal emission process. In this regime, electrons primarily escape by thermally "jumping" from the traps into the conduction band of the $SiN_x$. As such, the rate of $V_T$ decay (or charge loss) at a specific time is strongly correlated to the trap density at a certain energy depth [43]. In the following section, we present a derivation of an analytical expression that relates the rate of $V_t$ decay and storage trap density, under the condition where thermal emission is the dominant detrapping process.

Using the Shockley-Read-Hall theory of recombination, the rate of emission ($R_e$) of electrons from traps in the nitride is equal to the number of occupied electron traps, multiplied by the emission coefficient ($e_n$) [49]. And the number of occupied electron traps is equal to the total number of traps ($N_t$), multiplied by the occupational probability ($f_t$). As such we can write:

$$R_e = e_n N_t f_t \qquad (5.7)$$

Similarly, the rate of electron capture in the traps ($R_c$) is equal to the number of electrons ($n$) in the conduction band of $SiN_x$ multiplied by the number of empty trap states, multiplied by the capture coefficient ($c_n$), which may be written as:

$$R_c = c_n n N_t (1 - f_t) \qquad (5.8)$$

Under equilibrium conditions, we can assume that the capture rate is equal to the emission rate and therefore:

$$c_n n N_t (1 - f_t) = e_n N_t f_t \qquad (5.9)$$

$$e_n = \frac{c_n n (1 - f_t)}{f_t} \qquad (5.10)$$

Furthermore, we can also assume that the occupational probability is described the Fermi-dirac distribution and the concentration of the electrons in the conduction band of $SiN_x$ is given by Boltzmann's approximation, so we can write

$$\frac{(1 - f_t)}{f_t} = e^{\left[-\frac{(E_t - E_f)}{k_B T}\right]} \qquad (5.11)$$

$$n = N_c e^{\left[-\frac{(E_c - E_f)}{k_B T}\right]} \qquad (5.12)$$

Where $E_C$ is the conduction band edge, $E_t$ is the trap energy, $E_f$ is the Fermi level, and $N_c$ is the density of states in the conduction band of the $SiN_x$ given by

$$N_c = 2\left(\frac{2\pi m^* k_B T}{h^2}\right)^{3/2} \qquad (5.13)$$

Where m* is the electron effective mass in the $SiN_x$. The capture probability $C_n$ in eq 5.8 can be expressed as [50]:

$$C_n = \sigma_n V_{th} \qquad (5.14)$$

Where $\sigma_n$ is the capture cross section of the storage trap and $V_{th}$ is the electron thermal velocity given by:

$$V_{th} = \sqrt{\frac{3k_B T}{m^*}} \tag{5.15}$$

Equations 5.10 – 5.15 can be combined to write:

$$e_n = 2\sigma_n \left( \frac{2\pi m^* k_B T}{h^2} \right)^{3/2} \sqrt{\frac{3k_B T}{m^*}} e^{\left[ -\frac{(E_c - E_t)}{k_B T} \right]} \tag{5.16}$$

$$e_n(\phi_t) = AT^2 e^{\left[ -\frac{\phi_t}{k_B T} \right]} \tag{5.17}$$

Where $\varphi_t$ is the storage trap energy respect to the $SiN_x$ conduction band ($E_c - E_t$), and A is all the non-temperature dependent terms in equation 5.16 combined. This equation for the emission constant is derived for the special case of thermal equilibrium, which does not strictly hold for the thermal emission charge loss process in the ST-TFT. However, the equilibrium emission constant is a fairly good approximation for the non-equilibrium constant if the detrapping in ST-TFT is relatively slow and there is negligible trap-to-trap charge transfer, which are reasonable assumptions [48].

Therefore, the emission rate as a function of trap energy and time can be written as:

$$\frac{\delta n_t(\phi_t, t)}{\delta t} = -e_n(\phi_t) n_t(\phi_t, t) \tag{5.18}$$

Where $n_t(\varphi_t, t)$ is the density of trapped electrons at time t (in $cm^{-2}eV^{-1}$). Note that we have ignored the charge capture process, because the density of free electrons in the $SiN_x$ conduction band will be negligibly small and emitted electrons are swept out into the a-Si channel or metal gate by the built-in electric field. This equation has the solution:

$$n_t(\phi_t, t) = n_0(\phi_t) e^{(-e_n(\phi_t)t)} \tag{5.19}$$

Where $n_0(\varphi_t)$ is the initial density of trapped electrons immediately after the programming operation, and therefore it also represents that density of the charge traps responsible for storage. Using this, we can write the threshold voltage shift due to the stored charge at the charge-trapping interface as a function of time:

$$\Delta V_T(t) = \frac{X_{TN}}{\varepsilon_N} \int_{E_G, SiN_x} q n_t(\phi_t, t) d\phi_t = \frac{X_{TN}}{\varepsilon_N} \int_{E_G, SiN_x} q n_0(\phi_t) e^{(-e_n(\phi_t)t)} d\phi_t \quad (5.20)$$

Where $X_{TN}$ and $\varepsilon_N$ are the thickness and relative permittivity of the tunnel $SiN_x$ layer, respectively. Not knowing the functional form of $n_0$, the storage trap distribution in energy, it is not possible evaluate the integral in equation 5.20. However, it is possible to evaluate the rate of threshold voltage shift decay or the derivative of equation 5.20, which is given by:

$$\frac{\delta \Delta V_T(t)}{\delta t} = -\frac{X_{TN}}{\varepsilon_N} \int_{E_G, SiN_x} q n_0(\phi_t) e_n(\phi_t) e^{(-e_n(\phi_t)t)} d\phi_t \quad (5.21)$$

by noting that $e_n(\phi_t)e^{(-e_n(\phi_t)t)}$ is a sharply peaked function of $\phi_t$, with a maximum at

$$\phi_m = k_B T \ln(AT^2 t) \quad (5.22)$$

As such, it may be approximated as a delta function with the pre-multiplier equal to the total area underneath the curve (Figure 5.30). This approximation is tantamount to saying that at any given time t, all the thermal emission of electrons come from traps at a single energy $\varphi_m$. This is qualitatively consistent with the physics of charge detrapping via thermal emission. Electrons stored in the shallow traps escape faster than those stored in deep traps. At time t, most of the electrons in traps shallower than $\varphi_m$ have already escaped and the most the electrons in traps deeper than $\varphi_m$ are still trapped, and a majority of the thermal emission is coming from traps at $\varphi_m$.

To calculate the pre-multiplier for the delta function, we evaluate the following integral:

$$\int_{E_G, SiN_x} e_n(\phi_t) e^{(-e_n(\phi_t)t)} d\phi_t = \int_0^{E_G, SiN_x} AT^2 e^{\left[-\frac{\phi_t}{k_B T}\right]} e^{\left(-AT^2 e^{\left[-\frac{\phi_t}{k_B T}\right]} t\right)} d\phi$$

Let u = $e^{\left[-\frac{\phi_t}{k_B T}\right]}$ and a = $AT^2$, then we have

$$\int_{E_G, SiN_x} e_n(\phi_t) e^{(-e_n(\phi_t)t)} d\phi_t \approx -k_B T \int_1^0 a e^{(-aut)} du$$

$$= k_B T \left. \frac{e^{(-aut)}}{t} \right|_1^0$$

$$= \frac{k_B T}{t}(1 - e^{(-at)}) \approx \frac{k_B T}{t}$$

The last approximation holds for t >> $(AT^2)^{-1}$, which is satisfied for the time range of interest because $AT^2$ is approximately $10^{13}s^{-1}$, assuming $\sigma_n = 5x10^{-13}cm^2$ and $m^* = 0.5m_0$ [43]. Therefore:

$$e_n(\phi_t) e^{(-e_n(\phi_t)t)} \approx \frac{k_B T}{t} \delta(\phi_t - \phi_m) \qquad (5.23)$$

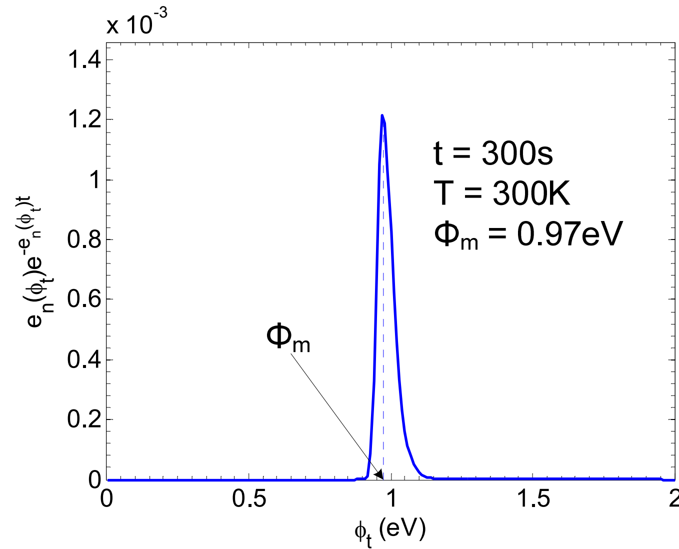


**Figure 5.30 The energy dependence of the function** $e_n(\phi_t) e^{(-e_n(\phi_t)t)}$

Substituting equation 5.23 into equation 5.21, we get

$$\frac{\delta \Delta V_T(t)}{\delta t} = -q \frac{X_{TN}}{\varepsilon_N} \int_{E_G, SiN_x} n_0(\phi_t) \frac{k_B T}{t} \delta(\phi_t - \phi_m) d\phi_t$$

$$= -q \frac{X_{TN}}{\varepsilon_N} \frac{k_B T}{t} n_0(\phi_m) \qquad (5.24)$$

Applying the identity $\frac{\delta}{\delta \log t} = 2.3t\frac{\delta}{\delta t}$, we get

$$\frac{\delta \Delta V_T}{\delta \log t} = -2.3q\frac{X_{TN}}{\varepsilon_N}k_B T n_0(\phi_m) \tag{5.25}$$

Using equation 5.25 and the retention characteristics of the improved ST-TFT non-volatile storage device measured at 100°C (Figure 5.31 inset), where thermal emission has been shown to be the dominant detrapping mechanism, we can calculate the storage trap distribution (Figure 5.31). Using this approach, we extracted a trap distribution that peaks around 1.3eV below the conduction band with a value of $2\times10^{12}$ $cm^{-2}eV^{-1}$. The density near $\phi_T$ = 1.1eV is extracted from $V_T$ decay curve at $10^0$ – $10^1$s, and the density near $\phi_T$ = 1.4eV is extracted from $V_T$ decay curve at $10^6$s, at 100°C. Previous studies of nitride defects responsible for charge storage in SONOS memory found similar density (~$1\times10^{12}$ $cm^{-2}eV^{-1}$), but shallower trap energy (1.1eV) [43]. This suggests that the plasma-induced defects are better storage traps.

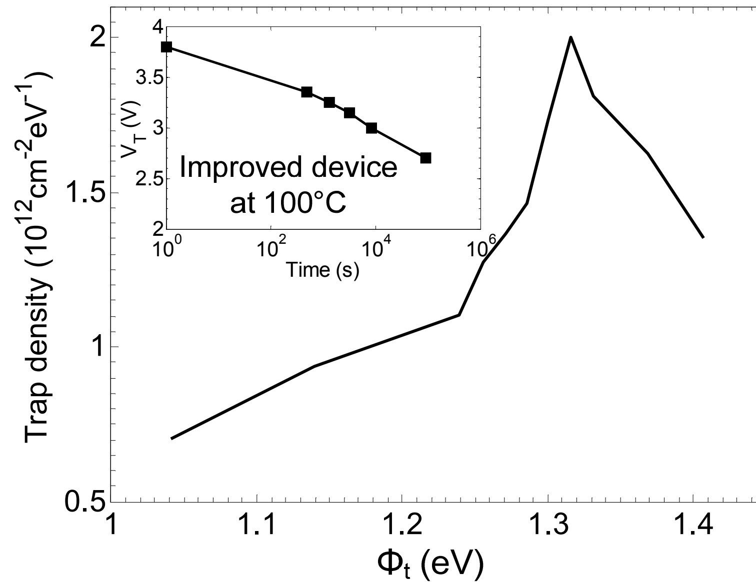


**Figure 5.31. Trap density as a function of energy at the charge trapping interface. Inset: Retention characteristic of the improved ST-TFT at 100°C used to extract the trap density. Energies are the differences between the trap energy and $E_C$ of the $SiN_x$.**

As noted earlier, we have assumed that at any given time, only traps at a single energy level are responsible for emission. As such, the time axis in the threshold voltage decay curves

can be mapped to the trap energy axis. For data at different temperatures, the same time translates to different trap energies (by equation 5.22), with time in higher temperature data equaling to deeper trap energies. This is why retention curves (of $V_T$ vs time) have different shapes at different temperatures. However, if the retention data were plotted as a function of trap energy, instead of time, then they should be identical. However, this would only be true if thermal emission were the dominant process responsible for retention loss in retention data at all temperatures, because the time-trap energy analog is derived from the thermal emission analysis, assuming trap-assisted tunneling was not important. To test this hypothesis, we re-plot the retention data, measured from the improved ST-TFT at various different temperatures, as a function of trap energy (Figure 5.32). The 75°C and 100°C curves are nearly identical, while the 25°C and 50°C curves are quite different from the other two and from each other. This is consistent with our initial hypothesis that trap-assisted tunneling is the dominant mechanism for charge loss at lower temperatures (<75°C), and thermal emission only becomes dominant at temperatures >75°C. Because the threshold voltage decay in the 25°C and 50°C data are due to a combination of the trap-assisted tunneling and thermal emission, it is expected that these curves would incorrectly over-estimate the threshold voltage decay associated with shallower trap energies.

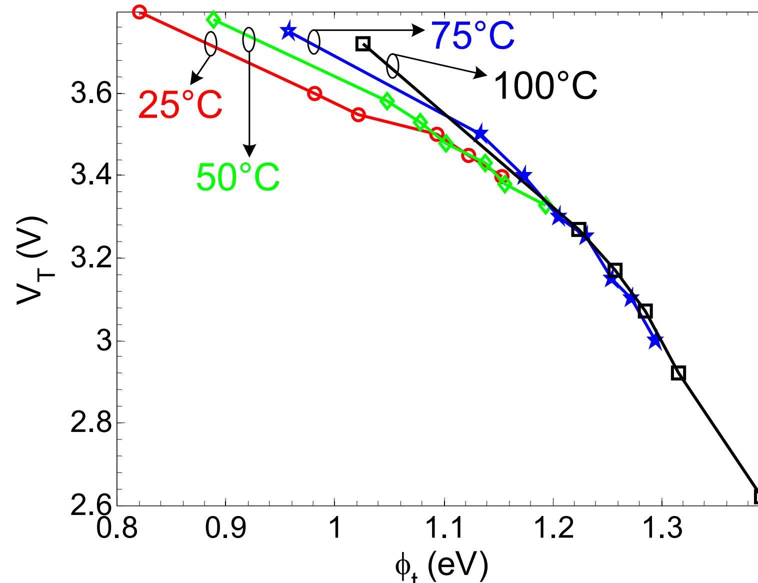


**Figure 5.32. Retention data of the improved ST-TFT re-plotted as a function of trap energy.**

### 5.3. Summary

Integration of non-volatile memory into existing large-area electronics devices, such as displays and medical imaging arrays, has the potential to great improve their functionality and enable new applications. Existing non-volatile memory technologies, including charge trapping memory, ferroelectric memory, phase change memory and magnetoresistive memory, are unsuitable for large area fabrication. These devices would have to be added as an external component, which would incur significant additional integration cost. An a-Si TFT based non-volatile memory can be a much better alternative, because it can be designed to be compatible with existing a-Si TFT fabrication process. Therefore, it may be easily integrated into large area electronics with little incremental cost.

The initial demonstration of the a-Si floating gate TFT memory, inspired by the c-Si counterpart, suffered from two major drawbacks, which are drain-voltage-dependent device saturation current and short retention time. The drain-voltage-dependence is caused by the parasitic capacitive coupling between the drain electrode and the floating gate electrode, and it is undesirable because many applications, such as AMOLED displays, require the TFT saturation current to be exclusively controlled by the gate voltage and not be affected by the drain voltage. We demonstrated a novel ST-TFT structure that eliminated the drain-voltage-dependence by replacing the floating gate with a layer of plasma-induced defects, as the charge trapping medium. The FG-TFT had poor retention performance because electrons stored in the floating gate are free to move around, and as such they can move to “weak” spots in the tunnel $SiN_x$ where it is easier to escape, resulting in the fast detrapping rate. The ST-TFT also offered improved retention performance, because in the ST-TFT the injected electrons are stored in localized traps instead of the conductive floating gate. However, the retention time in the ST-TFT is still relatively short. We have identified the key mechanism which limited the room temperature retention performance of the ST-TFT to be trap assisted tunneling leakage by studying the temperature dependence of the retention characteristics of the ST-TFT. We reduced this trap-assisted

tunneling leakage by reducing the defect density in our tunnel $SiN_x$ film. Low defect density in the tunnel $SiN_x$ film was achieved by using specific PECVD growth conditions that promoted more energetically favorable bond configurations, namely high $NH_3/SiH_4$ flow ratio and $H_2$ dilution. The optimized ST-TFT retains 75% of the initial injected charge after 10 years of room-temperature storage. Finally, we extracted the density distribution in energy of the plasma induced traps responsible for charge storage, by deriving an analytical expression that related the trap density to the thermal emission detrapping rate. We believe we have established a basic understanding of the physical mechanisms that govern the characteristics of the ST-TFT, laying ground work for further improvement and integration into more advanced systems.

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# Novel AMOLED display architecture enabled by the ST-TFT

In this chapter, a brief overview of the conventional AMOLED display technology and its shortcomings are presented. Then, a novel AMOLED display architecture, enabled by the non-volatile memory device ST-TFT (discussed in Chapter 5), that overcomes the disadvantages of the conventional approach is proposed. The new approach allows the display refresh step to be omitted when data is stable, potentially saving power. Finally, the implementation of the novel AMOLED pixel architecture is described and characterized. The work presented in this chapter was described in references [1] and [2].

## 6.1. Conventional AMOLED technology

The active matrix organic light emitted diode (AMOLED) display has many advantages over the conventional active matrix liquid crystal display (AMLCD), such as wider viewing angle, faster response time, lower power consumption [3][4], better contrast ratio, and simpler structure (Figure 6.1). When OLEDs were first invented, they had relatively poor efficiency [5]. The requirement of high drive current necessitated the use of polysilicon TFTs, which is a relatively expensive technology [6][7]. However, with the development of the more efficient phosphorescent OLED [8], as well as other advances, the requirement on drive current has been significantly relaxed. As a result, a-Si TFTs have become a suitable alternative for the OLED driver [9][10]. Integrating OLEDs with a-Si TFT backplanes is particularly attractive, because a-Si based AMOLED could potentially be produced at much lower cost over large-area using existing infrastructures and processes in the AMLCD industry. Furthermore, a-Si AMOLED would also be compatible with flexible substrates, which is required for the low-cost and high throughput roll-to-roll processes.

The conventional AMOLED pixel (Figure 6.2(a)) has two TFTs, a storage capacitor, and an OLED. The TFTs, interconnect lines and storage capacitors are the circuitry which drive the OLED, and are referred to as the “backplane” of the display. The OLED is the light emitting

element, and is the “frontplane” of the display. The fraction of the pixel area that emits light (the area marked ITO in Figure 6.2(b) divided by the total pixel area) is called the pixel fill factor. Ideally, the pixel fill factor should be as close to 1 as possible, but it is limited by the portion of the pixel area that is occupied by the backplane circuitry, which does not emit light.

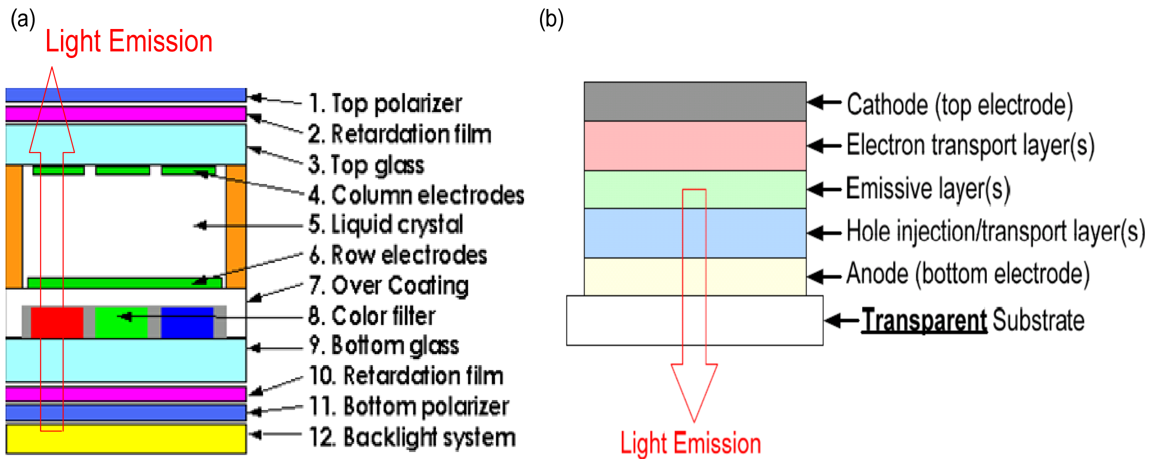


**Figure 6.1. (a) Structure of a LCD pixel element [11]. (b) Structure of an OLED [12].**

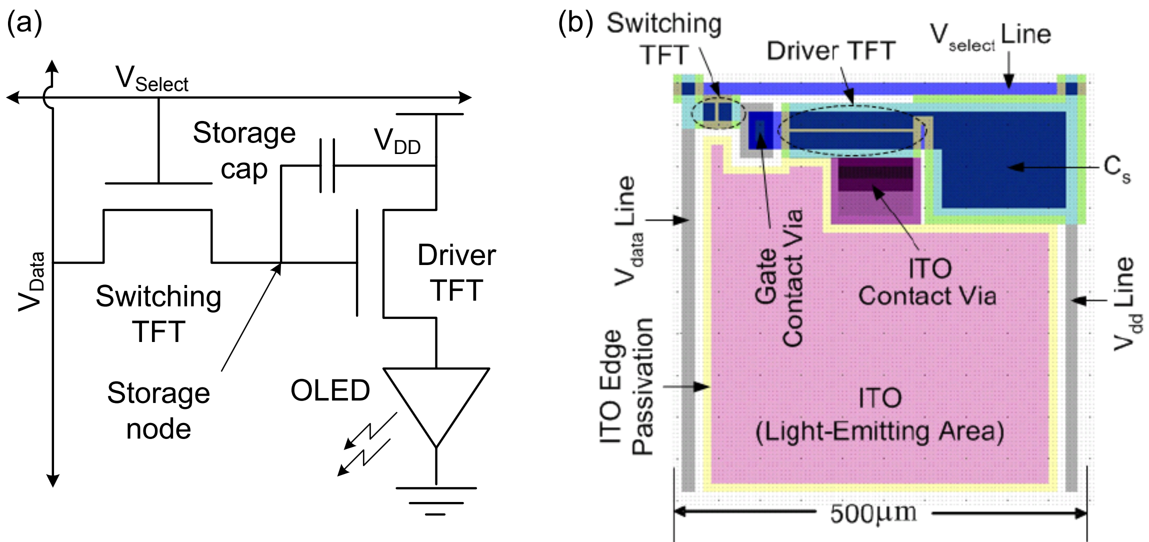


**Figure 6.2. (a) the conventional 2-TFT AMOLED pixel with the storage capacitor used to hold the voltage on the gate electrode of the driver TFT between pixel refreshes. (b) the design layout of the same 2-TFT AMOLED pixel shown in (a).**

During display operation, the select line ($V_{Select}$) is pulled high, turning on the switching TFT to allow the voltage on the data line ($V_{Data}$) to propagate to the storage node. This charges

up the storage capacitor and sets up the voltage on gate electrode of the driver TFT. The driver TFT converts $V_{Data}$ into electrical current and drives it through the OLED, which converts the current into light. The ideal pixel operation can be described by the following equations:

$$I_{TFT,driver} = \frac{1}{2}\mu C_{SiN_x}\left(\frac{W}{L}\right)_{driver}\left(V_{GS,driver} - V_{T,driver}\right)^2 \quad (6.1)$$

$$I_{OLED} = I_o\left(e^{\frac{qV_{OLED}}{nkT}} - 1\right) \quad (6.2)$$

$$V_{Data} = V_{GS,driver} + V_{OLED} \quad (6.3)$$

$$I_{TFT,driver} = I_{OLED} = I_{pixel} \quad (6.4)$$

$$Pixel\,brightness = I_{pixel} \times \eta_{OLED} \quad (6.5)$$

where $\mu$ is the field effective mobility of the TFT, $C_{SiNx}$ is the gate $SiN_x$ capacitance, W/L is the aspect ratio and the subscript "*driver*" refers to the driver TFT. $I_o$ is the pre-exponential constant of the current of the OLED and n is the ideality factor of the OLED. $\eta_{OLED}$ is the conversion efficiency of the OLED in Cd/A.

After the brightness of the given pixel has been set via the process described above, the select line is pulled low and the storage node is isolated from the voltages on the data line. This allows the brightness setting process to be repeated for the other rows in the display without disturbing the one that has already been set. The storage capacitor holds the voltage on the storage node and keeps pixel brightness unchanged while the brightness on the other pixels are being set. However, voltage on the storage node, the OLED current and the pixel brightness, will all decay due to off-current leakage in the switching TFT and the gate leakage current in the driver TFT and storage capacitor. In order to maintain the image on the display, the storage capacitor must be periodically recharged to ensure to that no perceivable changes to pixel brightness occur (Figure 6.3). The power consumed by these extra refresh cycles may be conserved if the pixel were designed to store the brightness information in a non-volatile fashion. This could potentially result in significant power savings in low-frame-rate or static display applications.

The AMOLED pixel is typically designed to show less than 0.1% change in pixel brightness between refreshes [12]. The 0.1% change in brightness is equivalent to a 0.1% change driver TFT current by equation 6.5, and that change in current can be translated to a change in the gate-source voltage by:

$$\frac{0.1\% I_{TFT}}{I_{TFT}} = \left[1 - \frac{\Delta V_{GS}}{(V_{GS} - V_T)}\right]^2 \qquad (6.6)$$

Where $\Delta V_{GS}$ is the change in gate-source voltage corresponding to a 0.1% change in TFT current and $V_{GS}$ and $I_{TFT}$ are the gate voltage and pixel current corresponding to the set pixel brightness.

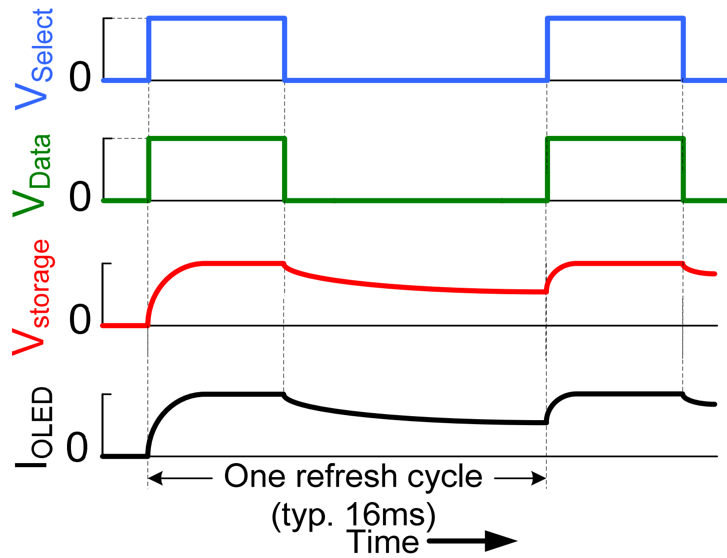


**Figure 6.3. Timing diagram of a conventional 2-TFT AMOLED pixel. Frame time is one refresh cycle, which is typically 16ms.**

Given that the pixels are typically refreshed at 60Hz, the storage capacitor must hold the voltage within tolerable limits for approximately 16ms. Using these constraints, the area of the capacitance required can be calculated as follows:

$$A_{cap} = \frac{T_{SiNx}}{\varepsilon_{SiNx}} \frac{I_{leak} \times 16ms}{\Delta V_{GS}} \qquad (6.7)$$

Assuming standard amorphous silicon TFT parameters, a pixel area of 500μm x 500μm, an OLED efficiency of 57Cd/A, an $I_{leak}$ of $10^{-12}$A, a desired pixel brightness of 1000Cd/m$^2$ and combining equations 6.1 through 6.6 [12], we calculate required storage capacitor needs to be

~$2.41 \times 10^4 \mu m^2$. This is approximately 10% of the pixel area. The specific number may vary based on assumptions, but the fact that storage capacitor can occupy significant portions of the light emitting area in a pixel is quite general. If the pixel were designed to not require the storage capacitor, then the pixel fill factor can be improved significantly. Furthermore, this becomes increasingly critical as pixel densities increase and pixel area decrease, because the area of the storage capacitor is not expected to scale proportionally due to fabrication alignment issues and parasitic effects [13]. As such, the storage capacitor will occupy an increasing percentage of the pixel area and become a major limiting factor for pixel fill factor.

## 6.2. Novel AMOLED display architecture

The conventional AMOLED pixel employs a storage capacitor to hold $V_{Data}$ in between pixel refreshes. This results in a limitation on the pixel fill factor and the requirement of refresh cycles to simply maintain a static image. As alluded to earlier, these issues can be resolved if the pixel brightness information were stored in a non-volatile fashion and not on a capacitor which loses charge quickly. This can be achieved if we take advantage of the non-volatile storage capability of the ST-TFT described in Chapter 5.

### 6.2.1. Theory of operation

Threshold voltage of the ST-TFT can tune up or down over a continuum of values by applying the corresponding programming or erasing voltage pulses (Figure 5.23). This property can be exploited to control pixel drive current, without a storage capacitor. In the proposed pixel structure (Figure 6.4), the ST-TFT is integrated as the driver TFT and the storage capacitor is eliminated. In the new circuit with the ST-TFT driver, the OLED brightness is not controlled by varying the $V_{DATA}$ applied to the gate of the driver ST-TFT through the switching TFT, as in the conventional AMOLED pixel (Figure 6.5(a)). Instead, a constant $V_{DATA}$ is applied to the gate of the driver ST-TFT. The current through the driver ST-TFT and the OLED brightness is controlled by changing the $V_T$ of the ST-TFT through programming (Figure 6.5(b)). If low brightness is desired, the ST-TFT is set to a high $V_T$ by programming with a large positive gate pulse. If high brightness

is desired, the ST-TFT is set to a low $V_T$ by programming with a small positive gate pulse, or not programming at all and leaving it with the initial $V_T$. Note this is analog storage, not digital as in flash memory.

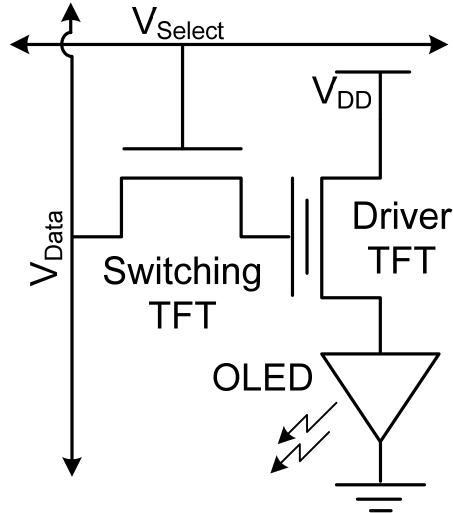


**Figure 6.4 Novel AMOLED pixel structure with integrated ST-TFT driver**

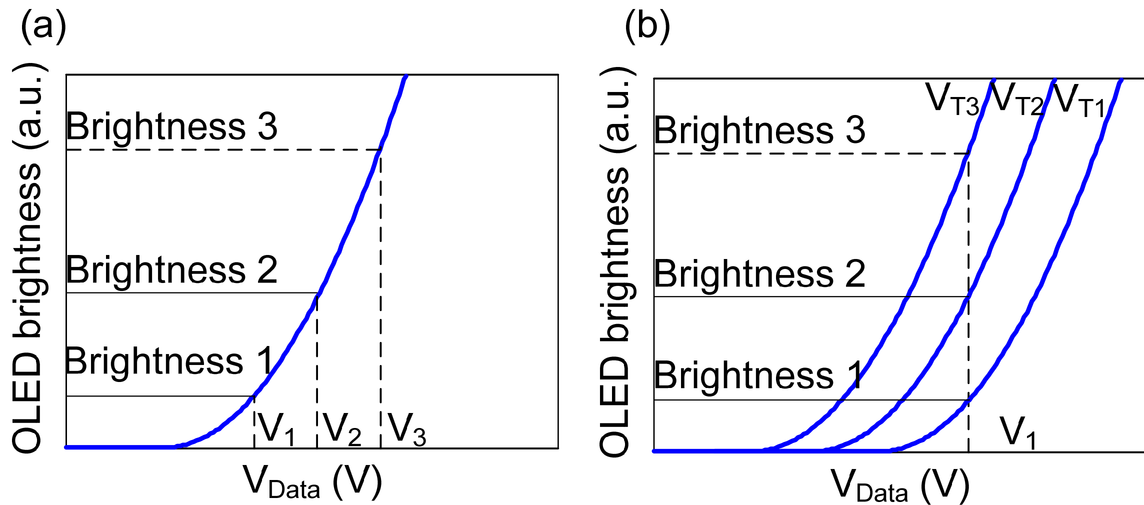


**Figure 6.5. (a) pixel brightness control scheme in conventional 2-TFT AMOLED pixel. (b) pixel brightness control scheme in novel AMOLED pixel with integrated ST-TFT driver. In the latter, a single $V_{DATA}$ is used and the brightness depends on the $V_T$ of the TFT.**

A pixel in this display is programmed by applying a high magnitude (e.g. 35V) and short duration (e.g. 10ms) voltage pulse to the corresponding data line (program mode in Figure 6.6). The same voltage pulse (plus ~2V to account for threshold voltage of the switching TFT) is

applied to the corresponding select line to allow the $V_{DATA}$ pulse to propagate to the gate of the desired driver ST-TFT. All other select lines are held at ground to prevent the $V_{DATA}$ pulse from programming other undesired pixels. $V_{DD}$ is held at ground during programming to ensure both the source and the drain of the ST-TFT are at 0V. This process is repeated until all pixels in the display have been programmed to threshold voltages corresponding to their respective brightness values.

After programming, the display is activated by setting $V_{DD}$ to 10V (display mode in Figure 6.6), $V_{DATA}$ to 8V on all the data lines, and $V_{SELECT}$ to 10V on all the select lines. The OLED current and therefore brightness of any given pixel is determined by the programmed $V_T$ of the driver ST-TFT. High $V_T$ translates into a small OLED current and a dim pixel, and a low $V_T$ translates into large OLED current and a bright pixel. It is important to note that both $V_{DATA}$ and $V_{SELECT}$ are constant DC voltages in the display mode, as a pixel refresh is not necessary to maintain a static image. The pixel brightness values remain stored in the ST-TFT threshold voltage even if the power is turned off.

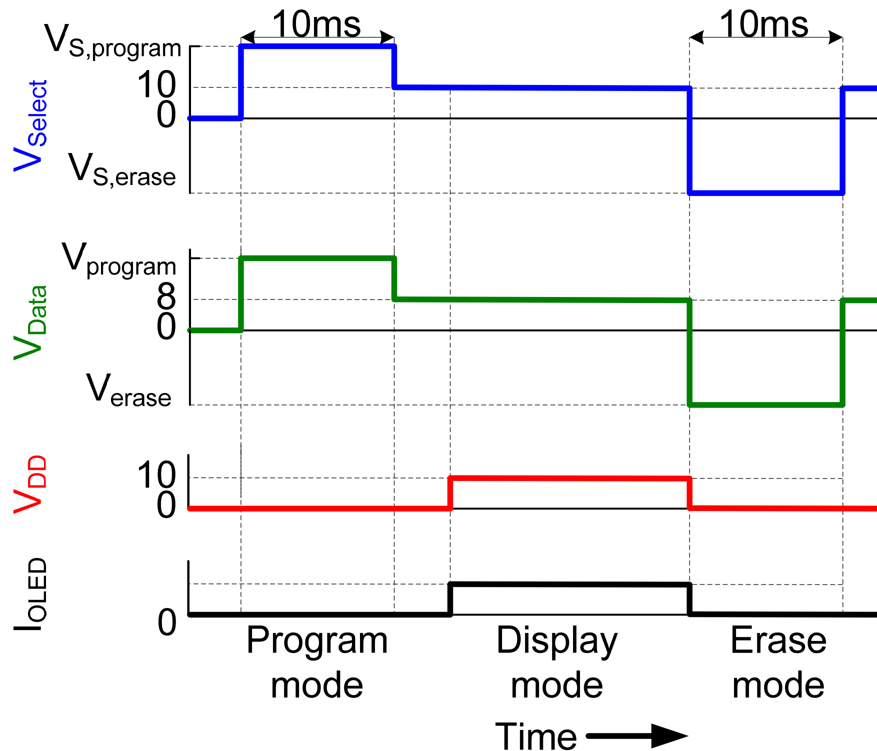


**Figure 6.6. Timing diagram showing the modes of operation in the new pixel in Figure 6.4.**

To change the programmed image, the pixels are first erased and then programmed again. Erase mode, shown in Figure 6.6, is identical to the program operation. The only difference is that the applied voltage pulse has a large negative magnitude, instead of a positive one. This negative voltage forces the trapped electrons in the ST-TFT to tunnel back out, causing $V_T$ to shift towards its initial unprogrammed value. Note that to erase a single pixel in the active matrix (instead of an entire column), all other select lines would have to be held at -30V to prevent the erase pulse from propagating to the undesired pixel drivers.

The proposed pixel structure effectively eliminates the need for a storage capacitor and power-consuming refresh cycles, by storing the pixel brightness information in the tunable threshold voltage of the ST-TFT. This improves both the power consumption of the display and the fill factor of the pixel, while also creating the additional capability to store programmed images without power.

### 6.2.2.Fabrication

The AMOLED backplane was fabricated using the ST-TFT process that is described in Chapter 5. After the completion of the backplane, which consists of the TFTs and the interconnect lines, the sample was encapsulated with a 300-nm-thick $SiN_x$ layer deposited via PECVD. This layer serves as insulation between the backplane and the OLEDs. Via holes were etched into the passivation $SiN_x$ using reactive ion etching (RIE) to allow contact between the source of the driver TFT and Indium Tin Oxide (ITO), which is the anode of the OLEDs. A 250nm-thick ITO layer was deposited via RF sputtering with a gas mixture of $Ar/O_2$ (99%/1%) at room temperature. The ITO layer was patterned via wet etching with aqua regia ($HNO_3/HCl/H_2O$ 1:5:6). A 1.4µm-thick photo-patternable planarization resist was spin-coated over the entire sample, and patterned to reveal the flat portions of the ITO anodes. The planarization resist is reflowed at 180°C to provide smooth edges that cover the rough features (steps) of the circuits and interconnect below. This improved the yield of the OLEDs by reducing the chance of short circuit faults. The sample was exposed to UV-ozone for about 5min, to increase the surface work function of the ITO anode and improve hole injection efficiency [14]. Organic multilayer of of *N,N'*-diphenyl-*N,N'*-bis(3-

methylphenyl) -1,1′-biphenyl-4,4′-diamine (TPD) / aluminum tris(8-hydroxyquinoline) (Alq3) were deposited via thermal evaporation to form green luminescent diodes [15]. The thicknesses of both layers were ~30nm. A bilayer of Mg/Ag (20nm/100nm) was evaporated via thermal evaporation to form the cathode of the OLEDs.

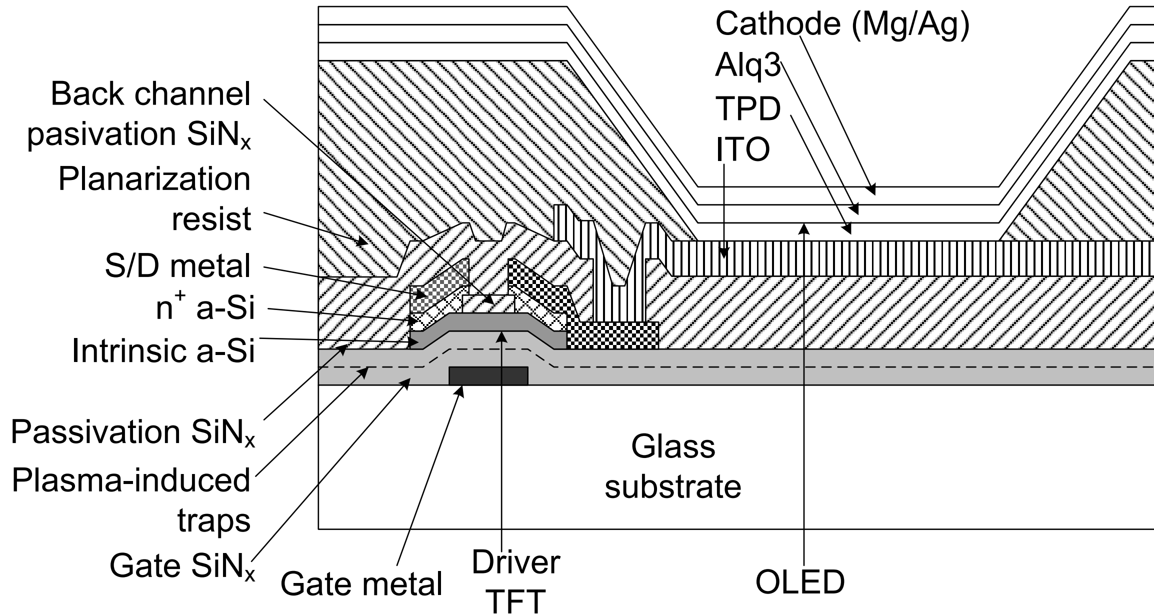


**Figure 6.7 Cross sectional structure of AMOLED pixel with integrated ST-TFT**

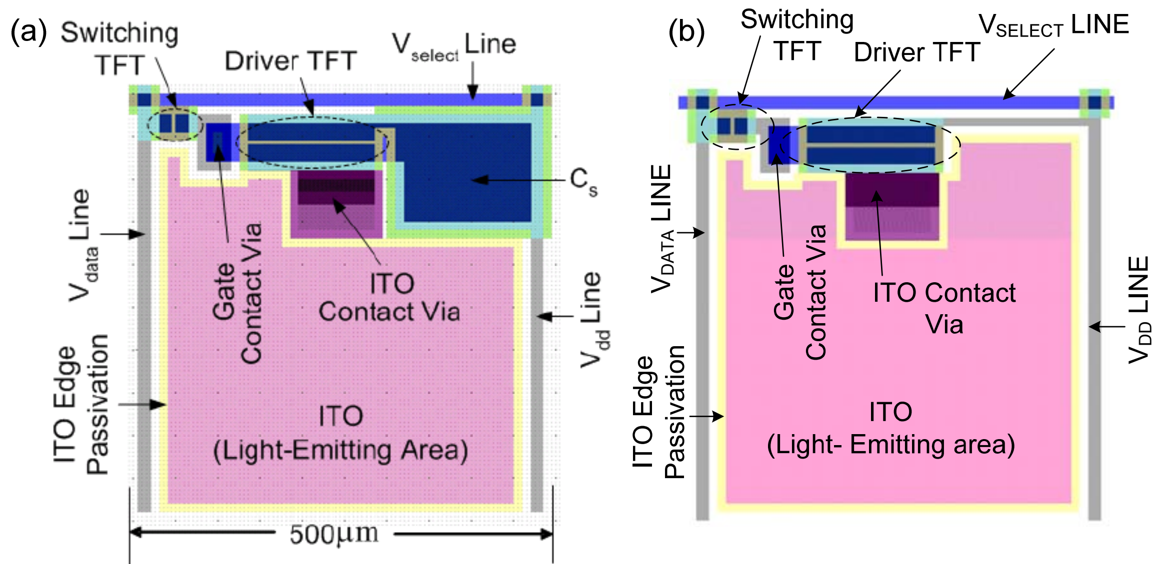


**Figure 6.8. (a) The conventional 2-TFT AMOLED pixel. (b) The novel AMOLED pixel with integrated ST-TFT drive and no storage capacitor.**

The cross section of the completed pixel is shown in Figure 6.7, and comparison between the conventional pixel layout and the novel pixel layout is shown in Figure 6.8. The pixel area is 500μm x 500μm. The switching TFT is 5μm/5μm and the driver TFT is 150μm/15μm. With a design rule of 10μm, the fill factor is 81%, a 15% improvement over the 66% fill factor of a conventional pixel fabricated with the same design rule and TFT dimensions.

### 6.2.3. Device performance

The pixel current-voltage characteristics were first measured prior to OLED integration by applying $V_{DD}$ of 10V, $V_{SELECT}$ of 10V, grounding the source of the driver ST-TFT (OLED anode) and sweeping $V_{DATA}$ from 0V to 8V in 50mV increments. $V_{DATA}$ should be fully transferred to the gate voltage of the ST-TFT for slow scans. With an initial TFT threshold voltage of ~ 1.5V, the TFT's are in saturation mode before programming. The curve marked "before program" in Figure 6.9 is the pixel current vs. $V_{DATA}$ characteristic of the as-fabricated pixel, and the one marked "after program at 35V" is the pixel characteristic after a 10ms, 35V programming pulse (with $V_{SELECT}$ = 37V) has been applied to the data lines with $V_{DD}$ grounded. A clear $V_T$ shift of ~2V is observed. Consequently, under the same bias conditions, the programmed pixel would provide less drive current than the unprogrammed pixel, resulting in a dimmer OLED. The curve marked as "after erase" is the pixel characteristic after the programmed pixel has been erased with 10ms, -28.5V voltage pulse on $V_{DATA}$ ($V_{SELECT}$ = -26.5). It can be seen that the programming-induced $V_T$ shift can be reversed via the erase operation and the pixel characteristics returned that of the unprogrammed state.

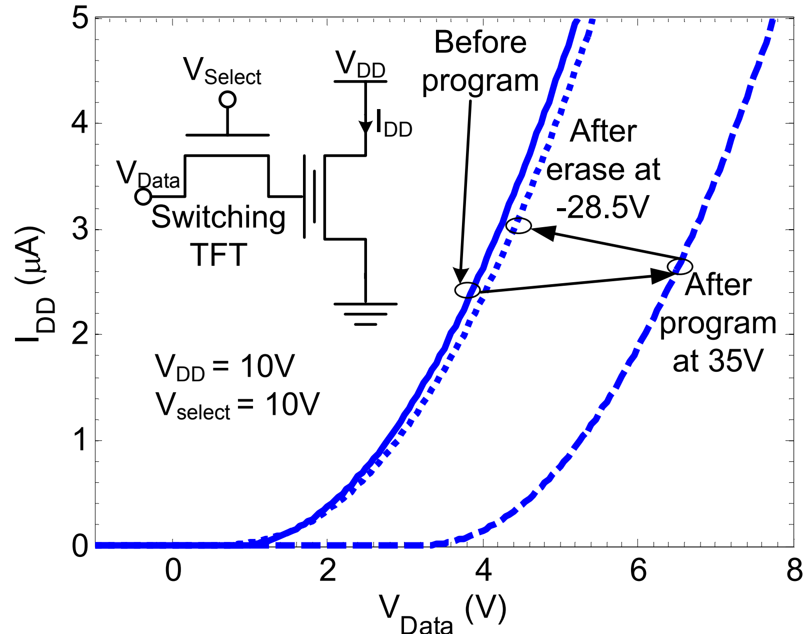


**Figure 6.9 Single-pixel current vs. $V_{DATA}$ characteristics before OLED integration. The aspect ratios of the driver TFT and switching TFT are 10 and 1, respectively. The curves are shown for pixel before programming, after programming at 35V ($V_{SELECT}$ = 37V) for 10ms, and after erasing at -28.5V ($V_{SELECT}$ = -26.5V) for 10ms.**

After OLED integration, the pixel programming functionality was tested by applying programming pulses to the $V_{DATA}$ and $V_{SELECT}$ terminals of the individual pixel (Figure 6.10). The programming pulses were 10ms long with peak voltages ranging from 20V to 35V for $V_{DATA}$ and 22V to 37V for $V_{SELECT}$. $V_{DD}$ and the cathode of the OLED were grounded during programming. After programming, individual pixels were driven with DC $V_{DATA}$ = 8V, $V_{DD}$ = 10V and $V_{SELECT}$ = 10V, and the pixel brightnesses were measured as a function of the programming voltage.

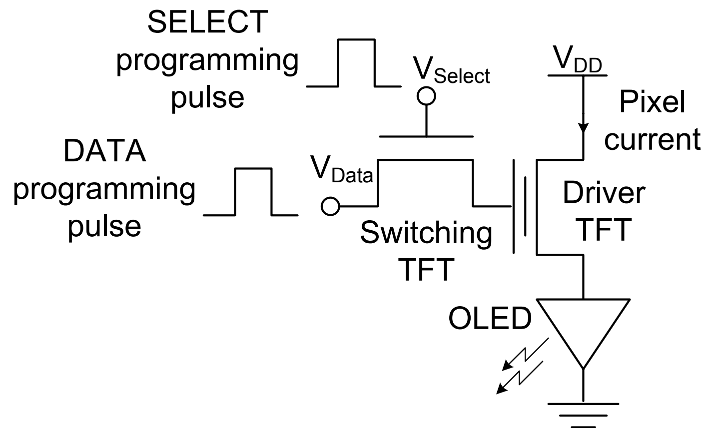


**Figure 6.10. Programming scheme of the individual pixels with integrated OLED.**

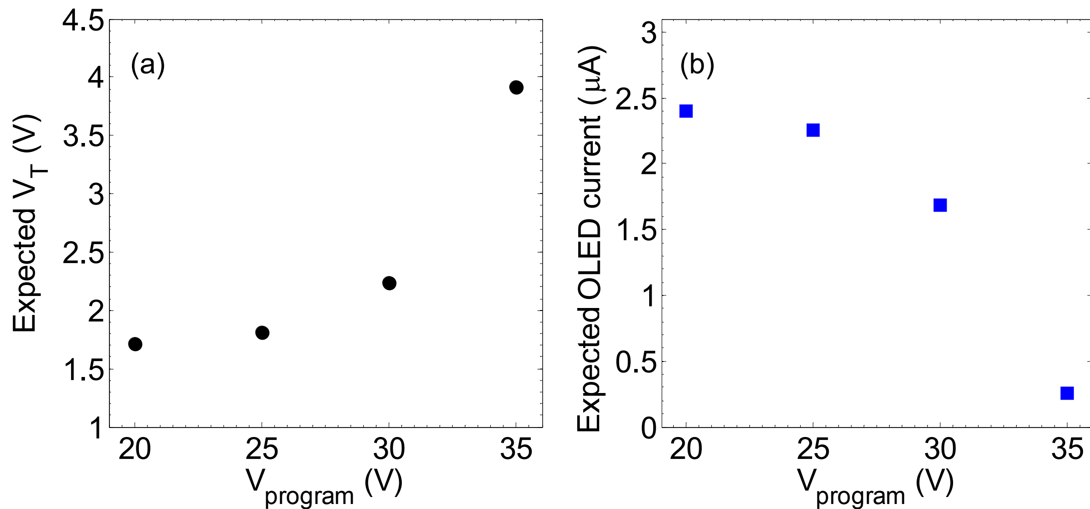


**Figure 6.11. Expected threshold voltage of the driver ST-TFT and expected OLED current in the test pixel as function of programming voltage. For $V_{DATA}$ = 8V and assumed $V_{OLED}$ = 3V.**

Based on the programming characteristics of the ST-TFT shown in Figure 5.23a, the threshold voltage of the driver TFT is expected to increase with increasing program voltage as shown in Figure 6.11a. As the threshold voltage of the driver ST-TFT increases, the magnitude of $V_{GS}$-$V_T$ for the driver ST-TFT also decreases, leading to a drop in OLED current and therefore brightness. Using a simplifying approximation of a fixed OLED voltage of 3V, the expected OLED current as function of program voltage is calculated and shown in Figure 6.11b.

Figure 6.12 shows the pixel brightness in an isolated test pixel as a function of programming voltage, after OLED integration with the cathode grounded. The measured pixel brightness decrease with increasing magnitude of the programming voltage pulse, with the pixel turned completely off for a programming voltage of 37 V. The trend is in agreement with the expectations of increasing threshold voltage shift of the driver ST-TFT is and decreasing OLED current with increasing programming voltages.

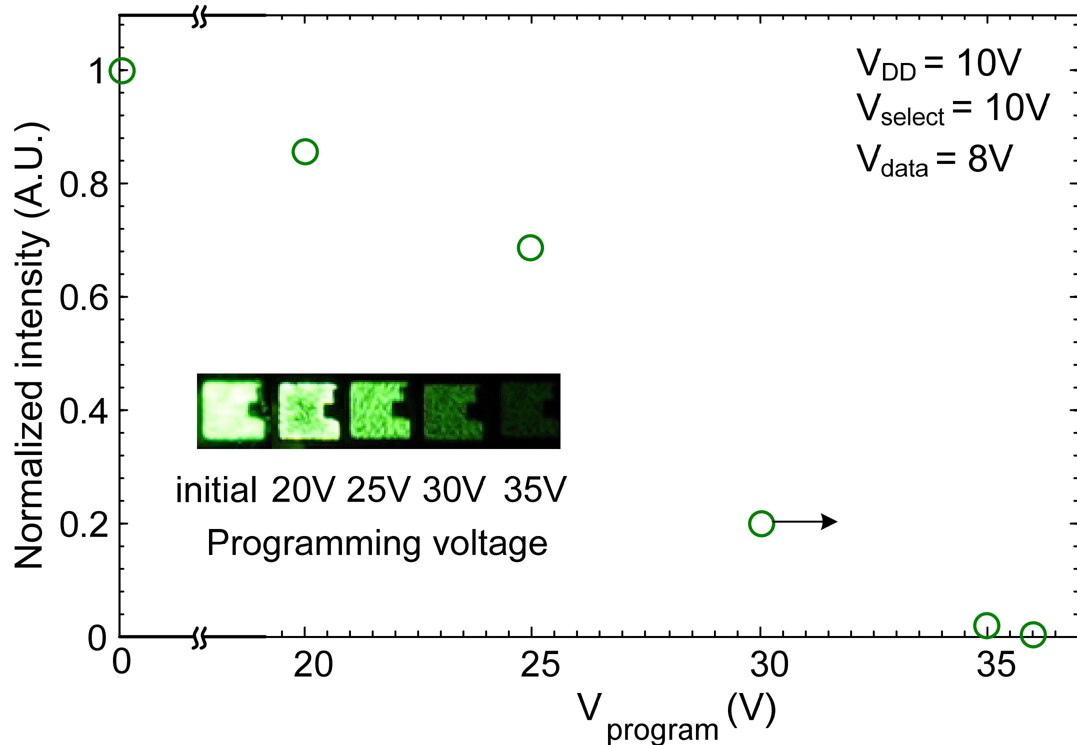


**Figure 6.12. Single pixel brightness as a function of programming voltage, after OLED integration. The inset shows photographs of five individual pixels, corresponding in order to the programming conditions of 0, 20, 25, 30, and 35V. Pixel brightness measured while pixels were driven with DC $V_{DATA}$ = 8V, $V_{DD}$ = 10V and $V_{SELECT}$ = 10V.**

Figure 6.13 shows the photograph of an integrated 10x10 AMOLED display. All the even data lines (columns) are tied together, and all the odd data lines are tied together for simplified testing. The select lines (rows) can be accessed individually. The odd columns were programmed by applying programming voltage pulses to the odd data lines, and no programming was done on the even columns. Programming was performed one row at a time, by activating the row select lines with the appropriate voltage pulse. Because the odd column data lines were tied together, all the odd-column pixels in a given row are programmed to the same intensity.

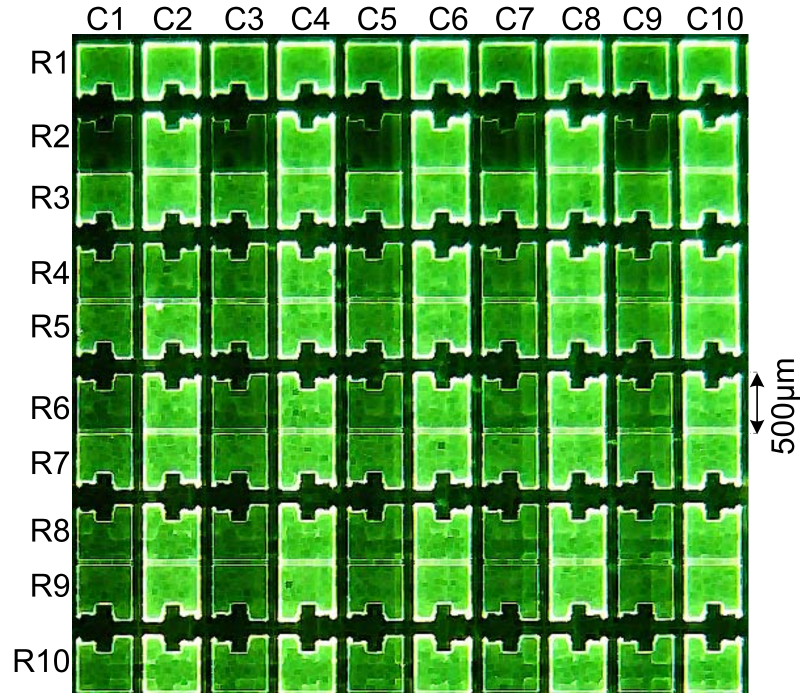


**Figure 6.13 Photograph of an integrated 10x10 AMOLED display. The even columns (C2, C4, C6, C8, and C10) have not been programmed and remain at full brightness. The odd columns (C1, C3, C5, C7, and C9) are tied together and have been programmed to four different intensity levels, with programming voltages of 20V (R1, R3 and R10), 24V (R5 and R7), 28V (R4, R6, R8 and R9), and 32V (R2).**

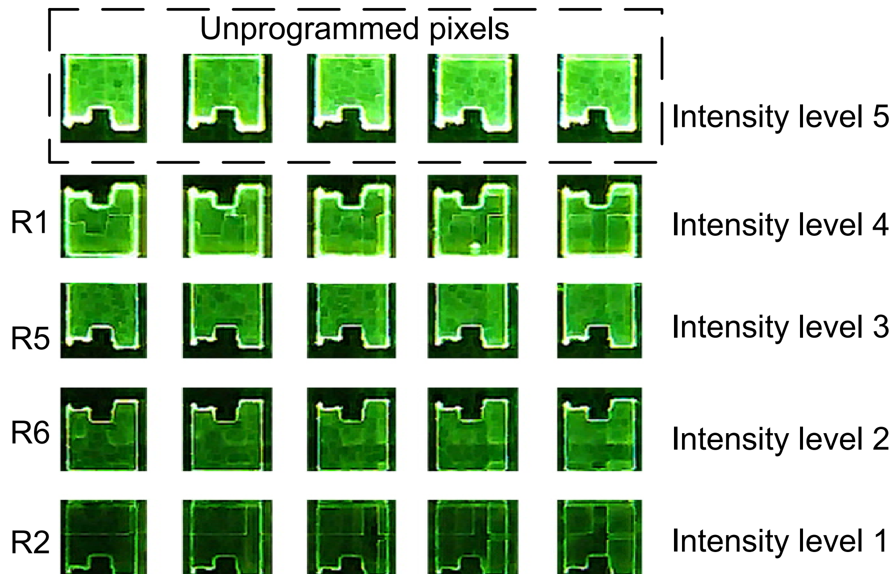


**Figure 6.14 Representative pixels from each of the four different programmed intensity levels (odd column), along with the unprogrammed pixels (from the even columns), are reproduced to for better viewing comparison.**

The rows were programmed to four different intensity levels with programming voltages of 20V, 25V, 27V, and 30V. After programming, the display was driven with constant DC voltages of $V_{DD}$ = 10V, $V_{SELECT}$ = 10V and $V_{DATA}$ = 8V. No pixel refreshes are performed. Representative pixels of each intensity level, along with unprogrammed pixels (from even rows), are reproduced in Figure 6.14 for better brightness comparison. R1, R5, R6, and R2 are programmed with 20V, 24V, 28V, and 32V, respectively. As the programming voltage is increased, raising the ST-TFT threshold, the brightness of the pixel decreases as expected.

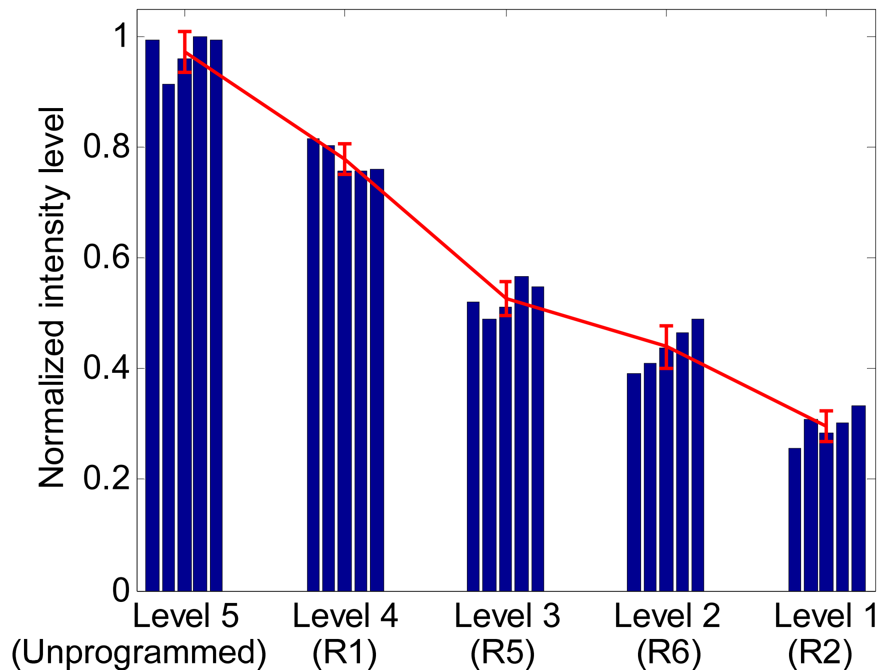


**Figure 6.15 Measured brightness statistics of the pixels from the array.**

Figure 6.15 shows the brightness level statistics of pixels from an integrated AMOLED display. Each brightness level shows, the brightness of the 5 programmed pixels from a given row. Pixels that have been programmed to the same brightness exhibit a standard deviation in brightness of ~4%, demonstrating good uniformity and control in setting the pixel brightness.

### 6.3. Summary

The conventional AMOLED pixel architecture requires power-consuming refresh cycles even if the image displayed is not changing. It also requires a storage capacitor, which limits pixel

fill factor, to hold the control voltage in between refreshes. We have successfully demonstrated a new approach for the control of pixel brightness by adjusting the threshold voltage of the OLED driver ST-TFT. The stored $V_T$ is programmed in an analog fashion to control the pixel brightness. In this architecture, the pixels do not need storage capacitors and as a result they achieve a better fill factor. The display can also potentially offer lower power consumption for low-frame-rate or static display applications by eliminating the extra refresh cycles needed to maintain a static image.

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# Summary and future work

The goal of this thesis was to find creative ways to improve the performance, reduce the cost and extend the functionality of a-Si-based large area electronics. To this end, we have developed a high-performance device structure in the top-gate a-Si TFT with a self-aligned silicide source/drain, a low-cost, high throughput fabrication technique in self-aligned imprint lithography, an innovative functionality in the non-volatile memory TFT, and a novel application in the AMOLED display architecture without pixel refresh.

The top gate a-Si TFT with self-aligned silicide source/drain eliminates the parasitic overlap capacitances that detrimentally affect the power and speed performance of conventional bottom-gate a-Si TFTs. This device can be fabricated with a simple two-photomask process without the use of specialized lithography tools or implantation and high temperature anneal, which are needed in traditional self-alignment processes. The process temperatures are less than 280°C, allowing this device to be fabricated on flexible substrates. The DC performance of the device is among the best ever reported for top-gate TFTs and on par with the bottom-gate TFTs. Therefore, we believe the top gate self-aligned silicide structure is an attractive path for high-speed and low power a-Si TFT circuitry on flexible substrates.

SAIL tackles the challenge of fabricating large-area electronic circuits on dimensionally unstable substrates such as flexible plastics. By using a single imprint step to transfer a three-dimensional mask structure that can be used to define all necessary device layers, SAIL eliminates misalignment due to substrate distortion, which not only improves yield but also reduces cost associated with multiple photolithography steps. SAIL, as proposed by Hewlett Packard, can only be used to make conventional bottom-gate TFTs, which have parasitic overlaps capacitances. We have demonstrated that SAIL can be used to fabricate our high performance top-gate TFT with self-aligned silicide contacts. We believe SAIL can potentially be a low cost and high throughput technique for fabrication of large area electronics on flexible substrates.

The a-Si TFT based non-volatile devices provides an efficient and low cost way of integrating memory capability into existing a-Si large area electronics applications. It can also potential enable many novel functionalities. We have demonstrated an a-Si floating gate non-volatile TFT, which works based on electrons tunneling into an a-Si floating gate from the channel or out from the floating gate into the channel depending on the sign of the applied gate voltage. The trapped charge or lack thereof determines the threshold voltage, which serves at the memory state. This initial demonstration suffered from drain-voltage-dependence saturation current and short retention issues. These problems were resolved with an improved ST-TFT non-volatile memory structure and improved tunnel $SiN_x$ deposition conditions.

A novel functionality enabled by the ST-TFT nonvolatile memory device is an active matrix organic light emitting diode display architecture that does not require pixel refresh. The conventional AMOLED pixel architecture requires power-consuming refresh cycles even if the image displayed is not changing. It also requires a storage capacitor, which limits pixel fill factor, to hold the control voltage in between refreshes. By integrating the ST-TFT as the driver TFT in the pixel circuit, we eliminate the need for refresh cycles and storage capacitors. The pixel brightness is stored in the threshold voltage of the memory TFT. As result, the novel AMOLED architecture achieves better pixel fill factor and potentially better power performance due to fewer refresh cycles. It also has the added capability of the storing programmed images without power. Therefore, we believe the new AMOLED architecture enabled by the ST-TFT is an attractive option for static or low-frame-rate display applications.

These findings suggest that there is plenty of room for creative innovations in device structure, fabrication technique and functionality to improve the performance and reduce the cost of a-Si based large area electronics. Some potential future work following this thesis are listed below:

I. Explore ambipolar behavior of the top-gate amorphous silicon TFT with self-aligned silicide source/drain. Viable p-channel device could lead to power efficient CMOS circuit applications.

II. Resolve circuit integration issues with a-Si top-gate TFT with self-aligned silicide source/drain. Integrate devices into circuit application such as ring oscillators to demonstrate the power and speed benefits over the conventional bottom-gate devices.
III. Optimize SAIL processing parameters to obtain better device performance and yield.
IV. Implement SAIL on flexible substrate.
V. SAIL fabrication of circuits such as active matrix backplanes.
VI. Reduce the magnitude of the programming/erasing voltages required for the ST-TFT by using thinner dielectrics. This may require exploration of different dielectric materials as $SiN_x$ may become leaky at thickness below 100nm.

# Appendices

*Appendix A. fabrication processes of the standard bottom-gate a-Si TFTs*

All thermal evaporations steps were performed using the Edwards Auto 306 thermal evaporator.

All lithography steps were performed using the MA6 mask aligner.

All plasma etching were performed using the PT720 plasma etcher.

Back channel etched TFT process

1. Gate Cr thermal evaporation: 60nm
2. Lithography 1: gate electrodes
3. Cr etch with Cr-7 wet etchant: 1min
4. Solvent clean of sample
5. Gate $SiN_x$ deposition: $SiH_4/NH_3$ 14sccm/130sccm, 500mT, 5W, 40min (300 300 280)
6. Channel intrinsic a-Si deposition: $SiH_4$ 50sccm, 500mT, 4W, 25min, (250 250 230)
7. n+ a-Si deposition: $SiH_4/PH_3$ 44sccm/6sccm, 500mT, 4W, 3min, (270 270 210)
8. Lithography 2: device active area
9. Si etch: $SF_6/CCl_2F_2$ 60sccm/20sccm 100mT 100W, 2min15s
10. Solvent clean of sample
11. Lithography 3: Gate contact via
12. $SiN_x$ etch: $CF_4/O_2$ 70/10 50mT 100W 2min
13. Solvent clean of sample
14. Lithography 4: S/D liftoff
15. 100:1 HF dip to remove native oxide on $n^+$ a-Si: 5s
16. S/D Cr thermal evaporation: 80nm
17. S/D liftoff via ultrasonic bath in Acetone
18. Solvent clean of sample
19. n+ a-Si etch: $CCl_2F_2/O_2$ 70sccm/10sccm 100mT 100W 3min30s

20. Anneal in the PECVD I-ch at heater set point (210 210 180): 60min

Back channel passivated TFT process

1. Gate Cr thermal evaporation: 60nm
2. Lithography 1: gate electrodes
3. Cr etch with Cr-7 wet etchant: 1min
4. Solvent clean of sample
5. Gate $SiN_x$ deposition: $SiH_4/NH_3$ 14sccm/130sccm, 500mT, 5W, 40min (300 300 280)
6. Channel intrinsic a-Si deposition: $SiH_4$ 50sccm, 500mT, 4W, 25min, (250 250 230)
7. Passivation $SiN_x$ deposition: $SiH_4/NH_3$ 14sccm/130sccm, 500mT, 5W, 30min (290 290 260)
8. Lithography 2: back channel passivation
9. Passivation $SiN_x$ etch: $CF_4/O_2$ 70/10 50mT 100W 1min
10. Solvent sample clean
11. 100:1 HF dip to remove native oxide on a-Si: 5s
12. n+ a-Si deposition: $SiH_4/PH_3$ 44sccm/6sccm, 500mT, 4W, 3min, (270 270 210)
13. Lithography 3: device active area
14. Si etch: $SF_6/CCl_2F_2$ 60sccm/20sccm 100mT 100W, 2min15s
15. Solvent clean of sample
16. Lithography 4: Gate contact via
17. SiNx etch: $CF_4/O_2$ 70/10 50mT 100W 2min
18. Solvent clean of sample
19. Lithography 5: S/D liftoff
20. 100:1 HF dip to remove native oxide on $n^+$ a-Si: 5s
21. S/D Cr thermal evaporation: 80nm
22. S/D liftoff via ultrasonic bath in Acetone
23. Solvent clean of sample
24. n+ a-Si etch: $CCl_2F_2/O_2$ 70sccm/10sccm 100mT 100W 3min30s

25 Anneal in the PECVD I-ch at heater set point (210 210 180): 60min

*Appendix B. Taurus device code for a-Si Schottky barrier transistor simulation*

```
###############################################################################
# Structure generation for NiSi2 thin film schottky contact transistor

# Enable device mode
Taurus {device}

# Define some variables
Define(ContL=20um)
Define(ContT=20nm)
Define(NitrideT=300nm)
Define(CrT=80nm)
Define(GateL=20um)
Define(asiT=250nm)
Define(blah=1nm)

#file name
Define(Devicename=concat("SBT_Nitride_", $NitrideT, "_L_", $GateL, "_depth_", $ContT))

# Define the device size, list the regions, and specify fixed mesh lines
DefineDevice (
minX=0, maxX=expr($ContL+$GateL+$ContL),
minY=-5nm, maxY=expr($CrT+$NitrideT+$asiT),
Region (name=Sub, material=ASi),
Region (name=GateDiel, material=Nit),
Region (name=Gate, material=electrode),
Region (name=sourceC, material=NiSi2),
Region (name=drainC, material=NiSi2),
x=expr($ContL/2), x=expr($ContL+$GateL/2), x=expr($ContL+$GateL+$ContL/2),
y=expr($CrT), y=expr($CrT+$NitrideT), y=expr($CrT+$NitrideT+$ContT)
)

# Define the amorphous silicon substrate region
DefineBoundary (
region=Sub,
Polygon2D (
Point (x=0, y=expr($CrT+$NitrideT+$ContT)),
Point (x=expr($ContL), y=expr($CrT+$NitrideT+$ContT)),
Point (x=expr($ContL), y=expr($CrT+$NitrideT)),
Point (x=expr($ContL+$GateL), y=expr($CrT+$NitrideT)),
Point (x=expr($ContL+$GateL), y=expr($CrT+$NitrideT+$ContT)),
Point (x=expr($ContL+$GateL+$ContL), y=expr($CrT+$NitrideT+$ContT)),
Point (x=expr($ContL+$GateL+$ContL), y=expr($CrT+$NitrideT+$asiT)),
Point (x=0, y=expr($CrT+$NitrideT+$asiT)),
```

```
)
)

# Define the Nitride region
DefineBoundary (
region=GateDiel,
Polygon2D (
Point (x=expr($ContL), y=expr($CrT)),
Point (x=expr($ContL+$GateL), y=expr($CrT)),
Point (x=expr($ContL+$GateL), y=expr($CrT+$NitrideT)),
Point (x=expr($ContL), y=expr($CrT+$NitrideT))
)
)

# Define the electrode gate region
DefineBoundary (
region=gate,
Polygon2D (
Point (x=expr($ContL), y=0),
point (x=expr($ContL+$GateL), y=0),
point (x=expr($ContL+$GateL), y=expr($CrT)),
point (x=expr($ContL), y=expr($CrT))
)
)

# Define the Source region
DefineBoundary (
region=sourceC,
Polygon2D (
Point (x=0, y=expr($CrT+$NitrideT)),

point (x=expr($ContL), y=expr($CrT+$NitrideT)),
point (x=expr($ContL), y=expr($CrT+$NitrideT+$ContT)),
point (x=0, y=expr($CrT+$NitrideT+$ContT))
)
)

# Define the Drain region
DefineBoundary (
region=drainC,
Polygon2D (
Point (x=expr($ContL+$GateL), y=expr($CrT+$NitrideT)),

point (x=expr($ContL+$GateL+$ContL), y=expr($CrT+$NitrideT)),
point (x=expr($ContL+$GateL+$ContL), y=expr($CrT+$NitrideT+$ContT)),
point (x=expr($ContL+$GateL), y=expr($CrT+$NitrideT+$ContT))
)
)

# Substrate Doping: P-type Uniform
```

```
Profile (name=Ptype, region=sub, Uniform (value=1e16))

# Flat Contacts
DefineContact (name=source, X (min=0, max=expr($ContL)), Y (min=expr($CrT+$NitrideT),
max=expr($CrT+$NitrideT+$ContT)))
DefineContact (name=drain, X (min=expr($ContL+$GateL),
max=expr($ContL+$GateL+$ContL)), Y (min=expr($CrT+$NitrideT),
max=expr($CrT+$NitrideT+$ContT)))

#include the physics files - using the silicon one for now (A-Si not yet available)
Include("Physics_Silicon.pdm")



# Set gate workfunction
Contact (name=gate, type = schottky,workfunction=4.5)
Contact (name=source, type=schottky, workfunction=4.25)
Contact (name=drain, type=schottky, workfunction=4.25)

#activate solution in NiSi2 material
activateEquation(name=poissons,material=NiSi2)
activateEquation(name=electronContinuity,material=NiSi2)
activateEquation(name=electricConductance,material=NiSi2)
# Initial coarse regrid
Regrid (gridProgram=pm, meshSpacingX=10um, meshSpacingY=0.1um)

# Regrid in channel
Regrid (
gridProgram=pm, region=Sub, meshspacingy=1nm,
minX=expr($ContL), maxX=expr($ContL+$GateL),
minY=expr($CrT+$NitrideT), maxY=expr($CrT+$NitrideT+$ContT)
)

# Regrid in channel near the contact
Regrid (
gridProgram=pm, region=Sub, meshspacingx=5nm,
minX=expr($ContL), maxX=expr($ContL+$ContL/200),
minY=expr($CrT+$NitrideT), maxY=expr($CrT+$NitrideT+$ContT)
)

# Regrid in channel near the contact
Regrid (
gridProgram=pm, region=Sub, meshspacingx=5nm,
minX=expr($ContL+$GateL-$ContL/200), maxX=expr($ContL+$GateL),
minY=expr($CrT+$NitrideT), maxY=expr($CrT+$NitrideT+$ContT)
)

#Change iteration setting hoping it would converge
Numerics(
   Iterations=100,relativeerror=1.e-8,
```

```
    linearsolver=direct,itresid=1e-7,
    linearsolver=ilucgs,itresid=1e-7,maxiiter=400,
    linearsolver=GBiCG1,linScale=1,
    linearsolver=ilugmres,maxBackVector=200,linScale=2,itresid=5.e-7, maxiiter=400
    OptimalWeight (
        hole
        electron
        conductance
        KCLTolerance=1e-20
    )
)

# Zero-carrier solve at equilibrium
Symbolic (carriers=0, conductance)

# Preliminary solution of the Poissons equation at the equilibrium
Solve {}

# Regrid on potential
#Regrid (
#gridProgram=pm, meshSpacing=5nm,
#Criterion (name=ElectricPotential, delta=.1, type=linear)
#)

# Regrid to desired grading factor and maximum element angle
Regrid (
gridProgram=pm, region=Sub,
gradingFactor=2.01, MaximumAngle (value=90)
)

# Redo solve
Solve {}

Save (meshfile=concat($Devicename, "_eqbm.tdf"),
            #Treefile=concat($Devicename, ".tree"),
            #Physicsfile=concat($Devicename, ".physics"),
            Add(
                        ConductionBand,
                        ValenceBand,
                        VacuumLevel,
                        ConductorFermiPotential,
                        electronquasifermienergy
                        #electronLifetime,
                        #holeLifetime,
        #SRHRecombination,
        #AugerRecombination,
        #DirectRecombination,
        #electroninterfacetraprecombination,
        #holeinterfacetraprecombination
            )
```

```
)

################################################################################
# Calculate the Gate transfer Characteristics

# Enable device mode
Taurus {device}

#Define some variables
Define(startvg=0)
#Define(stopvg=20)
Define(vgstep=1)
Define(vd=0.15)
Define(Devicename = "SBT_Nitride_0.3_L_20_depth_0.02")

# Load device structure
DefineDevice (meshfile=concat($Devicename, "_eqbm.tdf"))

# Include common physics models
Include (Physics_Silicon.pdm)


# Set gate workfunction
Contact (name=gate, type = schottky, workfunction=4.5)


#activating solution in the contact region
activateEquation(name=poissons,material=NiSi2)
activateEquation(name=electronContinuity,material=NiSi2)
activateEquation(name=electricConductance,material=NiSi2)


#Change iteration setting hoping it would converge
Numerics(
   Iterations=100,relativeerror=1.e-8,
   linearsolver=direct,itresid=1e-7,
   linearsolver=ilucgs,itresid=1e-7,maxiiter=400,
   linearsolver=GBiCG1,linScale=1,
   linearsolver=ilugmres,maxBackVector=200,linScale=2,itresid=5.e-7, maxiiter=400
   OptimalWeight (
      electron
      conductance
      KCLTolerance=1e-20
   )
)

# Set equilibrium bias on contacts
Voltage( electrode=source, value=0.0 )
Voltage( electrode=gate, value=0.0 )
Voltage( electrode=drain, value=0.0 )
```

```
# Specify zero-carrier solution
Symbolic (carriers=0)

# Do Solve
Solve { }

# Specify one-carrier solution with electrons
Symbolic (carriers=1, electron)

Voltage( electrode=drain, value=$vd )


Foreach stopvg (5)
{
	# Set drain bias
	#Voltage( electrode=drain, value=$vd)
	Foreach phim (4.65)
	{
		Contact
		(
			name=source,
			type=schottky,
			workfunction=$phim,
			#barrierlowering=true,
			#alpha=0,
			#vsurfn=0,
			#vsurfp=0
		)
		Contact
		(
			name=drain,
			type=schottky,
			workfunction=$phim,
			#barrierlowering=true,
			#alpha=0,
			#vsurfn=0,
			#vsurfp=0
		)


		Ramp
		(
			#logfile=concat($Devicename, "_vg_", $stopvg, "_phim_", $phim,
"_current.data"),
			Voltage (electrode=gate, startValue=expr($startvg), vStep=expr($vgstep),
nSteps=expr(abs($stopvg-$startvg)/$vgstep))

		)
	}
```

```
}

# Save TDF file
Save (
meshfile=concat($Devicename, "_vg_", $stopvg, "_vd_0.15", "_phim_", $phim, "_band.tdf")
        Add(
            ConductionBand,
            ValenceBand,
            VacuumLevel,
            #holeLifetime,
            #ElectronLifetime,
            #SRHRecombination,
            #AugerRecombination,
            #DirectRecombination,
            #electroninterfacetraprecombination,
            #holeinterfacetraprecombination
        )
)
```

*Appendix C. fabrication processes of the non-volatile a-Si TFT memory devices*

All thermal evaporations steps were performed using the Edwards Auto 306 thermal evaporator.

All lithography steps were performed using the MA6 mask aligner.

All plasma etching were performed using the PT720 plasma etcher.

Floating gate a-Si TFT

1. Gate Cr thermal evaporation: 60nm
2. Lithography 1: gate electrodes
3. Cr etch with Cr-7 wet etchant: 1min
4. Solvent clean of sample
5. Blocking gate $SiN_x$ deposition: $SiH_4/NH_3$ 14sccm/130sccm, 500mT, 5W, 30min (400 400 350)
6. Floating gate a-Si deposition: $SiH_4/H_2$ 20sccm/200sccm, 900mT, 4W, 3min, (250 250 230)
7. Lithography 2: Floating gate
8. Si etch: $SF_6/CCl_2F_2$ 60sccm/20sccm 100mT 100W, 12s
9. Tunnel gate $SiN_x$ deposition: $SiH_4/NH_3$ 14sccm/130sccm, 500mT, 5W, 2min (400 400 350)

10. Channel a-Si deposition: $SiH_4/H_2$ 20sccm/200sccm, 900mT, 4W, 60min, (250 250 230)
11. Passivation $SiN_x$ deposition: $SiH_4/NH_3$ 14sccm/130sccm, 500mT, 5W, 30min (290 290 260)
12. Lithography 3: back channel passivation
13. Passivation $SiN_x$ etch: $CF_4/O_2$ 70/10 50mT 100W 1min
14. Solvent sample clean
15. 100:1 HF dip to remove native oxide on a-Si: 5s
16. n+ a-Si deposition: $SiH_4/PH_3$ 44sccm/6sccm, 500mT, 4W, 3min, (270 270 210)
17. Lithography 4: device active area
18. Si etch: $SF_6/CCl_2F_2$ 60sccm/20sccm 100mT 100W, 2min15s
19. Solvent clean of sample
20. Lithography 5: Gate contact via
21. SiNx etch: $CF_4/O_2$ 70/10 50mT 100W 2min
22. Solvent clean of sample
23. Lithography 6: S/D liftoff
24. 100:1 HF dip to remove native oxide on $n^+$ a-Si: 5s
25. S/D Cr thermal evaporation: 80nm
26. S/D liftoff via ultrasonic bath in Acetone
27. Solvent clean of sample
28. n+ a-Si etch: $CCl_2F_2/O_2$ 70sccm/10sccm 100mT 100W 3min30s
29. Anneal in the PECVD I-ch at heater set point (210 210 180): 60min

SiNx trap a-Si TFT

Standard $SiN_x$: $SiH_4/NH_3$ 14sccm/130sccm, 500mT, 5W, (400 400 350)

Improved $SiN_x$: $SiH_4/NH_3/H_2$ 6sccm/150sccm/90sccm, 500mT, 5W, (400 400 350)

1. Gate Cr thermal evaporation: 60nm
2. Lithography 1: gate electrodes
3. Cr etch with Cr-7 wet etchant: 1min

4. Solvent clean of sample
5. Blocking gate $SiN_x$ deposition: Standard $SiN_x$ 15min / Improved $SiN_x$ 20min
6. a-Si deposition: $SiH_4/H_2$ 20sccm/200sccm, 900mT, 4W, 3min, (250 250 230)
7. Si etch: $SF_6/CCl_2F_2$ 60sccm/20sccm 100mT 100W, 15s
8. Tunnel gate $SiN_x$ deposition: standard $SiN_x$ 1min / Improved $SiN_x$ 1min30s
9. Channel a-Si deposition: $SiH_4/H_2$ 20sccm/200sccm, 900mT, 4W, 60min, (250 250 230)
10. Passivation $SiN_x$ deposition: $SiH_4/NH_3$ 14sccm/130sccm, 500mT, 5W, 30min (290 290 260)
11. Lithography 2: back channel passivation
12. Passivation $SiN_x$ etch: $CF_4/O_2$ 70/10 50mT 100W 1min
13. Solvent sample clean
14. 100:1 HF dip to remove native oxide on a-Si: 5s
15. n+ a-Si deposition: $SiH_4/PH_3$ 44sccm/6sccm, 500mT, 4W, 3min, (270 270 210)
16. Lithography 3: device active area
17. Si etch: $SF_6/CCl_2F_2$ 60sccm/20sccm 100mT 100W, 2min15s
18. Solvent clean of sample
19. Lithography 4: Gate contact via
20. SiNx etch: $CF_4/O_2$ 70/10 50mT 100W 2min
21. Solvent clean of sample
22. Lithography 5: S/D liftoff
23. 100:1 HF dip to remove native oxide on $n^+$ a-Si: 5s
24. S/D Cr thermal evaporation: 80nm
25. S/D liftoff via ultrasonic bath in Acetone
26. Solvent clean of sample
27. n+ a-Si etch: $CCl_2F_2/O_2$ 70sccm/10sccm 100mT 100W 3min30s
28. Anneal in the PECVD I-ch at heater set point (210 210 180): 60min

*Appendix D. List of patent disclosures, publications and conference presentations resulting from this thesis*

Patent disclosures

1. “Top-gate amorphous silicon TFT with self-aligned silicide source and drain”, Yifei Huang and James Sturm. Disclosure filed September 2008
2. “Self-aligned imprint lithography for the fabrication of top-gate amorphous silicon TFT with self-aligned silicide source and drain”, Yifei Huang and James Sturm, Disclosure filed September 2008
3. “Novel AMOLED pixel architecture without pixel refresh enabled by a-Si non-volatile TFT memory”, Yifei Huang and James Sturm, Disclosure filed Oct 2011

Journal publications

1. Y. Huang, S. Wagner and J. C. Sturm, “Amorphous silicon thin film transistor based non-volatile memory with room-temperature retention time > 10 years”, *Applied Physics Letters*, Submitted for peer review in June 2011
2. Y. Huang, S. Wagner and J. C. Sturm, “Non-volatile amorphous silicon thin-film transistor memory structure for drain-voltage independent saturation current”, *IEEE Transaction of Electron Devices*, Vol. 58 , Iss. 9, in the press as of July 2011
3. L. Han, Y. Huang, J. C. Sturm, and S. Wagner, “Self-Aligned Top-Gate Coplanar a-Si:H Thin-Film Transistors With a SiO2–Silicone Hybrid Gate Dielectric”, *IEEE Electron Device Letters*, Vol. 32, no. 1, pp. 36, Jan 2011
4. E. Lausecker, Y. Huang, T. Fromherz, J. C. Sturm, and S. Wagner, “Self-aligned imprint lithography for top-gate amorphous silicon thin-film transistor fabrication”, *Applied Physics Letters*, Vol. 96, p 263501, June 2010
5. Y. Huang, B. Hekmatshoar, S. Wagner and J. C. Sturm , “Static active-matrix OLED display without pixel refresh enabled by amorphous-silicon non-volatile memory”, *Journal of Society for Information and Displays*, Vol. 18, iss. 11, pp. 879, 2010
6. Y. Huang, B. Hekmatshoar, S. Wagner and J. C. Sturm , “High Retention-Time Nonvolatile Amorphous Silicon TFT Memory for Static Active Matrix OLED Display without Pixel Refresh”, *Electrochemical Society Transactions*, Vol. 33, iss. 5, pp. 365, 2010
7. Y. Huang, S. Wagner and J. C. Sturm, “Amorphous Silicon Floating Gate Transistor”, *Proceedings of 67th Annual Device Research Conference, Conference Digest*, p 135-136, June 2009
8. Y. Huang, B. Hekmatshoar, S. Wagner and J. C. Sturm, “Electron Injection Mechanism in Top-gate Amorphous Silicon Thin-film Transistors with Self-aligned Silicide Source and Drain”, *Proceedings of 66th Annual Device Research Conference, Conference Digest*, p 241-242, June 2008

9. Y. Huang, B. Hekmatshoar, S. Wagner, J.C. Sturm, “Top-gate Amorphous Silicon TFT with Self-aligned Silicide Source/Drain and High Mobility”, *IEEE Electron Device Letters*, Vol: 29 (7) pp. 737-739, 2008

Conference presentations

1. Y. Huang, B. Hekmatshoar, S. Wagner and J. C. Sturm , “High Retention-Time Nonvolatile Amorphous Silicon TFT Memory for Static Active Matrix OLED Display without Pixel Refresh”, presented at the 218th Electrochemical Society Meeting, October 2010

2. Y. Huang, S. Wagner and J. C. Sturm, “High retention-time nonvolatile amorphous silicon TFT memory for static active matrix OLED display without pixel refresh”, presented in at the 68th Annual Device Research Conference, University of Notre Dame, June 2010

3. B. Hekmatshoar, Y. Huang, S. Wagner and J. C. Sturm, “Effect of the Gate Nitride on the Low Field Lifetime of Highly Stable Amorphous Silicon Thin Film Transistors”, presented at the 9th Annual Flexible Display & Microelectronics Conference, Phoenix, AZ, USA, February 2010

4. Y. Huang, S. Wagner and J. C. Sturm, “Amorphous Silicon Floating Gate Transistor”, 67th Annual Device Research Conference, presented at Penn State University, PA, June 2009

5. B. Hekmatshoar, K. Cherenack, Y. Huang, S. Wagner and J. C. Sturm, “100-Year Low-Gate-Field Half-life of Amorphous-Si Thin-Film Transistors with a Plastic-Compatible Modified Gate Nitride Process”, presented at the Materials Research Society Spring Meeting, San Francisco, CA, April 2009

6. Y. Huang, S. Wagner and J. C. Sturm, “Transient Phenomena in Top-gate Amorphous Silicon Thin-film Transistors with Self-Aligned Silicide Source and Drain”, Proceedings of 5th Annual International Thin-Film Transistor Conference, Paris, France, March 2009

7. Y. Huang, B. Hekmatshoar, S. Wagner and J. C. Sturm, “Electron Injection Mechanism in Top-gate Amorphous Silicon Thin-film Transistors with Self-aligned Silicide Source and Drain”, 8th Annual Flexible Electronics & Display Conference, Phoenix, AZ, February 2009

8. Y. Huang, B. Hekmatshoar, S. Wagner and J. C. Sturm, “Electron Injection Mechanism in Top-gate Amorphous Silicon Thin-film Transistors with Self-aligned Silicide Source and Drain”, 66th Annual Device Research Conference, presented at Santa Barbara, CA, June 2008

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