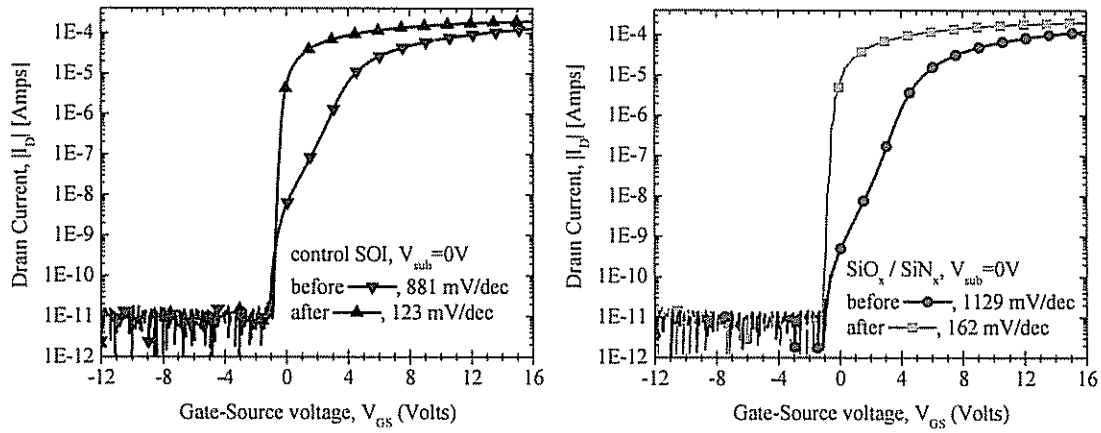
anneal is important not only for ohmic p-type contacts, but for reducing gate oxide interface states present in both nFET and pFET devices.

In order to obtain well-behaved devices, the MOSFETs presented below (unless otherwise specified) were all fabricated with the process described above in Sec. 7.1: post-implant anneals of 30 min at 700°C (nFETs) and 850°C (pFETs), followed by Cr/Al metallization and a forming gas anneal.

7.2.2 Choosing a Substrate Bias for Full Channel Depletion

A schematic cross-section of a completed transistor is shown in Fig. 7.26. The silicon channel is sandwiched in between two dielectrics: the gate oxide and the BPSG layer. There are effectively two transistor gates, one from the top poly-Si/TEOS oxide/silicon channel stack, and the second from the back silicon substrate/BPSG/silicon channel stack. These will be referred to as the "top" and "back" gate, respectively. Because the silicon layer is relatively thin (< 100 nm), the channel can be gated by either of these MOS capacitors. In this section the effect of substrate voltage on transistor current-voltage characteristics is evaluated, and appropriate substrate bias values for device operation and characterization are chosen.

For a dual gate transistor such as the thin SOI MOSFET shown in Fig. 7.26, the substrate bias has a strong effect on the charge carrier type and concentration in the silicon channel. In Fig. 7.27, the drain current vs gate voltage as a function of substrate voltage is plotted for pFET and nFET transistors with SiO_2/SiN_x barrier layers. The threshold voltages and subthreshold slopes have been extracted from the current-voltage data, and are plotted vs substrate voltage in Fig. 7.28. Take, for example, the nFET transistor. When the substrate voltage is strongly negative, the bottom of the p-type silicon layer is in accumulation, with the bottom silicon/oxide surface potential pinned at zero volts. The top gate can readily control the silicon layer depletion. Because the back surface potential is pinned, the top gate threshold voltage, $V_{t,top}$, is a constant value independent of the substrate voltage, V_{sub}. This is shown in the current-voltage curves for -40 to -20V, which are nearly indistinguishable in Fig. 7.27b, and by the constant nFET $V_{t,top}$ value of ~3.5V over the same voltage region, shown in Fig. 7.28a. As the substrate voltage increases, the back interface starts to become depleted, with the extent of



(a) (b)

Figure 7.25: Effect of forming gas anneal on sub-threshold slope of NMOSFETs for (a) control SOI sample (Fig. 7.5a) and (b) bonded sample with SiO_2/SiN_x barrier layers (Fig. 7.5d). The transistors are unstrained nFETs with W/L=120μm/20μm, fabricated on 300-μm x 300-μm islands aligned to the <110> crystal direction with Cr/Al metallization, and measured with V_{DS}=+0.1V. For both samples, the forming gas anneal greatly decreases the sub-threshold slope.

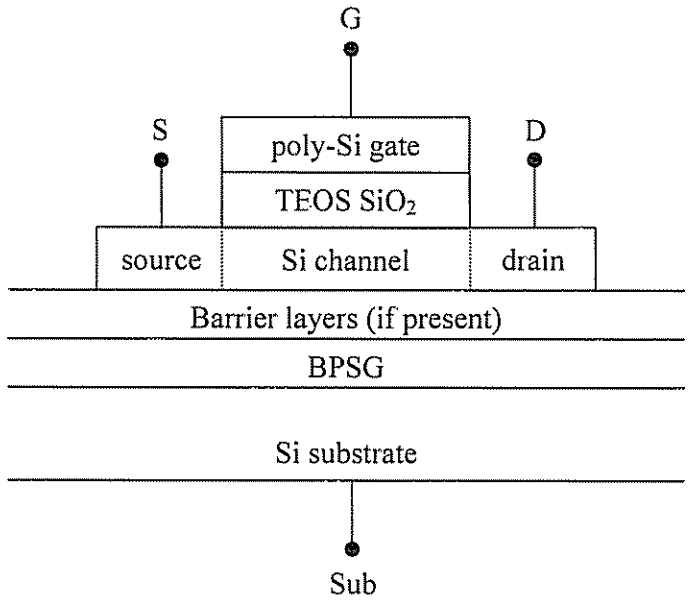
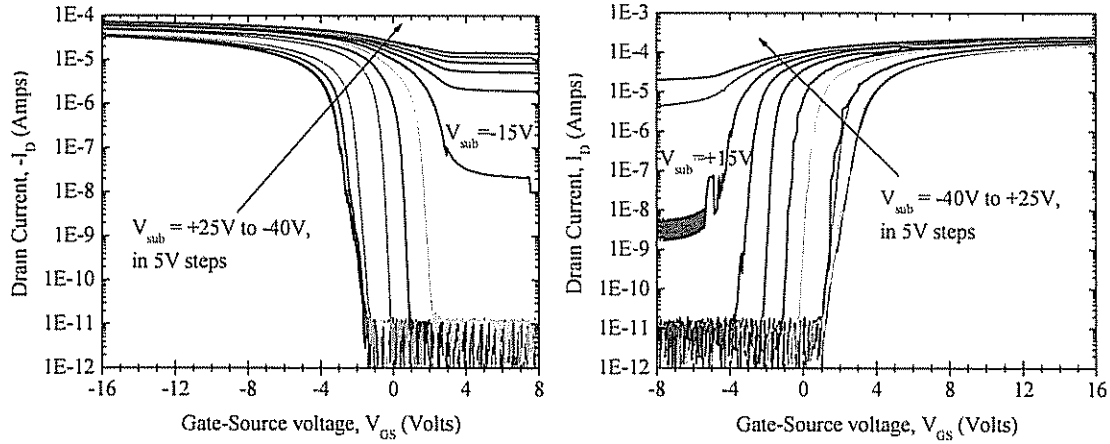
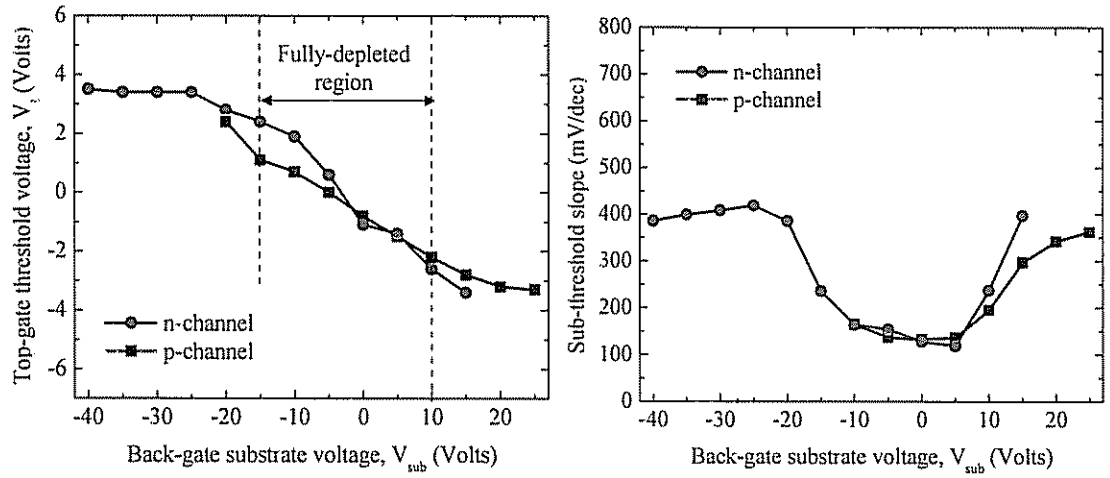


Figure 7.26: Schematic cross-section of a transistor, showing the four electrical nodes, gate (G), drain (D), source (S) and substrate (Sub). For simplicity, the passivation oxide and metallization are not drawn.



(a) (b)

Figure 7.27: Drain current vs gate voltage for various substrate bias values for (a) pFETs and (b) nFETs with $|V_{DS}| = 0.1V$. The samples have SiO_2/SiN_x barrier layers (after 7.5d), and the transistors have W/L = 120 μm / 20 μm on unstrained silicon (originally 300-μm x 300-μm islands) aligned to the <110> crystal directions.



(a) (b)

Figure 7.28: (a) Top-gate threshold voltage and (b) sub-threshold slope vs back-gate substrate voltage for bonded SOI nFETs and pFETs with SiO_2/SiN_x barrier layers. The plotted values have been extracted from the current-voltage curves shown in Fig. 7.27. In (a), the substrate voltage region for full depletion of the silicon channel is indicated. These two plots are used to select the substrate bias, V_{sub}=0 V, for further device characterization.

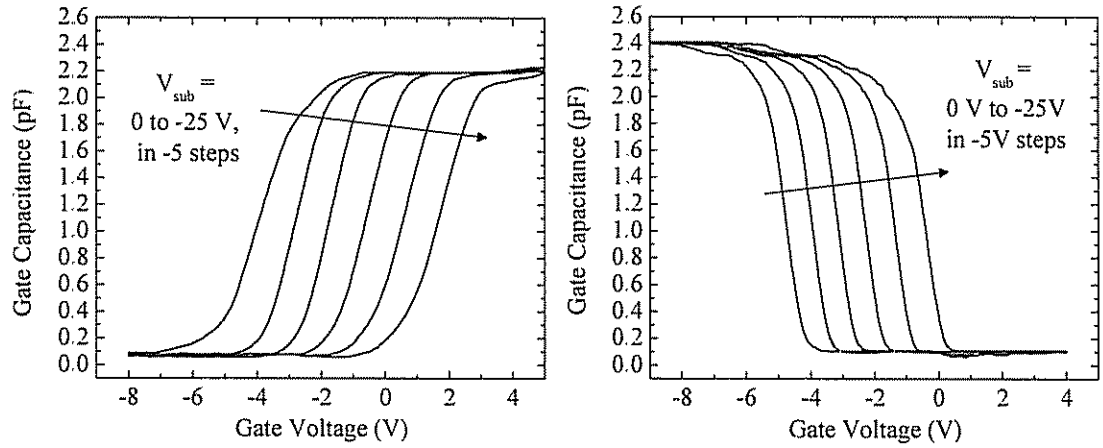
depletion determined by the back substrate voltage. Therefore the top gate threshold voltage will be linearly related to the substrate voltage. This region is known as "full depletion," and is the desired region of operation for the transistor. If the back substrate voltage on an nFET becomes very positive, the back channel interface will become inverted. The back channel then acts as a parasitic conduction channel, and it is difficult to satisfactorily turn off the transistor, even when the top gate is strongly negative. This is illustrated clearly in Fig. 7.27b, as the ON/OFF current ratio drops from 10^7 for V_{sub} =0V to ~10^1 for V_{sub} =+25V, and in the increase in sub-threshold slope shown in Fig. 7.28b from 130 mV/dec for V_{sub} =0V to 400 mV/dec for V_{sub} =+15V.

The pFET exhibits exactly analogous behavior, with the back channel being accumulated for large positive V_{sub}, and inverted for large negative V_{sub}, with a region of full-depletion in between, as shown in Figs. 7.27a and 7.28a. The dependence of the top-gate threshold voltage on the back substrate voltage is visible not only the transistor current-voltage characteristics, but also in gate capacitance vs gate voltage measurements. In Fig. 7.29, the C-V traces for both nFETs and pFETs shift along the voltage axis as the substrate voltage is changed.

For proper CMOS operation, the substrate voltage should be selected for full-depletion and minimal sub-threshold slopes of both NMOS and PMOS devices. For devices with SiO_2/SiN_x barrier layers, from Fig. 7.28 it is seen that a substrate voltage of zero volts will meet these criteria. A similar analysis was performed for each sample in Fig. 7.5. The results for the BPSG-only sample are shown in Fig. 7.30. Because there is no barrier layer between the BPSG and the silicon channel, phosphorus may have diffused from the BPSG into the silicon channel during FET processing. Therefore, the back interface has many trap states and a large negative substrate bias is needed for full-depletion. The chosen substrate voltage values for each sample type are listed in Table 7.3.

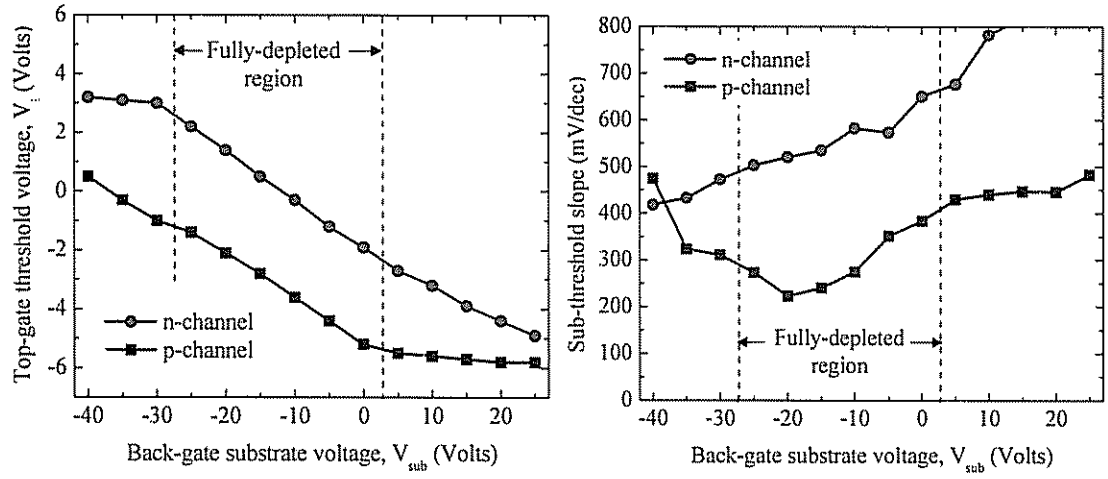
7.2.3 Optimizing the BPSG/Silicon Interface

The substrate voltages required for complete depletion of the silicon channel layer, listed in Table 7.3, vary greatly with sample type. Samples with no barrier layer (BPSG only) or a SiO_2 barrier layer require a large negative substrate bias (-15 to -20V)



(a) (b)

Figure 7.29: Gate capacitance vs. top gate voltage as a function of back substrate bias for bonded SOI (a) nFETs and (b) pFETs with no barrier layer (BPSG only). The transistors, with W/L = 120 μm / 20 μm, are fabricated on islands aligned to <100> that were initially 50 μm x 300 μm. The source and drain are grounded during C-V measurements at 20 kHz. The capacitance data has been smoothed by averaging adjacent 20 points.



(a) (b)

Figure 7.30: (a) Top-gate threshold voltage and (b) sub-threshold slope vs back-gate substrate voltage for bonded SOI nFETs (W/L = 120 μm / 10 μm) and pFETs (W/L = 120 μm / 20 μm) with no barrier layer (BPSG only). The transistors are on unstrained silicon (originally 300-μm x 300-μm islands) aligned to the <110> crystal directions. Based on these data, a substrate bias of V_{sub}=-20V is chosen. Note that for this sample the n-channel devices are not all well-behaved (due to anomalous processing problems) and thus the nFET sub-threshold slope does not reach a minimum in the fully-depleted region.

in order to deplete the channel region. In contrast, the control SOI sample requires only a grounded substrate (*i.e.*, zero substrate bias) for full depletion. The large substrate bias values reflect electronic trap states at the back silicon interface and unintentional phosphorus doping in the silicon channel, which negatively impact device performance. In this section these phenomena will be briefly investigated and it will be shown that their impact on device performance can be minimized by using SiO_2/SiN_x barrier layers.

In Fig. 7.31 typical drain current – gate voltage curves are shown for n- and p-FETs on several different substrate types. The samples with only BPSG ("no barrier") show very poor turn-on characteristics compared to control SOI devices. Device parameters for the curves of Fig. 7.31 are listed in Table 7.4. For pFETs the BPSG-only device has a sub-threshold slope of 292 mV/dec while the control SOI device has a slope of 105 mV/dec. The nFETs show an even greater difference: 521 vs 123 mV/dec, respectively. (The slopes observed here are larger than the ideal value for thermal SiO_2 on bulk silicon, 60 mV/dec, probably due to the deposited gate oxide.) Likewise, the mobilities measured for BPSG-only samples are significantly lower than those measured on control SOI devices. The hole mobility reaches 177 $cm^2V^{-1}s^{-1}$ on control devices but only 79 $cm^2V^{-1}s^{-1}$ on BPSG-only samples, while the electron mobilities are similarly reduced from 416 to 260 $cm^2V^{-1}s^{-1}$, respectively.

There are two reasons for the poor performance of devices on BPSG-only bonded SOI compared with transistors on control SOI wafers. First, the bonding interface can contain a large number of electronic traps. The cleanliness, surface roughness and chemical preparation of the bonding surfaces will all affect the density and type of electronic trap states at the interface. For the BPSG-only devices, the bonding interface occurs at the back of the silicon channel, and thus has a strong influence on device performance. Second, the BPSG layer contains boron and phosphorus which can readily out-diffuse into the silicon channel if an effective barrier layer is not present. This unintentional doping will shift the threshold voltage and lower the mobility by adding ionized-impurity scattering sites to the fully-depleted channel. It is proposed that the poor device turn-on and reduced mobilities observed in the BPSG-only devices are caused by electronic states at the bond interface and the out-diffusion of phosphorus into the silicon channel.

Sample	Chosen V_{sub}
BPSG only (Fig. 7.5b)	-20 V
SiO_2 barrier + BPSG (Fig. 7.5c)	-15 V
SiO_2/SiN_x barriers + BPSG (Fig. 7.5d)	0 (zero) V
control SOI (Fig. 7.5a)	0 (zero) V

Table 7.3: Substrate bias voltages chosen to ensure full depletion of the silicon channel layer.

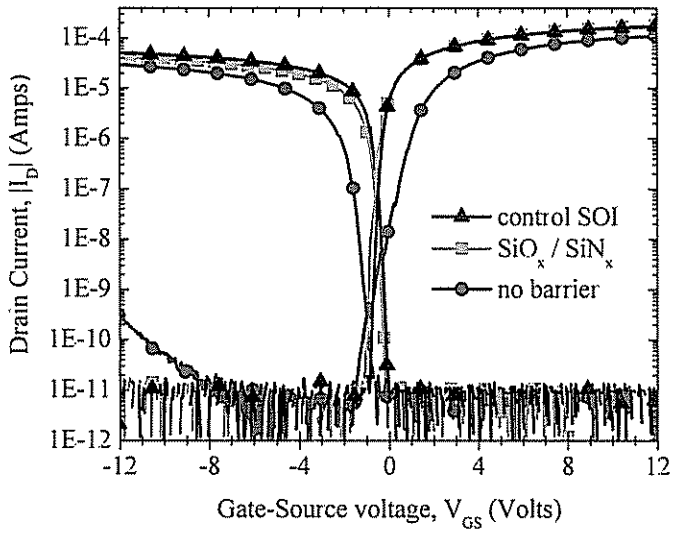


Figure 7.31: Drain-current vs gate-source voltage for various types of bonded SOI nFETs and pFETs. The devices have $|V_{DS}|$=0.1V, substrate biases as given in Table 7.3 and W/L = 120 μm / 20 μm, except the no barrier nFET, which has W/L = 120 μm / 10 μm. The transistors are on unstrained silicon (originally 300-μm x 300-μm islands) aligned to the <110> crystal directions.

Device	nFET	pFET	nFET	pFET
	sub-V_T slope, mV/dec		mobility, $cm^2/V/s$	
BPSG only (Fig. 7.5b)	521	292	260	79
SiO_2/SiN_x barriers + BPSG (Fig. 7.5d)	162	149	395	128
control SOI (Fig. 7.5a)	123	105	416	177

Table 7.4: Sub-threshold slopes and mobilities for the transistor curves shown in Fig. 7.31. The sample with only BPSG has very large slopes (poor device turn-on) and low mobility compared to the control SOI sample. The introduction of SiO_2/SiN_x barrier layers greatly reduces the sub-V_T slopes and increases the mobilities, so the values are close to the control SOI sample values.

The impact of both of these phenomena can be significantly reduced by the introduction of a barrier layer between the BPSG and silicon channel. Ideally, a barrier layer will completely prevent out-diffusion of boron and phosphorus into the channel. If a barrier layer caps the epitaxial silicon layer before initial wafer bonding, the bonding interface moves away from the silicon channel. Moreover, the back silicon channel interface quality is now determined by the barrier layer growth/deposition process, and not by the bonding process. For this work, barrier layers of thermally-grown SiO_2 and SiO_2 capped with LPCVD-SiN_x were used. The barrier layer growth/deposition processes are described in detail in Sec. 7.1.1. The thermal SiO_2 layer is used to create a high-quality electronic interface to the silicon channel, and the SiN_x is deposited as a diffusion barrier.

The results are visible in Fig. 7.31 and Tables 7.3 and 7.4 by comparing transistor performance on SiO_2/SiN_x barrier layers to the BPSG-only and control SOI samples. The SiO_2/SiN_x barrier devices require zero substrate bias for full-depletion, the same as for control SOI devices, indicating an acceptably low density of electronic states at the back silicon interface. The devices with SiO_2/SiN_x barrier layers turn-on more quickly than devices on BPSG only, with sub-threshold slopes of 162 and 149 mV/dec for the nFET and pFET devices shown in Fig. 7.31. Likewise, transistors made on samples with SiO_2/SiN_x barrier layers exhibit higher electron and hole mobilities compared to the BPSG-only sample. Clearly the presence of the double barrier layer has caused a significantly improvement in the device performance.

The efficacy of the SiN_x as a diffusion barrier can be examined by measuring boron and phosphorus concentrations in the silicon channel after FET processing by SIMS. In Fig. 7.32, dopant concentrations after annealing are plotted vs distance from the Si/BPSG interface, when no barrier layer is present. Fig. 7.32a shows the B and P concentrations measured by SIMS. Both boron and phosphorus have diffused out of the BPSG layer into the silicon channel, as is evident by the gradation in concentration peaking near the Si/BPSG interface and decreasing toward the top silicon surface. The dopant concentrations are quite high; in the middle of the silicon channel: $[P]=4x10^{18}$ cm^{-3}, and $[B]=1x10^{18}$ cm^{-3}. Note that due to the silicon dioxide capping layer used, the measured B and P concentrations are not accurate at the top SiGe surface. In

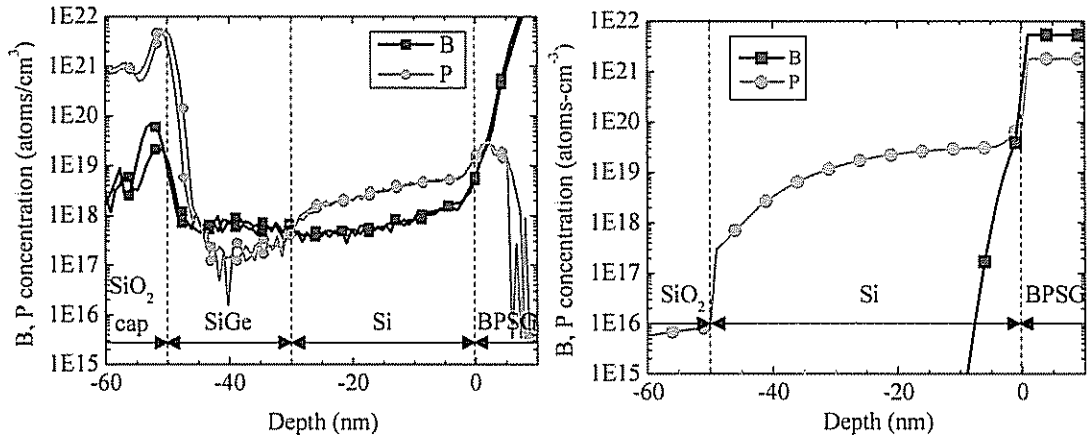


Figure 7.32: (a) Measured and (b) simulated boron and phosphorus concentrations vs sample depth after a 2-hr anneal at 800°C followed by a 30-min 850°C anneal for the BPSG-only structure of Fig. 7.5b capped with 28-nm SiO_2. The measurement results in (a) were taken using SIMS; the simulation script for (b) is found in Table 7.5. Arrows and dashed lines indicate interfaces between the various layers.

Table 7.5: TSUPREM4 simulation script for BPSG outdiffusion

```
INITIALIZE BORON=1E15

DEPOSITION MAT=OXIDE THICKNESS=0.200 BORON=5.4e21 PHOSPHOR=1.8e21
CONCENTR SPACES=200
DEPOSITION MAT=SILICON THICKNESS=0.050 SPACES=200
DEPOSITION MAT=OXIDE THICKNESS=0.030

DIFFUSION TEMP=800 TIME=120 INERT
DIFFUSION TEMP=850 TIME=30 INERT

SELECT Z=BORON
EXTRACT OUT.FILE="BPSG_anneal_B.data" PREFIX="Depth vs. Boron doping"
FOREACH DEPTH (-0.31 TO 0.5 STEP 0.001)
EXTRACT X=0.0 DISTANCE=@{DEPTH} Y.EXT VAL.EXT
END
EXTRACT CLOSE

SELECT Z=PHOSPHORUS
EXTRACT OUT.FILE="BPSG_anneal_P.data" PREFIX="Depth vs. P doping"
FOREACH DEPTH (-0.31 TO 0.5 STEP 0.001)
EXTRACT X=0.0 DISTANCE=@{DEPTH} Y.EXT VAL.EXT
END
EXTRACT CLOSE
```

Fig. 7.32b are plotted the predicted B and P concentrations after the same anneals, from a TSUPREM simulation script detailed in Table 7.5. For simplicity, the simulation was done with a single silicon layer instead of the Si/SiGe bi-layer present in the measured samples. Comparing the two figures, the simulation over-predicts the amount of phosphorus out-diffusion and under-predicts the boron out-diffusion. But the simulation agrees with the measurement on the critical fact that the phosphorus concentration in the channel due to out-diffusion will be significantly greater than that of boron, leading to a channel which is nominally n-type with compensated doping.

The boron and phosphorus that has out-diffused from the BPSG into the channel will affect the threshold voltage. Already it has been observed that the BPSG-only devices require a large negative substrate bias in order to fully deplete the transistors, compared to the control SOI and SiN_x barrier layer devices, which require only substrate grounding. According to SIMS, the net doping in the channel should be n-type, with N_D=3x10^{18} cm^{-3} (phosphorus concentration minus boron concentration). The threshold voltage required to fully deplete the doped channel will thus shift by $\Delta V_T = -t_{Si} N_D q / C_{ox}$, where t_{Si} is the silicon thickness (27 nm), q is the elemental charge and C_{ox} is the gate oxide capacitance (1.04x10^{-7} F/cm). Using this simple approximation, the expected shift in threshold voltage is -12 V, close to the -20 V observed.

The high doping level of phosphorus in the channel will also affect the sub-threshold slope. For a bulk silicon MOSFET, the sub-threshold slope, S, is given [175] by $S = 2.3(kT/q)(1 + C_D/C_{ox})$, where kT/q is 26 mV at room temperature and $C_D = \varepsilon_{Si}/x_d$ is the depletion capacitance for a depletion width of $x_d = \sqrt{4\varepsilon_{Si}(kT/q)\ln(N_D/n_i)/qN_D}$, where the n_i is the intrinsic doping concentration (1.5x10^{10} cm^{-3} in silicon). For N_D=3x10^{18} cm^{-3}, x_d is 38 nm and S = 214 mV/decade. Note that the calculated depletion width is greater than the silicon channel thickness; therefore x_d should be set equal to t_{Si}, causing S to increase to 279 mV/decade. This is in general agreement with the measured sub-threshold slopes of 292 and 521 mV/decade for pFETs and nFETs, respectively, on BPSG only.

The SiN_x barrier layer has been added in order to reduce out-diffusion of B and P from the BPSG into the channel layer [8,161]. In Fig. 7.33 the measured B and P

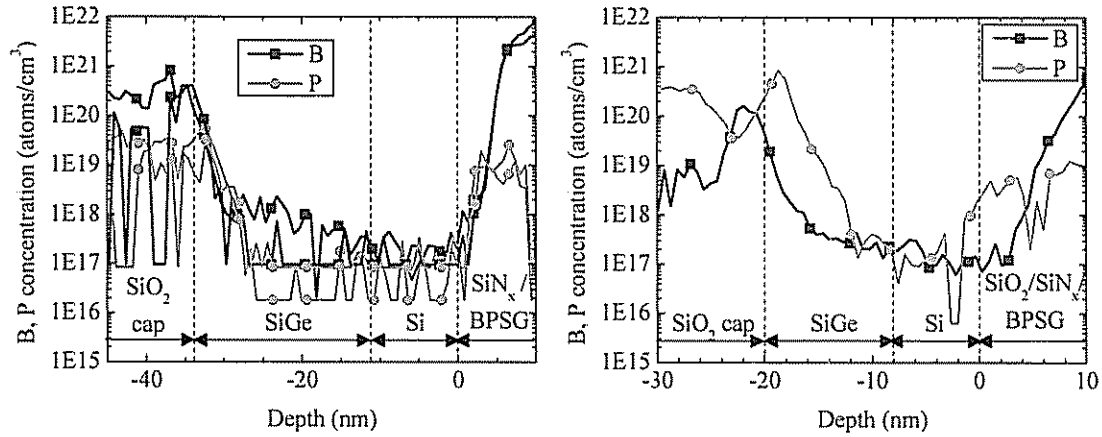


Figure 7.33: SIMS measurements of boron and phosphorus concentrations vs sample depth after a 2-hr anneal at 800°C followed by a 30-min 850°C anneal for (a) the SiN_x barrier structure of Fig. 5.2b and (b) the SiO_2/SiN_x barrier layer structure of Fig. 7.5d.

concentrations are plotted vs distance from the Si / barrier layer interface. Results are shown for a single SiN_x barrier layer (the structure of Fig. 5.2b) in Fig. 7.33a and a SiO_2/SiN_x double barrier layer (the structure of Fig. 7.5d) in Fig. 7.33b. The presence of a silicon nitride layer has completely prevented out-diffusion. The boron and phosphorus concentrations, which reach a maximum of about $5x10^{17}$ cm^{-3} in the silicon layers, are almost an order of magnitude lower than those shown in Fig. 7.32a without the nitride barrier layer. The presence of the SiO_2 layer in the SiO_2/SiN_x double barrier layer of Fig. 7.33b does not appreciably affect the out-diffusion; it remains low. The nitride layer is indeed effective in preventing out-diffusion of B and P from the BPSG layer into the silicon channel.

When only a SiO_2 barrier layer is present, the FET performance is poor, compared to samples where a dual-barrier layer of SiO_2 and SiN_x is present. As seen in Table 7.3, a substrate bias of -15 V is required to fully deplete the silicon layer for SiO_2 barriers. The average electron and hole mobilities for unstrained devices aligned to <110> on SiO_2 barrier layers of 373 and 76 $cm^2V^{-1}s^{-1}$ are lower, and the sub-threshold slopes of 226 and 356 mV/decade for n- and p-FETs, respectively, are larger, than for the SiN_x/SiO_2 barrier layer and control devices (described in Fig. 7.31 and Table 7.4). For both NMOS and PMOS, devices with SiO_2 barrier layers offer only marginal performance improvement over the BPSG-only devices. This FET data seems to indicate that the SiO_2 barrier layer does not significantly reduce dopant out-diffusion from the BPSG, although SIMS measurements on these samples to confirm this have not yet been taken. Since they offer little technological advantage, the SiO_2 barrier layer devices will not be pursued further.

By measuring transistor performance and dopant diffusion, and comparing the results with and without SiN_x barrier layers, it has been shown that the presence of a nitride layer between the BPSG and silicon channel effectively prevents boron and phosphorus out-diffusion and allows low doping levels in the channel. Moreover, the use of a SiO_2/SiN_x double barrier layer drastically improves the transistor sub-threshold slope and increases charge carrier mobility for both electrons and holes, by reducing the density of trap states at the back channel. Such barrier layers are thus a critical tool to enable the use of our BPSG-based strain generation technique in electrical or optical device applications.

7.3 Strain-Induced Mobility Enhancement

A fabrication scheme and process have been presented to make transistors with biaxially-strained, uniaxially-strained and unstrained silicon channels all on the same silicon-on-insulator sample. By optimizing the source/drain contact and BPSG barrier layer technologies, the resulting n- and p-MOSFETs show well-behaved current-voltage characteristics, typical of fully-depleted SOI transistors. In this section, the electron and hole mobility enhancements induced by biaxial and uniaxial strain in these silicon layers, which motivate the strain generation work presented in this thesis, will be measured and compared to predictions from bulk piezoresistance theory.

7.3.1 Strain-Induced Mobility Enhancement Predicted by Bulk Piezoresistance Theory

The physical basis of mobility enhancement in the inversion layer of biaxially-tensile strained-silicon MOSFETs is well understood and has been discussed above in Ch. 2. However the charge transport effects of uniaxial strain are not fully understood from a theoretical standpoint. Therefore, in order to come up with first-order predictions of the expected strain-induced mobility enhancements for our devices, bulk piezoresistance theory is used.

Silicon, germanium, and their alloy are piezoresistive materials, that is, their resistivity changes as stress or strain is applied [178]. The relationship between electric field, E, and current, J, is defined by the resistivity, ρ, where in the matrix representation [179]:

$$\begin{bmatrix} E_1' \\ E_2' \\ E_3' \end{bmatrix} = \begin{bmatrix} \rho_1' & \rho_6' & \rho_5' \\ \rho_6' & \rho_2' & \rho_4' \\ \rho_5' & \rho_4' & \rho_3' \end{bmatrix} \cdot \begin{bmatrix} J_1' \\ J_2' \\ J_3' \end{bmatrix}, \tag{7.2}$$

where the primed variables represent arbitrary cubic reference directions. The component resistivities are comprised of the isotropic resistivity, ρ_o, plus the change in resistivity, $\Delta\rho'$, due to piezoresistance:

$$\begin{bmatrix} \rho_1' \\ \rho_2' \\ \rho_3' \\ \rho_4' \\ \rho_5' \\ \rho_6' \end{bmatrix} = \begin{bmatrix} \rho_o \\ \rho_o \\ \rho_o \\ 0 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} \Delta\rho_1' \\ \Delta\rho_2' \\ \Delta\rho_3' \\ \Delta\rho_4' \\ \Delta\rho_5' \\ \Delta\rho_6' \end{bmatrix}, \text{ where} \tag{7.3}$$

$$\frac{1}{\rho_o}\begin{bmatrix} \Delta\rho_1' \\ \Delta\rho_2' \\ \Delta\rho_3' \\ \Delta\rho_4' \\ \Delta\rho_5' \\ \Delta\rho_6' \end{bmatrix} = \begin{bmatrix} \pi_{11}' & \pi_{12}' & \pi_{13}' & \pi_{14}' & \pi_{15}' & \pi_{16}' \\ \pi_{21}' & \pi_{22}' & \pi_{23}' & \pi_{24}' & \pi_{25}' & \pi_{26}' \\ \pi_{31}' & \pi_{32}' & \pi_{33}' & \pi_{34}' & \pi_{35}' & \pi_{36}' \\ \pi_{41}' & \pi_{42}' & \pi_{43}' & \pi_{44}' & \pi_{45}' & \pi_{46}' \\ \pi_{51}' & \pi_{52}' & \pi_{53}' & \pi_{54}' & \pi_{55}' & \pi_{56}' \\ \pi_{61}' & \pi_{62}' & \pi_{63}' & \pi_{64}' & \pi_{65}' & \pi_{66}' \end{bmatrix} \cdot \begin{bmatrix} \sigma_{11}' \\ \sigma_{22}' \\ \sigma_{33}' \\ \tau_{23}' \\ \tau_{13}' \\ \tau_{12}' \end{bmatrix}. \tag{7.4}$$

The piezoresistance coefficients are represented by π'_{ij}, while σ'_{ii} and τ'_{ij} represent the normal and engineering shear stresses, respectively, in the arbitrary reference directions. Here the analysis is limited to the linear (first-order) regime, which is justified because strain levels observed in this work are low (~1.0% maximum). For measurements of the non-linearity of piezoresistance in silicon, see Ref. [180], [181], [182], and [183].

For cubic crystals with a (001) surface plane, the piezoresistance coefficients are given by [184-186]

$$\boldsymbol{\pi}' = \begin{bmatrix} \pi_{11} - \frac{\pi_c}{2}\sin^2 2\theta & \pi_{12} + \frac{\pi_c}{2}\sin^2 2\theta & \pi_{12} & 0 & 0 & -\frac{\pi_c}{2}\sin 4\theta \\ \pi_{12} + \frac{\pi_c}{2}\sin^2 2\theta & \pi_{11} - \frac{\pi_c}{2}\sin^2 2\theta & \pi_{12} & 0 & 0 & +\frac{\pi_c}{2}\sin 4\theta \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ -\frac{\pi_c}{4}\sin 4\theta & +\frac{\pi_c}{4}\sin 4\theta & 0 & 0 & 0 & \pi_{44} + \pi_c \sin^2 2\theta \end{bmatrix} \tag{7.5}$$

where π_{11}, π_{12}, π_{44} are the piezoresistance constants that depend [178,187-189] on material, dopant type and dopant concentration, and are given in Table 7.6 for lightly-doped silicon. The variable θ is the angle in the (001) plane from the <100> direction, and $\pi_c = \pi_{11} - \pi_{12} - \pi_{44}$.

Here, what is relevant is the case when current and voltage occur in the same direction, which can be arbitrarily assigned to be the first component direction:

$$E_1' = \rho_1' \cdot J_1' = \rho_o \cdot \left(1 + \Delta\rho_1'/\rho_o\right) \cdot J_1' . \tag{7.6}$$

The fractional change in the resistance of the (001) layer due to stress or strain is then simply

$$\Delta\rho_1'/\rho_o = \pi_{11}'\sigma_{11}' + \pi_{12}'\sigma_{22}' + \pi_{13}'\sigma_{33}' + \pi_{16}'\tau_{12}' . \tag{7.7}$$

In our strain-generation process, the stress out of the plane is always zero, and thus the third term is equal to zero. Moreover, for the case of uniform stress in the plane of the film, one can neglect the shear stress term τ'_{12}. (As discussed in Ch. 4, the shear stress is strictly zero only at the center of the islands used for strain generation.) All that remains are two piezoresistance terms, one for the stress parallel to the current flow ($\pi'_{11}\sigma'_{11}$) and one for the stress perpendicular to the current flow ($\pi'_{22}\sigma'_{22}$). Thus Eqn. 7.7 simplifies to

$$\Delta\rho/\rho_o = \pi_\ell\sigma_\ell + \pi_t\sigma_t , \tag{7.8}$$

where the ℓ and t subscripts refer to the longitudinal (parallel) and transverse (perpendicular) directions, so that $\pi_\ell = \pi_{11}'$ and $\pi_t = \pi_{12}'$. For the (001) surface plane, in the <100> direction $\pi_\ell = \pi_{11}$ and $\pi_t = \pi_{12}$, while in the <110> direction, $\pi_\ell = 1/2\left(\pi_{11} + \pi_{12} + \pi_{44}\right)$and $\pi_t = 1/2\left(\pi_{11} + \pi_{12} - \pi_{44}\right)$.

When strain is biaxially-symmetric, the effective piezoresistance coefficient is just the sum of π_ℓ and π_t, also equal to the sum of π_{11} and π_{12}, which here will be defined as π_{biax}:

$$\Delta\rho_{biaxial}/\rho_o = \pi_{biax}\sigma_{biax} = \left(\pi_\ell + \pi_t\right)\sigma_{biax} = \left(\pi_{11} + \pi_{12}\right)\sigma_{biax} \tag{7.9}$$

Note that while the longitudinal and transverse piezoresistance coefficients are dependent on the crystal-direction of the electric field and current, the biaxial coefficient is constant in the plane of the film. The piezoresistance coefficient values of π_ℓ, π_t, π_{biax} given by Eqn. 7.5 are graphically plotted vs angle in the (001) plane for n- and p-type silicon in Fig. 7.34. The values of these coefficients in the <100> and <110> crystal directions for a silicon film with a (001) surface plane are given in Table 7.7.

So far these results are completely generic for the case of a biaxially-symmetric or asymmetric (*e.g.*, uniaxial) stress in the plane of a (001) film. The results have been stated

in terms of applied stress. Chapter 5 demonstrated a new method for generating uniaxial strain in thin silicon layers. In order to predict the results of these experiments, Eqns. 7.8 and 7.9 should be rewritten in terms of film strain, using Eqn. 3.14. The notation of m, for elastoresistance, is used to represent the coefficient relating the change in resistance to applied strain. The resistance change due to biaxial strain (for the case of zero stress normal to the surface, $\sigma_{zz} = 0$) is

$$\Delta\rho/\rho_o = m_\ell \varepsilon_\ell + m_t \varepsilon_t, \tag{7.12}$$

where, using Eqns. 3.14 and 7.8,

$$m_\ell = \frac{E}{1-\nu^2}\left(\pi_\ell + \nu\pi_t\right) \text{ and} \tag{7.13a}$$

$$m_t = \frac{E}{1-\nu^2}\left(\nu\pi_\ell + \pi_t\right). \tag{7.13b}$$

Where E, ν, π_ℓ, and π_t are all dependent on the crystal-direction of the current. Because a biaxial strain is simply a superposition of two uniaxial strains, the biaxial elastoresistance is equal to the sum of the two uniaxial components:

$$\Delta\rho_{biaxial}/\rho_o = m_{biax}\varepsilon_{biax} = \left(m_\ell + m_t\right)\varepsilon_{biax} = \pi_{biax}\frac{E}{1-\nu}\varepsilon_{biax}, \tag{7.14}$$

where the quantity $E/(1-\nu)$ is a constant, independent of crystal-direction. The elastoresistance coefficients are plotted vs crystal direction in Fig. 7.35 and are tabulated for the <100> and <110> directions in Table 7.8.

The above discussion provides the piezoresistance and elastoresistance coefficients for the typical case of zero stress in the z-direction, normal to the sample surface. For the more general case case of non-zero stress, σ_z, and strain, ε_z, in the z-direction, Eqn. 7.8 becomes

$$\Delta\rho/\rho_o = \pi_\ell\sigma_\ell + \pi_t\sigma_t + \pi_z\sigma_z. \tag{7.15}$$

Similarly, Eqn. 7.12 becomes

$$\Delta\rho/\rho_o = m_{\ell,general}\varepsilon_\ell + m_{t,general}\varepsilon_t + m_{z,general}\varepsilon_z, \tag{7.16}$$

and Eqn. 7.13 becomes

$$m_{\ell,general} = \frac{E}{(1+\nu)(1-2\nu)}\left[(1-\nu)\pi_\ell + \nu\pi_t + \nu\pi_z\right], \tag{7.17a}$$

Material	resistivity	π_{11} (10^{-11} Pa^{-1})	π_{12} (10^{-11} Pa^{-1})	π_{44} (10^{-11} Pa^{-1})
n-Si	11.7 Ω-cm	-102.2	+53.4	-13.6
p-Si	7.8 Ω-cm	+6.6	-1.1	+138.1

Table 7.6: Piezoresistance constants of silicon at 298 K from the literature. The silicon is lightly doped, as indicated by the listed resistivity [178].

Material	crystal-direction	π_L (10^{-11} Pa^{-1})	π_t (10^{-11} Pa^{-1})	π_{biax} (10^{-11} Pa^{-1}) $=\pi_L+\pi_t$
n-Si	<100>	-102.2	+53.4	-48.8
	<110>	-31.2	-17.6	
p-Si	<100>	+6.6	-1.1	+5.5
	<110>	+71.8	-66.3	

Table 7.7: Calculated piezoresistance coefficients of n-type and p-type silicon for biaxially-asymmetric or symmetric stress in the <100> or <110> crystal directions of the (001) film surface plane.

Material	crystal-direction	m_L ($\%^{-1}$)	m_t ($\%^{-1}$)	m_{biax} ($\%^{-1}$) $= m_L + m_t$
n-Si	<100>	-123.3	+35.2	-88.1
	<110>	-54.8	-33.2	
p-Si	<100>	+8.9	+1.0	+9.9
	<110>	+114.6	-104.6	

Table 7.8: Calculated elastoresistance coefficients of n-type and p-type silicon for biaxially-asymmetric or symmetric stress in the <100> or <110> crystal directions of the (001) film surface plane. The elastoresistance units are per percentage strain.

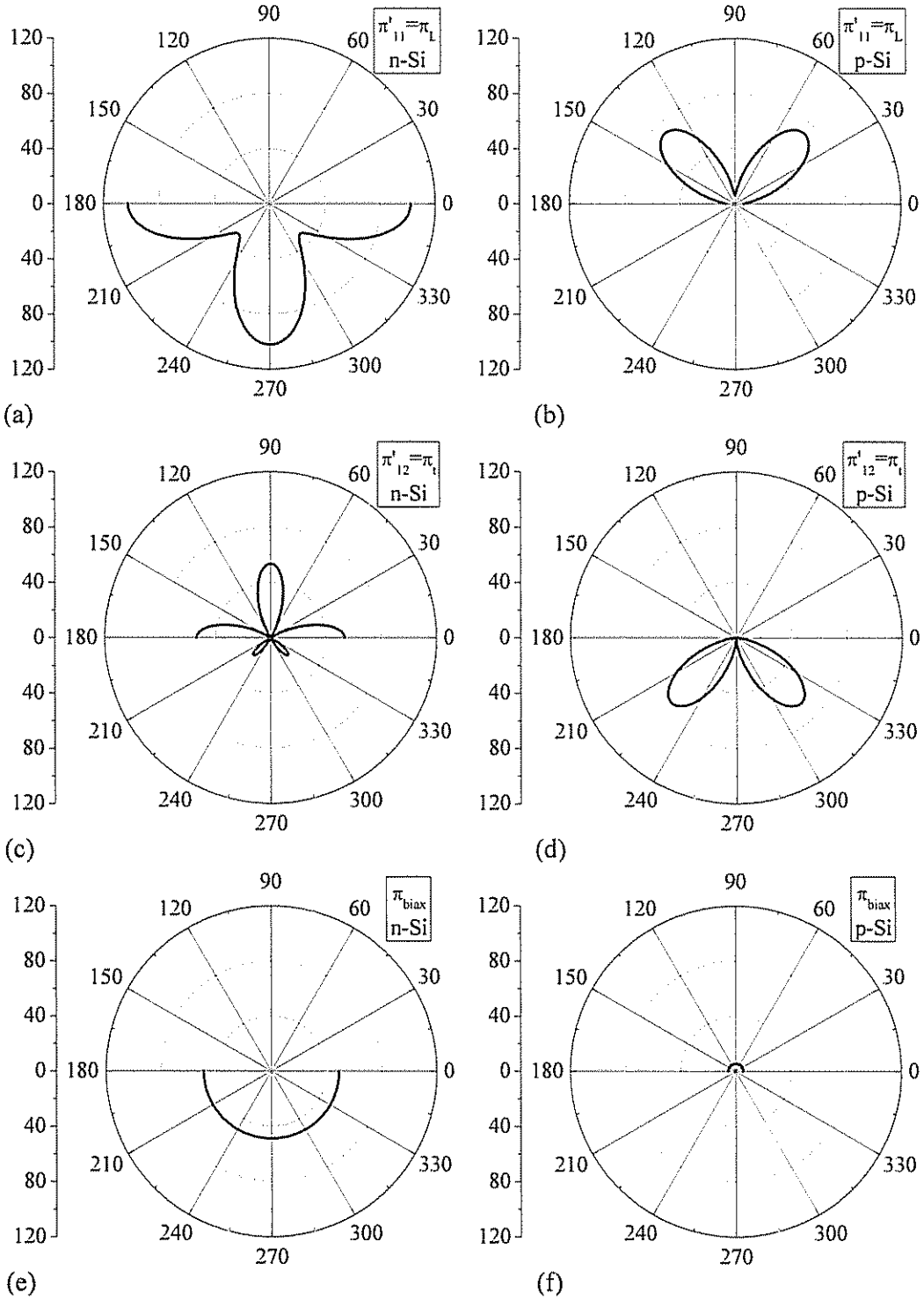


Figure 7.34: Piezoresistance coefficients (a, b) $\pi'_{11}=\pi_L$, (c, d) $\pi'_{12}=\pi_t$, and (e, f) $\pi_{biax}=\pi_L+\pi_t$, for n-type (a, c, e) and p-type (b, d, f) silicon at 298 K, in units of 10^{-11} Pa^{-1}. after Ref. [188] and [196]. The values are plotted for 0-180°: positive values are shown in the top half while negative values are shown in the bottom half of the polar plot.

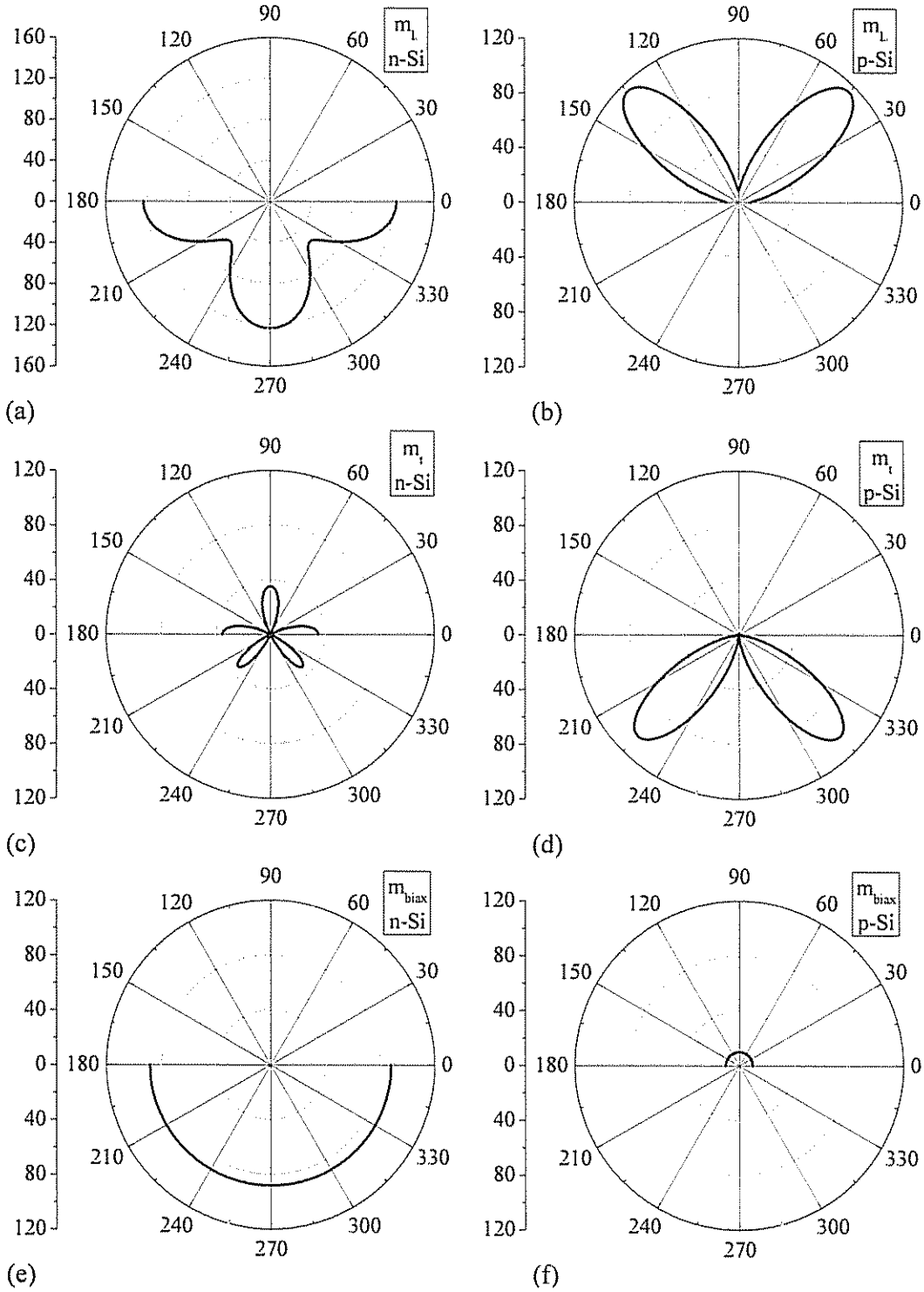


Figure 7.35: Elastoresistance coefficients (a, b) $m_{uni,parallel}$, (c, d) $m_{uni,perpendicular}$, and (e, f) $m_{biaxial}$, for n-type (a, c, e) and p-type (b, d, f) silicon at 298 K in units of $\%^{-1}$. The values are plotted for 0-180°: positive values are shown in the top half while negative values are shown in the bottom half of the polar plot. Note the different radial axis in (a).

$$m_{t,general} = \frac{E}{(1+\nu)(1-2\nu)}\left[\nu\pi_t + (1-\nu)\pi_t + \nu\pi_z\right] \text{ and} \tag{7.17b}$$

$$m_{z,general} = \frac{E}{(1+\nu)(1-2\nu)}\left[\nu\pi_t + \nu\pi_t + (1-\nu)\pi_z\right]. \tag{7.17c}$$

For cubic crystals with an (001) surface plane $\pi_z = \pi_{11}$.

The mobility of a layer is directly related to the layer's conductivity, which is inversely proportional to its resistivity. Thus, the fractional change in mobility due to piezoresistance is

$$\frac{\Delta\mu}{\mu_o} = -\frac{\Delta\rho/\rho_0}{1+\Delta\rho/\rho_0}. \tag{7.18}$$

When the fractional change is small ($\Delta\rho/\rho_0 << 1$), Eqn. 7.18 can be approximated as

$$\frac{\Delta\mu}{\mu_o} \approx -\frac{\Delta\rho}{\rho_0}. \tag{7.19}$$

A tensile stress or strain (σ, $\varepsilon > 0$) is predicted to result in mobility enhancement when the corresponding π or m value is negative. Conversely, a positive π or m value predicts mobility enhancement for compressive stress or strain (σ, $\varepsilon < 0$). Using Eqns. 7.8, 7.12 and Tables 7.7 and 7.8, the mobility enhancement under various types of strain can be predicted.

Inspecting Tables 7.7 and 7.8, the motivation behind Intel's work on uniaxial compression for hole mobility enhancement is clear: the m_t and π_t values for <110> p-type silicon are quite large, leading to significant hole mobility enhancement with uniaxial stress or strain along the channel direction. For 600 MPa of uniaxial compressive stress, the hole mobility is predicted to increase by 40%. The two electron mobility enhancement cases discussed in Ch. 2 are also predicted by piezoresistance. For biaxial tensile strain, a 0.8% strain (equivalent to strained silicon grown on a relaxed $Si_{0.8}Ge_{0.2}$ buffer) should result in 70% electron mobility enhancement according to the piezoresistance theory. Similarly, Intel's success using a nitride capping layer to introduce small uniaxial tensile stress along the <110> nFET channel, resulting in smaller $I_{D,sat}$ increases is expected from piezoresistance: a 320 MPa stress should result in a 10% mobility increase.

Clearly the piezoresistance theory can provide a good estimate of the mobility enhancement expected from various types of uniaxial and biaxial strain. More complicated theoretical models that depict band shifts, splits and bending undoubtedly provide more accurate predictions of mobility enhancement (as well as insight into the physical mechanisms driving the changes in carrier transport, as discussed in Ch. 2). However, linear piezoresistance has great power in its very simplicity: the relative benefit of a wide variety of stress/strain configurations can be easily compared. Specifically, the effects of the crystal-direction and stress/strain direction relative to the electric field and electric current are readily inspected. Later in this chapter, mobility enhancements for a number of different such strained-silicon configurations will be measured and compared to piezoresistance theory.

7.3.2 Measuring Mobility in Thin SOI Devices

To obtain the charge carrier mobility in MOSFETs, typically the drain current (I_D) – gate-source voltage (V_{GS}) characteristic is used. A typical measured I_D-V_{GS} characteristic for an n-MOSFET device with W/L=15 μm / 5 μm is shown in Fig. 7.36a. The device is well behaved with low off-current (less than 1 pA), sharp turn on (142 mV/dec), and strong on-current (84 μA at V_{GS}=+8V). The I_D-V_{GS} relationship in an ideal MOSFET operating in the linear region is given by:

$$I_{D,linear} = \mu_{eff,linear} \frac{W}{L} C'_{ox} (V_{GS} - V_T) V_{DS}, \tag{7.20}$$

where $\mu_{eff,\,linear}$ is the effective linear device mobility, W and L are the transistor width and length, C'_{ox} is the gate capacitance per unit area, V_{DS} is the drain-source voltage and V_T is the threshold voltage. The transconductance of the device, g_m, plotted in Fig. 7.36c, is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \tag{7.21}$$

For the device of Fig. 7.36, the linear transconductance reaches a maximum of 1.23×10^{-5} A/V at V_{GS}=+0.1V.

From Eqn. 7.20, it is clear that in the linear region the drain current should be linearly related to V_{GS} via a constant that is proportional to the mobility of charge carriers

in the channel. Thus, using a linear plot of $I_{D,linear}$ vs V_{GS}, the mobility can be calculated from the observed slope, and the threshold voltage from the x-intercept. The I-V characteristic plotted in Fig. 7.36a on semi-log axes is re-plotted on linear axes in Fig. 7.36b. A linear fit to the I-V data, indicated by the thin solid line, is performed on the data in the range of 2±0.5 volts beyond the maximum transconductance, *e.g.*, for this device, from 1.6 to 2.6 V. From this linear fit a mobility 329 $cm^2V^{-1}s^{-1}$ and a threshold voltage -0.97 V are extracted.

However, looking closely at Fig. 7.36b, the current-voltage relationship is not quite linear with V_{GS}. At high currents the current is less than that predicted by the linear relationship of Eqn. 7.20. This is because the ideal MOSFET equation given by Eqn. 7.20 ignores two important effects. First, the dependence of mobility on V_{GS}, that is, on the vertical electric field, has been omitted. This well-known effect can be observed in Fig. 7.36c in the decrease of transconductance as V_{GS} increases. In order to account for the mobility's vertical-field dependence, the form $\frac{\mu_o}{1+\theta(V_{GS}-V_T)}$ is substituted for the linear mobility term in Eqn 7.20, where θ is the mobility reduction factor (an unknown constant) and μ_o is the charge carrier mobility in the linear regime.

Second, the source-drain resistance, R_{SD}, has been neglected. For the thin SOI devices made in this work, the relatively high source-drain resistance compared to bulk silicon devices reduces the effective drain-source voltage seen by the channel compared to the applied V_{DS} value. In Sec. 7.2.1 the average film resistance for nFETs was measured to be 410 Ω/□. For the W/L=15 μm / 5 μm devices shown in Fig. 7.36, the total source-drain resistance (corresponding to 0.67 squares) is 273 Ω. Thus for a current of 80 μA, the source-drain resistance consumes 22 mV of the 100 mV applied across the device under test, so that the actual source-drain voltage at the inner transistor nodes is reduced to 78 mV. This is a significant reduction, and must be accounted for in the I-V analysis to obtain correct mobility values. So, the model drawn in Fig. 7.37 is adopted, with a total source-drain resistance, R_{SD}, split on the source and drain sides.

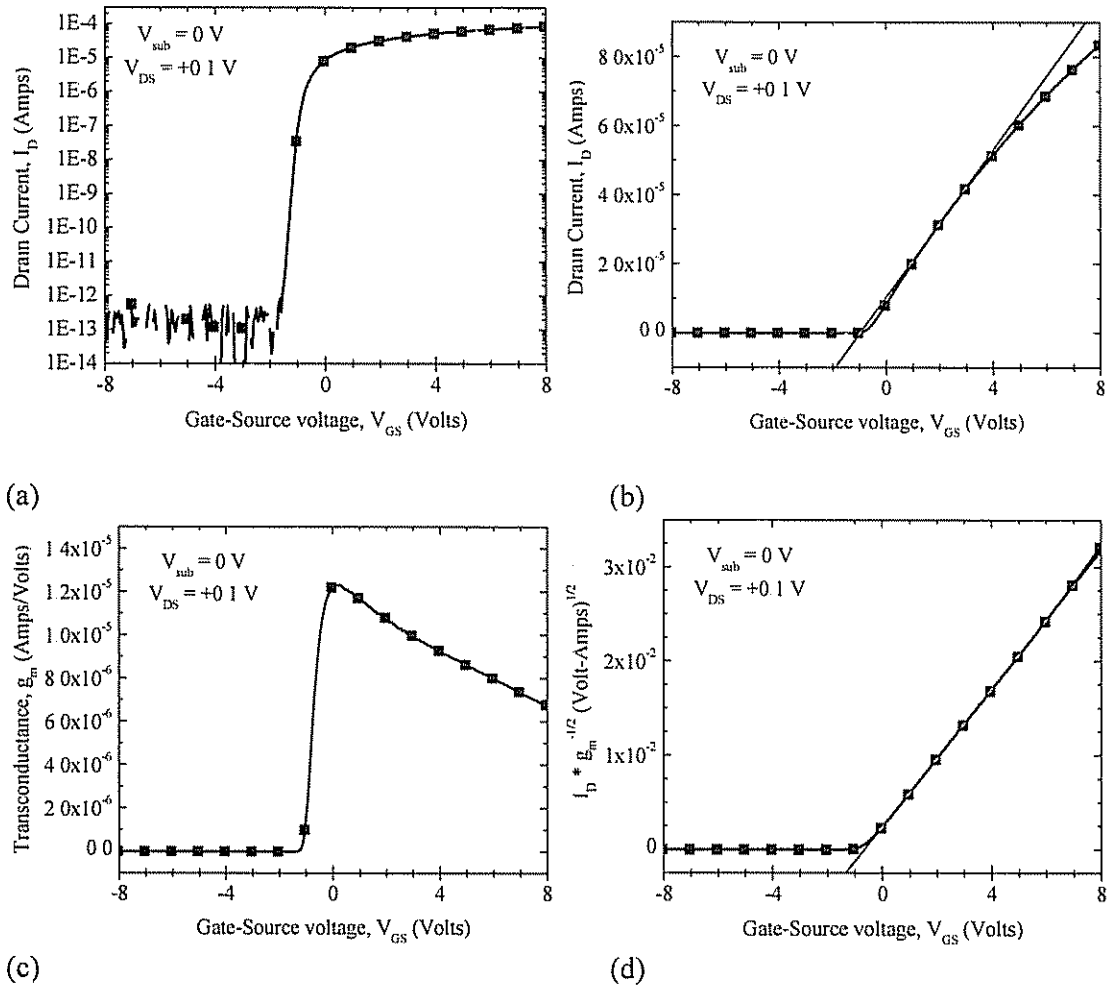


Figure 7.36: Transistor characteristics for an n-MOSFET: (a) Drain current vs gate voltage, semi-log plot; (b) Drain current vs gate voltage, linear plot; (c) transconductance vs gate voltage; and (d) drain current divided by the square root of transconductance (Eqn. 7.23) vs gate voltage. The devices has SiO_2/SiN_x barrier layers (after Fig. 7.5d), and W/L = 15 μm / 5 μm on unstrained silicon (originally 300-μm x 300-μm islands) aligned to the <110> crystal directions. The measurement was taken with V_{DS} = +0.1 V and V_{sub} = 0 V.

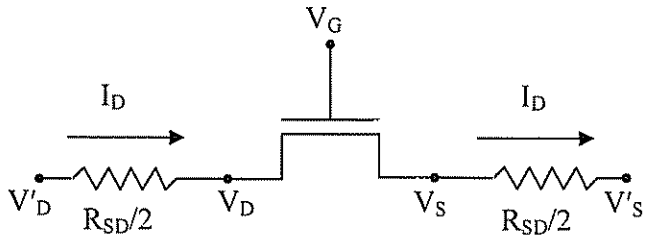


Figure 7.37: Model of an ideal MOSFET plus source and drain resistances of $R_{SD}/2$. The primed voltages V'_D and V'_S indicate measured quantities, while the unprimed ones (V_D, V_S) indicate voltages at the internal transistor nodes.

Accounting for gate-voltage dependent mobility and the source-drain resistance, Eqn. 7.20 becomes

$$I_{D,linear} = \frac{\mu_o}{1+\theta(V_{GS}-V_T)}\frac{W}{L}C_{ox}'(V_{GS}-V_T)(V_{DS}'-I_{D,linear}R_{SD}), \tag{7.22}$$

where V'_{DS} is the applied drain-source voltage. In Eqn. 7.22 the effect of the source-drain resistance on the gate-source voltage has been neglected. This approximation is justified because the gate-source voltages of interest are at least an order of magnitude greater than V_{DS} and thus are trivially reduced by the source resistance.

This revised model of the transistor given by Eqn. 7.22 shows a non-linear dependence of drain current on gate voltage. In order to extract the mobility [175], the ratio of the drain current to the square root of transconductance, $I_{D,linear}g_{m,linear}^{-1/2}$ is therefore used:

$$\frac{I_{D,linear}}{\sqrt{g_{m,linear}}} = (V_{GS}-V_T)\sqrt{\mu_o\frac{W}{L}C_{ox}'V_{DS}'}. \tag{7.23}$$

This function is conveniently linearly dependent on the gate-source voltage, with the slope proportional to the square root of mobility and the x-intercept equal to the threshold voltage. Note that Eqn. 7.23 is not dependent on either the source-drain resistance nor on the value of θ. Thus by calculating $I_D g_m^{-1/2}$ from the measured I-V characteristics in the linear region, the source-drain resistance and first-order V_{GS} mobility dependence can both be eliminated, and the charge carrier mobility, μ_o, and threshold voltage, V_T, can be obtained.

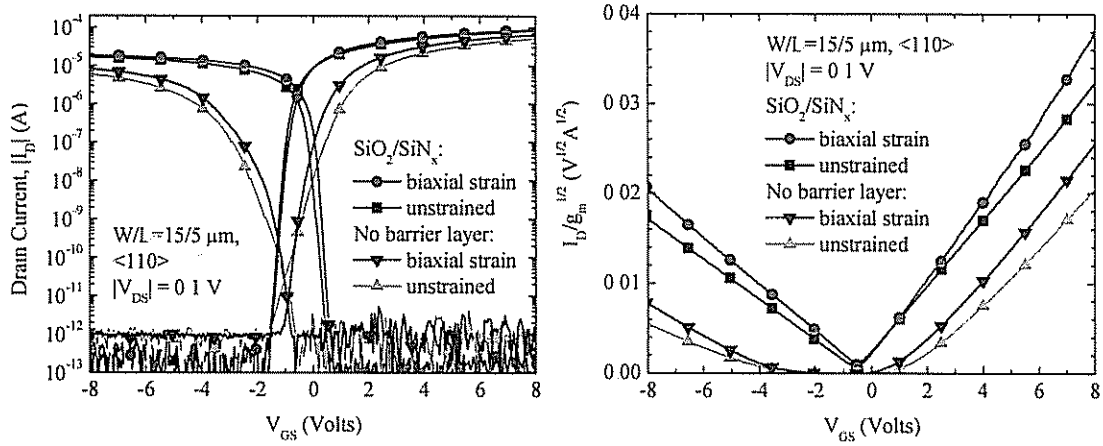
In Fig. 7.36d, the measured ratio of the drain current to the square root of transconductance is plotted. The thin line shows the linear fit, again performed around the point two volts beyond the maximum transconductance, which almost completely overlaps the measured data. The linear fit shown in Fig. 7.36d of the I-V data to Eqn. 7.23 is very good throughout the plotted voltage range, showing the validity of the two corrections made to Eqn. 7.20. The extracted mobility is $\mu_{o,\,linear}$=414 $cm^2V^{-1}s^{-1}$ and the threshold voltage is V_T=-0.65 V. For the upcoming sections, device mobility will be obtained from measured I-V characteristics by linearly fitting $I_D g_m^{-1/2}$ as described above.

7.3.3 Electron and Hole Mobility Enhancement due to Biaxial Strain

By using large (300 x 300 μm^2) and small (30 x 30 μm^2) square islands on the same sample, the effect of biaxial tensile strain on hole and electron mobility has been measured. Typical I-V characteristics measured with $|V_{DS}|$=0.1V are shown in Fig. 7.38a for devices with W/L=15/5 $\mu m/\mu m$. Measurements for two samples are shown: for the BPSG-only sample (Fig. 7.5a) and for the sample with a SiO_2/SiN_x barrier layer (Fig. 7.5d). In both cases, the transistors are aligned to the <110> crystal direction, as in standard CMOS processes. The I-V curves of Fig. 7.38a show that both strained and unstrained devices are well-behaved, with no significant strain dependence of the threshold voltage, sub-threshold slope, or off-current.

In Fig. 7.38b the function $I_D \cdot g_m^{-1/2}$ is plotted as calculated for the measured I-V curves shown in Fig. 7.38a. The increased slopes of $I_D \cdot g_m^{-1/2}$ for biaxially-strained n- and p-FETs, indicate that both samples have significantly enhanced electron and hole mobility due to biaxial tensile strain. Average mobilities extracted using Eqn. 7.23 from measurements of many devices with L = 5 μm and W = 10 - 60 μm are tabulated in Table 7.9 along with Raman-measured strain. The devices with no barrier layer show a 44% electron mobility enhancement, from 290 to 418 $cm^2V^{-1}s^{-1}$ and 55% hole mobility enhancement, from 67 to 104 $cm^2V^{-1}s^{-1}$, for biaxial strain of +0.52%. Transistors made on substrates with SiO_2/SiN_x barrier layers to BPSG exhibit similar mobility enhancements due to biaxial tensile strain and higher overall mobilities, due to the improved back channel interface and reduced BPSG out-diffusion as described in Sec. 7.2.3. N-FETs on SiO_2/SiN_x barrier layers have a mobility of 416 with zero strain and 543 $cm^2V^{-1}s^{-1}$ (a 31% increase) with +0.38% biaxial strain, while pFETs show a 30% increase from 177 to 230 $cm^2V^{-1}s^{-1}$ when 0.45% biaxial tensile strain is introduced. The BPSG only and SiO_2/SiN_x barrier layer samples have different biaxial strain levels due to different Si and SiGe thicknesses, and to the barrier layers which share the force balance with the Si/SiGe bi-layer [161], reducing the final silicon strain. Because the samples have different silicon strains, it is expected that they will exhibit slightly different mobility enhancements.

The electron mobility enhancements measured here for BPSG-only and SiN_x/SiO_2 barrier layer samples (listed in Table 7.9) and those of previous work [8,161] are plotted as a function of strain using symbols in Fig. 7.39. Also shown are the bulk



(a) (b)

Figure 7.38: (a) I-V characteristics and (b) $I_D \cdot g_m^{-1/2}$ for nFET and pFET transistors with zero and biaxial strain. The transistors have W/L=15/5 μm/μm, $|V_{DS}|$=0.1V, and are aligned to <110>. Data are shown for two samples: BPSG only and SiO_2/SiN_x barrier layer. Both samples show significantly enhanced electron and hole mobility.

type	sample	μ_{zero}	ε_{zero}	μ_{biax}	ε_{biax}	μ increase
n-Si	SiO_2/SiN_x/BPSG	416±21	0.00%	543±13	0.38%	+31%
	BPSG only	290±14	0.02%	418±15	0.52%	+44%
p-Si	SiO_2/SiN_x/BPSG	177±17	0.02%	230±25	0.45%	+30%
	BPSG only	67±7	0.01%	104±9	0.52%	+55%

Table 7.9 Average nFET and pFET mobilities ($cm^2V^{-1}s^{-1}$) under zero or biaxial tensile strain. For each sample and strain type, at least six different transistors were measured and the average and standard deviation of mobility tabulated. The mobilities reported here and in subsequent tables are calculated using Eqn. 7.23. Raman measurement error for biaxial strain is ±0.06%.

piezoresistance model of Sec. 7.3.1, and the well-accepted phonon-limited model of Ref. [42]. (The model has been favorably compared to experimental data in the literature; see the review in Sec. 2.2.2.) The two models generally predict similar levels of mobility enhancements in the low strain region (< 0.7% biaxial strain) where the piezoresistance theory is valid, and the measured results agree well with the theory.

The hole mobility enhancement vs strain is plotted in Fig. 7.40 for the six-band k·p model of Ref. [58] and for the bulk piezoresistance theory described above. The quantum model has been shown to agree qualitatively with experimental measurements, at least at low vertical electric fields; see the discussion in Sec. 2.3.1. Here, the piezoresistance and quantum theory predictions do not agree, because the piezoresistance model treats bulk strained silicon, while the k·p model accounts for the 2-D hole inversion channel layer. For the case of hole transport in a strained-silicon MOSFET inversion layer, the piezoresistance theory does a poor job of predicting hole mobility enhancement [190]. The symbols of Fig. 7.40 indicate the transistor results measured here (for the BPSG-only and SiN_x/SiO_2 barrier layer samples tabulated in Table 3.9), which are in good agreement with the quantum theory model prediction. The results presented here may differ from other published work (showing higher hole mobility enhancements) because the gate oxide is deposited, not thermally grown, as is typical, in order to reduce the thermal budget and maintain the desired silicon strain. The gate oxidation process is modified by, and itself modifies the surface roughness at the channel / oxide interface. Since surface roughness is strongly correlated with charge carrier mobility, particularly at high vertical electrical fields, the deposited gate oxide used in this work may modify the mobility results in unexpected ways.

Transistor measurements on strained-silicon films on BPSG, obtained by the methods discussed previously in this work, have shown that both electron and hole mobility are enhanced by biaxial tensile strain, in samples both with and without barrier layers. The measurement results agree well with piezoresistance theory for electrons, whereas for holes the bulk piezoresistance theory is insufficient, and a more detailed quantum theory is needed to explain the observed hole mobility enhancement. In the following sections, electron and hole mobility enhancement for various types of uniaxial strain will be measured and compared to the piezoresistance theory of Sec. 7.3.1.

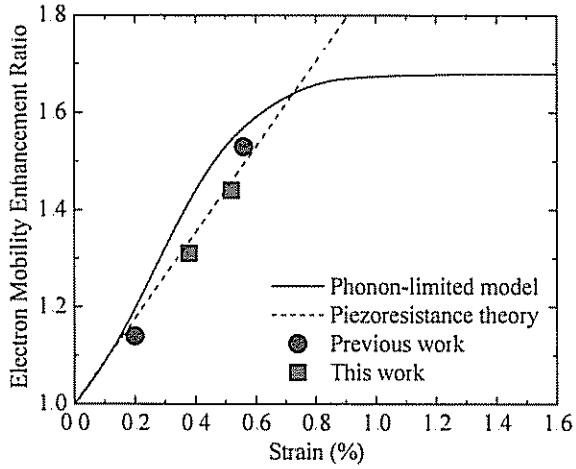


Figure 7.39: Electron mobility enhancement due to biaxial tensile strain from the phonon-limited model of Ref. [42] at 300K with sheet electron inversion charge density of n_S=10^{12} cm^{-2}, from bulk piezoresistance theory (Eqn. 7.14), and measured results in this and previous [161] work.

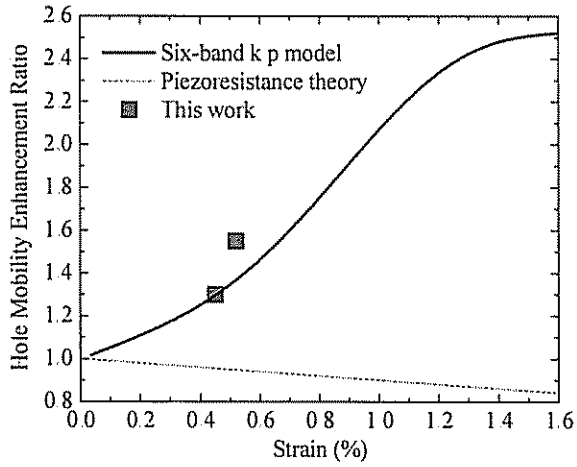


Figure 7.40: Hole mobility enhancement due to biaxial tensile strain from a six-band k·p model from Ref. [58] at 300K with sheet electron inversion charge density of n_S=10^{12} cm^{-2}, from bulk piezoresistance theory (Eqn. 7.14), and from measured results presented in this work.

7.3.4 Uniaxial-strain Induced Electron Mobility Enhancement

Earlier in this thesis it was seen that after patterning Si/SiGe islands of various shapes and sizes, by force balance and the Poisson effect one can obtain silicon film mesas with zero strain, biaxial strain and uniaxial strain on the same SOI sample. In the previous section, biaxial strain made in this fashion was shown to enhance electron and hole mobility in n- and p-channel MOSFETs, compared to neighboring transistors made on unstrained silicon. In this section and the next, the enhancement of electron and hole mobility due to the introduction of uniaxial strain will be measured and discussed.

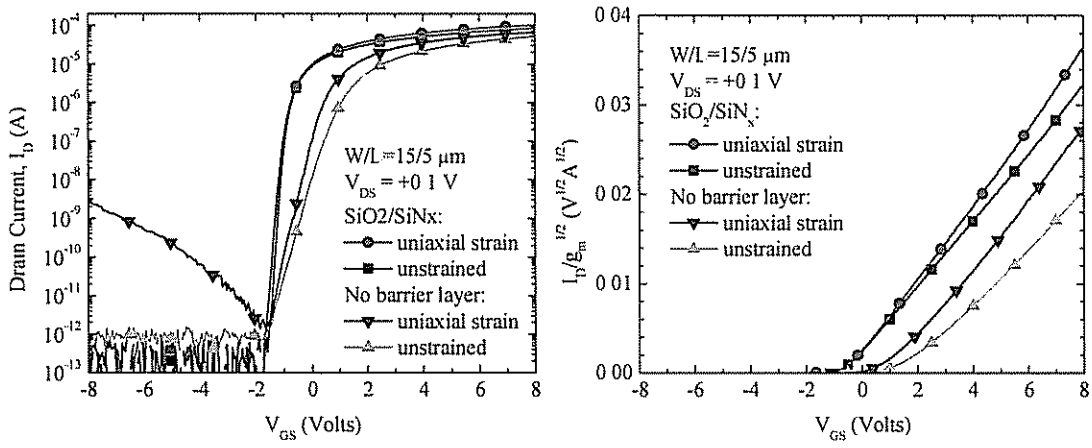
The bulk piezoresistance theory summarized by Eqn. 7.12 and Table 7.8 predicts that electron mobility will be enhanced under certain types of uniaxial strain. The crystal-direction of the channel and the channel's orientation relative to the uniaxial strain determine whether the electron mobility is increased or decreased due to the addition of uniaxial tensile strain. Specifically, the largest value of m in Table 7.8 for n-type silicon is $m_{L,\,<100>}$, so the strongest beneficial effect of tensile strain on mobility when $\sigma_{zz}=0$ should be seen for transistors aligned to the <100> crystal direction, with current flow in the channel *parallel* to the uniaxial strain. Alternately, for a channel aligned *perpendicular* to a <100> uniaxial strain, the positive value of $m_{t,\,<100>}$ indicates that the mobility is expected to decrease under uniaxial tensile strain. For transistors aligned to the <110> crystal direction, a positive but weaker tensile strain-mobility correlation is expected, regardless of whether the channel is parallel and perpendicular to the strain direction.

Using the fabrication scheme shown in Fig. 7.6, n-MOSFETs with uniaxial tensile strain were fabricated alongside the biaxially-strained and unstrained silicon devices discussed above. The uniaxial strain was aligned to <110> (Fig. 7.6c,d) or <100> (Fig. 7.6e,f), with channel directions parallel (Fig. 7.6c,e) or perpendicular (Fig. 7.6d,f) to the strain, in order to investigate all four cases described above.

First, the most promising case of nFET transistor channels aligned parallel to a <100> uniaxial tensile strain will be examined. Typical measured I-V curves from such transistors are shown in Fig. 7.41a for devices with SiO_2/SiN_x barrier layers and devices with no barrier layers. As in the case of biaxial strain, the uniaxial strain does not appreciably shift the threshold voltages or sub-threshold slopes of the curves. The high

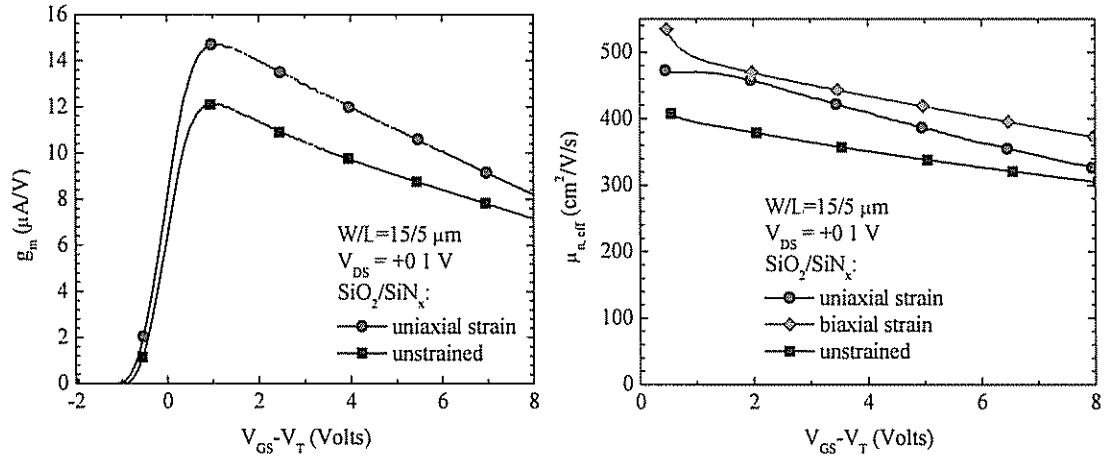
off current observed for the uniaxially strained nFET on BPSG is anomalous for this device and is not a strain-related effect. The function of Eqn. 7.23 is plotted for this I-V data in Fig. 7.41b, and from these plots the electron mobilities are extracted. For both samples, the uniaxial strain significantly enhances the electron mobility. For these particular devices, with no barrier layer to BPSG the mobility is increased from 312 to 452 $cm^2V^{-1}s^{-1}$ (+45%) for a uniaxial strain of ~0.57%, while with SiO_2/SiN_x barrier layers the mobility is increased from 414 to 510 $cm^2V^{-1}s^{-1}$ (+23%) for a uniaxial strain of ~0.53%. The calculated transconductance curves of uniaxially-strained and unstrained devices with the SiO_2/SiN_x barrier layers are plotted Fig. 7.42a. The maximum transconductance is increased by the addition of uniaxial strain from 12.3 to 14.8 μA/V, an increase of 20%. Note that the 20% increase in transconductance generally agrees with the extracted mobility increase of 23%. At higher gate voltages the strain still increases the transconductance, but by a lesser factor: at $V_{GS}-V_T=+8V$ the transconductance change due to uniaxial strain is 7.1 to 8.2 μA/V, an increase of 16%. For comparison with biaxially-strained devices, in Fig. 7.42b the effective mobility (calculated from measured I-V curves using Eqn. 7.20) is plotted for the biaxially- and uniaxially-strained <100> nFETs characterized in Figs. 7.38 and 7.41. As expected from the mobilities extracted using Eqn. 7.23 discussed above, the biaxially-strained channel exhibits the highest electron mobility. Notably, the electron mobility enhancement in the uniaxially-strained device degrades more quickly as the gate overdrive voltage ($|V_{GS}-V_T|$) increases, compared to the biaxially-strained and unstrained silicon devices. Uniaxially-strained devices show good drain current – drain voltage (I_D-V_D) characteristics, as shown in Fig. 7.43 for a sample with BPSG only. The saturated drain current, $I_{D,sat}$, increases due to uniaxial strain. At $V_{DS}=+4V$ and $V_{GS}-V_T=3V$, $I_{D,sat}$ increases from 349 μA for unstrained devices to 477 μA on uniaxially strained devices, an increase of 37%. These curves were measured on a sample with uniaxial strain of 0.68%, and thus the $I_{D,sat}$ increase is greater than the mobility and transconductance increases observed above for $\varepsilon_{uni}=$~0.55%.

In summary, when uniaxial tensile strain is present in the <100> crystal direction and nFET transistor channels are aligned parallel to the strain, significant increases in electron mobility, transconductance and saturation current are obtained, compared to unstrained nFETs fabricated side-by-side on large square islands on the same sample. The



(a) (b)

Figure 7.41: (a) I-V characteristics and (b) $I_D \cdot g_m^{-1/2}$ for nFET transistors with zero and uniaxial strain. The uniaxial strain is along the <100> crystal direction, parallel to the direction of current flow in the channel. The transistors have W/L=15/5 μm/μm and V_{DS}=+0.1V. Data are shown for two samples: BPSG only and SiO_2/SiN_x barrier layer. Both samples show enhanced electron mobility.



(a) (b)

Figure 7.42: (a) Transconductance, g_m, and (b) effective mobility, μ_{eff}, vs gate voltage minus the threshold voltage, V_{GS}-V_T, for nFET transistors with zero and uniaxial strain and, in (b), biaxial strain. The uniaxial strain is along the <100> crystal direction, parallel to the direction of current flow in the channel. The transistors have W/L=15/5 μm/μm and V_{DS}=+0.1V. Data are shown for a sample with SiO_2/SiN_x barrier layers. The biaxial-strained induced enhancement of effective mobility persists at high gate voltages, but the uniaxial-strain induced enhancement decreases in magnitude as V_{GS} increases.

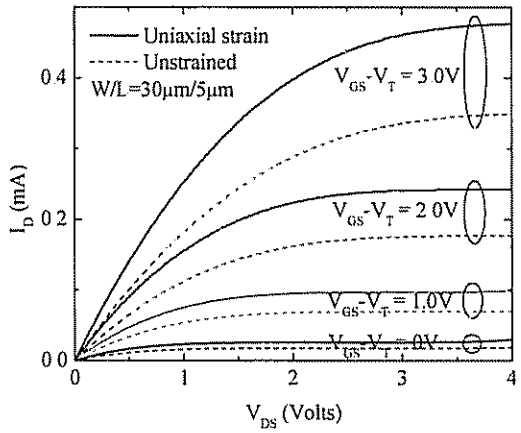


Figure 7.43: Typical drain current – drain voltage (I_D-V_D) characteristics for uniaxially-strained and unstrained n-channel MOSFET transistors with W/L=30/5 μm/μm aligned to the <100> crystal-direction on samples with no barrier layer (BPSG only). These devices were made in a separate run than the others presented in this section under slightly different conditions and thus have a higher uniaxial strain of 0.68%.

effect of uniaxial strain is consistent for devices with and without barrier layers. The uniaxially-strained devices are well-behaved, with no major changes in threshold voltages or sub-threshold slopes compared to the unstrained devices. Moreover, examination of the transconductance and effective mobility vs gate voltage (Fig. 7.42a,b) indicates that the strain-induced electron transport enhancement persists (albeit at reduced levels) at high vertical electrical fields. We believe this to be the first report of electron mobility enhancement in <100> uniaxially-strained silicon channels.

The average measured mobilities under various types of uniaxial strain are given in Table 7.10. As has already been seen, <100> strain alignment parallel to the channel yields average mobility increases of 24% (with SiO_2/SiN_x barrier layers) and 38% (with no barrier layers). The piezoresistance theory of Eqn. 7.12 and Table 7.8, however, predicts much higher increases of 65% and 70%, respectively. The lower levels of mobility enhancement observed may be due to the limits of bulk piezoresistance theory in describing electron transport in uniaxially-strained inversion layers, or to the failure of the piezoresistance theory to apply to highly strained layers, such as were used in this work, or to a physical effect that mitigates the strain-induced mobility enhancement in these uniaxially-strained silicon transistors.

NFET transistors with different crystal and strain/channel alignments were also well-behaved. The threshold voltage, sub-threshold slope and off current do not change appreciably from transistors of one strain type (or direction) to another, as has already been shown for the biaxial and uniaxial <100> "parallel" strain cases. Table 7.10 summarizes the measured electron mobility enhancements. For transistors with <110> strain parallel to the channel, piezoresistance predicts a moderate mobility enhancement, here ~30%, about half the strength of that predicted for the <100> parallel case. Instead, enhancements are observed that are at least as strong as the <100> case. With SiO_2/SiN_x barrier layers, transistors aligned to <110> with the channel and strain parallel show a 23% mobility enhancement, while devices with no barrier layer show a remarkable 72% electron mobility enhancement. Electron mobility enhancement due to uniaxial stress or uniaxial strain parallel to a <110> channel has been observed by Intel [4,5] and other researchers [69,77-79,81].

sample	channel alignment	ε_{uni}	$\mu_{longitudinal}$	μ increase	$\mu_{transverse}$	μ increase
SiO_2/SiN_x/BPSG	<100>	~0.6%*	515±4	+24%	435±17	+4.6%
	<110>	0.53%	512±5	+23%	445±8	+7.0%
BPSG only	<100>	~0.6%*	399±77	+38%	330±12	+14%
	<110>	0.57%	498±19	+72%	323±19	+11%

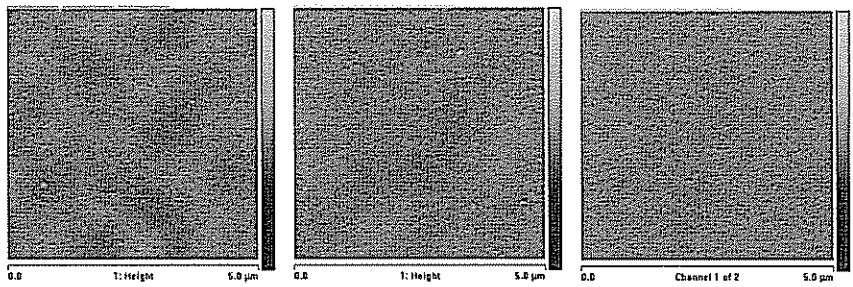
Table 7.10 Average nFET mobilities ($cm^2V^{-1}s^{-1}$) under zero or uniaxial strain. For each sample and strain type, at least three different transistors were measured. The mobility enhancements are calculated vs the unstrained values given in Table 7.9. Raman measurement error for uniaxial strain is ±0.12%. For islands with uniaxial strain aligned to [100], the channels are in the [100] (longitudinal) or [010] (transverse) directions. For uniaxial strain aligned to [110], the channels are in the [110] (longitudinal) or [$1\bar{1}0$] (transverse) direction. *The strain in <100> channels was not measured, but should be slightly higher than that in <110> channels, as discussed in Sec. 5.2.1.

Transistor with channels aligned *perpendicular* to the uniaxial strain show very slight mobility enhancements of 5-14%. Note typical process variations across a control nFET sample cause mobility variance of approximately ±10%, so it is difficult to draw firm conclusions from these small changes. The piezoresistance theory predicts that devices aligned to the <100> direction with the strain and channel perpendicular should show a ~20% decrease in mobility, while those aligned to <110> should show a ~20% increase. Changes of this magnitude should be observable, and they are not found in our measurements. A survey of the literature shows conflicting results. Using mechanically-induced uniaxial strain perpendicular to a <110> silicon nFET channel, Zhao, *et. al.* [81] observed an $\pi_{t,<110>}$ value of -16 to -25 $x10^{-11}$ Pa^{-1}, close to the predicted value of -18 $x10^{-11}$ Pa^{-1} (Sec. 7.3.1), while Wang, *et. al.* [79] observed a negligibly small increase (<1%) in mobility. In both of these references, the authors used low levels (≤0.2%) of uniaxial strain. Using the same strain configuration, Haugerud, *et. al.* [82] observed very large increases in effective mobility and saturation current (+18%) from a very small amount of mechanical tensile strain (+0.05%). The physical cause of this strong mobility increase (possibly aided by a contact or source/drain resistance effect) was not determined. Our results, showing a negligible mobility increase from a large uniaxial strain perpendicular to the nFET channel, seem to agree with Ref. [79]. However, it may be that the piezoresistance theory is simply insufficient to describe electron mobility enhancement in our highly strained layers, or that an unknown effect is at work in these devices to minimize the mobility enhancement when the strain and channel are perpendicular.

One such possible effect is the surface roughness of the silicon film. Surface roughness of a silicon channel at its interface with the (SiO_2) gate dielectric is known [191,192] to reduce the charge carrier mobility in the channel. Fischetti, *et. al.*, [43,193] have proposed that the widely accepted experimental observations of electron mobility enhancement in biaxially-strained silicon cannot be fully attributed to strain effects. Specifically, at high carrier densities, the inversion potential at an SiO_2/unstrained Si channel interface splits the six-fold degenerate conduction band minima and shifts the bands, thus rendering ineffective further energy band shifts due to biaxial or uniaxial strain (as described in Ch. 2). A similar argument was made by Dorda [44], to explain the

gate voltage dependence of π_{11} and π_{12} in silicon. Moreover, at high vertical electric field, the carriers are tightly confined to the interface, and thus are more strongly influenced by its surface roughness compared to the case at low vertical fields. Thus, several recent works [43,46,47] have attributed the mobility enhancement observed at high vertical field in biaxially-strained silicon layers to a smoother SiO_2/Si interface, by comparison of measured FET data and transport models. The decreased surface roughness has also been experimentally measured [48-50] for the case of strained silicon grown on relaxed SiGe buffers, and much work has been done using, for example, chemical mechanical polishing [67] to further reduce the surface roughness.

Our strain generation process does not depend on relaxed SiGe buffers, and thus is immune from this particular source of surface roughness. However, as shown in Ch. 6, the thin silicon films used here can buckle during the lateral expansion process that generates the silicon strain. The buckling amplitude, or surface roughness, increases exponentially with anneal time, as given by Eqn. 6.2. Figure 7.44 shows AFM images of the buckling at the center of the three different island sizes used for devices for a SiGe/Si bilayer with no barrier layers (*i.e.*, sample of Fig. 7.5b) after a 30-min anneal at 800°C. The FET samples were annealed for 45 min at 800°C to generate the desired silicon strain, and thus will be slightly more buckled than the images shown here. The RMS surface roughness is least on the 30-μm x 30-μm biaxially-strained island, 0.60 nm, where due to the islands small size the films can quickly expand to reach stress balance before significantly buckling occurs (Fig. 7.44c). In contrast, on the 300-μm x 300-μm "unstrained" island the buckling pattern is clearly seen in Fig. 7.44a. The measured surface roughness has increased to 0.67 nm because the lateral expansion process has not yet reached the center of the island, and thus buckling dominates the film dynamics there. The 30-μm x 300-μm island used for uniaxial strain shows slight surface roughening of 0.63 nm, in between that of the other two islands (Fig. 7.44b). So, the biaxially-strained island is the flattest, with the uniaxially-strained island slightly flatter than the "unstrained" island. This qualitative trend is also reflected in our mobility data for the sample with SiN_x/SiO_2 barrier layers: the biaxially-strained layers have greater mobilities (543 $cm^2V^{-1}s^{-1}$) than uniaxially-strained layers (435-515 $cm^2V^{-1}s^{-1}$), which in turn have larger mobilities than unstrained layers (416 $cm^2V^{-1}s^{-1}$). Moreover, the uniaxially-strained



(a) (b) (c)

Figure 7.44: Atomic Force Microscopy (AFM) images of the surface of a 30-nm SiGe/25-nm Si bilayer on 235-nm BPSG (Fig. 7.5b) after annealing for 30 min at 800°C, measured at the center of islands: (a) 300 µm x 300 µm; (b) 30 µm x 300 µm aligned to the <100> crystal plane; and (c) 30 µm x 30 µm. The RMS surface roughness for the three scans is: (a) 0.67 nm, (b) 0.63 nm, and (c) 0.60 nm. The AFM scan size is 5x5 μm^2 and the *z*-axis scale is 15 nm. The edges of the images are along <110> planes.

islands exhibit one-dimensional buckles (see Fig. 6.22) and thus the surface roughness effect on carrier transport could be different is the directions parallel and perpendicular to the strain. For the SiN_x/SiO_2 barrier layer sample, channels parallel to uniaxial strain (*i.e.*, with the channel electrons traveling along the 1D buckle troughs and peaks) exhibit mobilities of 512-515 $cm^2V^{-1}s^{-1}$. Compare the much lower mobilities of 435-445 $cm^2V^{-1}s^{-1}$ measured for channels perpendicular to the uniaxial strain (*i.e.*, with the electrons traveling across the 1-D buckling troughs and peaks). Finally, note that this latter trend occurs for both crystal-directions, <100> and <110>, which directly contradicts the expectation of piezoresistance that the two directions should exhibit opposite mobility-strain relationships as discussed earlier. Given these trends, it seems possible that surface roughness, in addition to film strain, is affecting the measured electron mobility.

The conventional understanding indicates that surface roughness can only affect mobility if its correlation length (*i.e.*, the roughness wavelength) is of the order of a few nanometers, near the Fermi wavelength of the charge carriers [192,193]. However, the wavelength of the buckling observed in Ch. 6 is about 1 μm, a factor of 10^3 larger. Such long wavelength surface roughness is not normally expected to have any effect on the mobility. However, recent work [194,195] has shown that roughness with a long correlation length (>100 nm) and significant amplitude (> 3 nm) can also reduce mobility, although the mechanism is not well understood. So, it is proposed that the electron mobility enhancements observed here may be influenced not only by channel strain, but also by buckling-induced long-wavelength surface roughness. Using the buckling mitigation techniques presented in Ch. 6, it should be possible to significantly reduce buckling and thus its influence on mobility; more work is needed on this front.

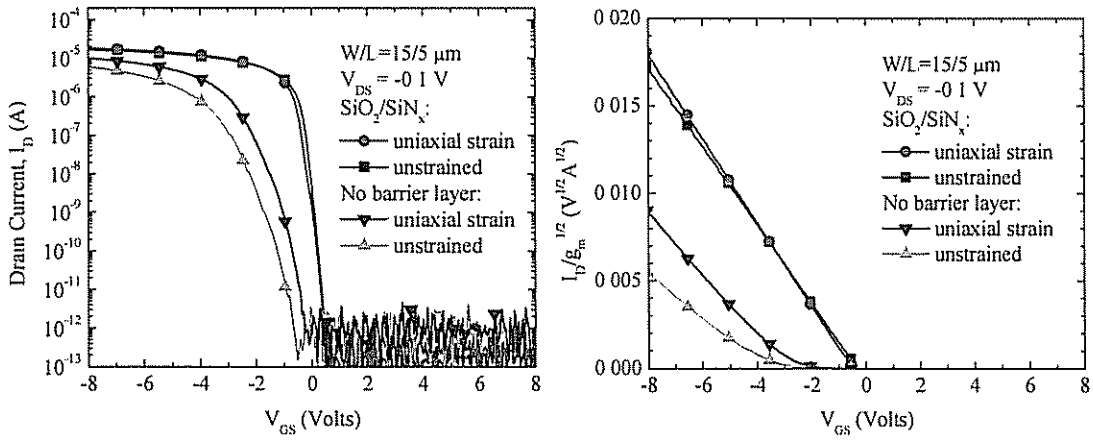
Finally, from piezoresistance (Eqn. 7.12) it is expected that the fractional mobility enhancements due to uniaxial longitudinal and transverse stresses should sum to equal to biaxial-strain induced mobility enhancement. Comparing the data in Tables 7.9 and 7.10, it seems this is true. For the SiO_2/SiN_x barrier layer devices, the sum of the two uniaxial enhancements (longitudinal + transverse) for <100> and <110> are 28.6% and 30.0%, respectively, very close to the 31% enhancement observed for biaxial strain, especially considering that the uniaxial and biaxial strain levels are, of course, slightly different.

To summarize, uniaxial strain on the order of 0.55% in the <100> or <110> crystal directions, parallel to an nFET channel induces significant (20-40%) enhancements of electron mobility, transconductance, and saturation current, which persist up to high vertical electric fields. When the same uniaxial strain is oriented perpendicular to the channel, negligible changes in mobility (< 15%) are observed, regardless of the crystal direction of the channel. The results are consistent for samples with and without SiN_x/SiO_2 barrier layers on the BPSG insulator. The observation here of electron mobility enhancement in <100> channels due to parallel or perpendicular uniaxial strain is believed to be the first such experimental report. More work is needed to eliminate the possible effects of surface roughness on our FETs, and to provide better models of electron transport in highly-uniaxially-strained silicon layers.

7.3.5 Uniaxial-strain Induced Hole Mobility Enhancement

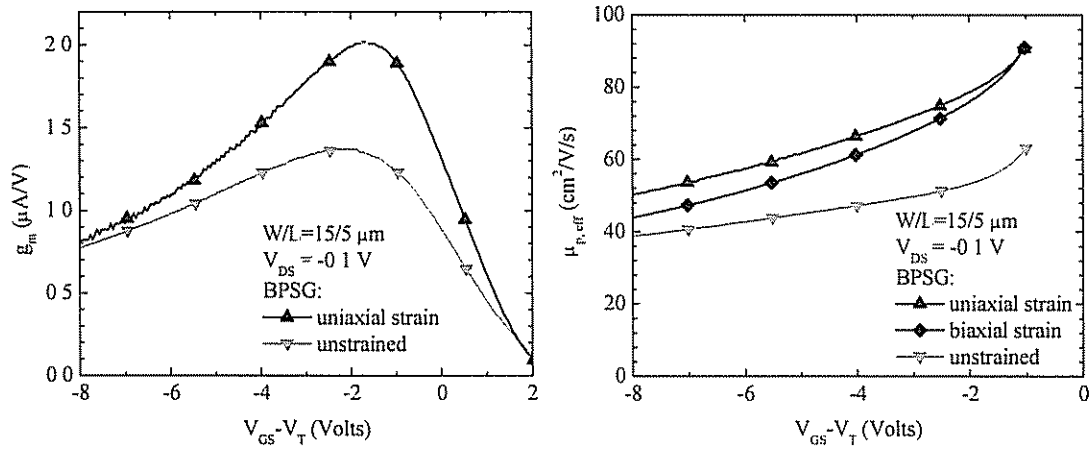
Uniaxially-strained p-MOSFET devices have also been measured. First consider the case of uniaxial tensile strain perpendicular to the <110> channel, which from piezoresistance theory is expected to show a large hole mobility improvement. Typical measured I-V_G curves for transistors with and without the SiN_x/SiO_2 barrier layers are plotted in Fig. 7.45a. As with the nFETs, the uniaxially-strained pFET devices are well-behaved, with low off currents, and negligible changes in threshold voltage and sub-threshold slopes compared to unstrained channel transistors. Again the barrier layer devices exhibit much quicker turn-on and higher ON currents than the BPSG-only devices. Due to the higher source/drain resistance of the pFET devices, the variation in mobility for these devices, as measured across control SOI pFET samples, is unfortunately large, at ±20%.

In Fig. 7.45b, the function $I_D \cdot g_m^{-1/2}$ is plotted for the measured device curves. The uniaxially-strained devices with barrier layers show a negligible amount of mobility enhancement, while the BPSG-only devices show a significant mobility enhancement. The reason for this discrepancy is not immediately clear, but will be discussed further below. The transconductance for the BPSG-only devices is plotted in Fig. 7.46a. The maximum transconductance increases 54% due to uniaxial strain from 1.43 to 2.20 μA/V,



(a) (b)

Figure 7.45: (a) I-V characteristics and (b) $I_D \cdot g_m^{-1/2}$ for pFET transistors with zero and uniaxial strain along the <110> crystal direction, with uniaxial strain perpendicular to the direction of current flow in the channel. The transistors have W/L=15/5 μm/μm and V_{DS}=+0.1V. Data are shown for two samples: BPSG only and SiO_2/SiN_x barrier layer.



(a) (b)

Figure 7.46: (a) Transconductance, g_m, and (b) effective hole mobility, $\mu_{p,\,eff}$, vs gate voltage minus the threshold voltage, V_{GS}-V_T, for pFET transistors with zero and uniaxial strain and, in (b), with biaxial strain. The uniaxial strain is along the <110> crystal direction, perpendicular to the direction of current flow in the channel. The transistors have W/L=15/5 μm/μm and V_{DS}=-0.1V. Data are shown for a sample with no barrier layers (BPSG only). The strained-induced enhancement of transconductance decreases sharply as the gate overdrive is increased. However, the effective hole mobility enhancement caused by uniaxial strain does persist at high gate voltages, in contrast to that caused by biaxial strain, which degrades as V_{GS} increases.

but as the gate overdrive ($|V_{GS}-V_T|$) increases, the transconductance enhancement is sharply reduced. To compare the effect of biaxial and uniaxial strain on hole mobility, in Fig. 7.46b the effective hole mobility (calculated from Eqn. 7.20 for the pFETs measured for Figs. 7.38 and 7.45) is plotted for the biaxial-strain, <110> transverse uniaxial-strain and unstrained silicon cases. The picture is in good agreement with that observed by others. The biaxial tensile strain causes hole mobility enhancement which degrades as the gate overdrive voltage ($|V_{GS}-V_T|$) increases, while the <110> transverse uniaxial strain-induced hole mobility enhancement persists at high gate voltages. This is in agreement with the uniaxial tensile strain results of Haugerud, *et. al.*, [82] who observed a 14% increase in hole mobility with the application of 0.031% strain, of Zhao, *et. al.*, who observed a 7% hole mobility increase with 0.12% strain, and of Wang, *et. al.*, who observed a 7% increase in on current with 0.2% strain. In these works, the strain was applied transverse to the current flow in the channel (as for our data presented above), and the hole mobility increase persisted up to vertical effective electric fields of ~0.6 MV/cm. The results of Fig. 7.46b indicate that uniaxial-strain induced hole mobility enhancement at high vertical field occurs not only for the low strain levels measured by these authors, but also for the larger uniaxial tensile strains achieved here.

Strain-induced hole mobility shifts were also measured for <110> channel orientations with the strain parallel to current flow in the channel. The averaged results are given in Table 7.11: The barrier layers devices show a hole mobility decrease of -11% (within the error bars) while the BPSG-only transistors exhibit a hole mobility increase of +21% (just beyond the error bars.) Other researchers have shown that in agreement with piezoresistance theory, the hole mobility has significantly decreased with the application of this type of strain [79,81]. It is possible that the slight mobility decrease observed for transistors with SiN_x/SiO_2 reflect this same trend. The reason for the hole mobility increase for the BPSG-only sample is not clear.

Mobility results for <100> channel orientations are also given in Table 7.11. This is the second known report of pFET transistors on uniaxially strained silicon aligned to <100> [94,95]. From piezoresistance it is expected that the mobility would slightly degrade. For each data point at least three transistors, with L = 5 μm and W = 10-60 μm were measured and their extracted mobilities averaged. The BPSG-only devices show

sample	channel alignment	ε_{uni}	μ_L	μ increase	μ_t	μ increase
SiO_2/SiN_x/BPSG	<100>	~0.4%*	176±4	-0.6%	164±19	-7.3%
	<110>	0.32%	158±2	-11%	170±13	-4.0%
BPSG only	<100>	~0.4%*	103±6	+54%	83±4	+24%
	<110>	0.34%	81±1	+21%	93±5	+39%

Table 7.11 Average pFET mobilities ($cm^2V^{-1}s^{-1}$) under zero or uniaxial strain. For each sample and strain type, at least three different transistors were measured. The mobility enhancements are calculated vs the unstrained values given in Table 7.9. Raman measurement error for uniaxial strain is ±0.12%. See the comment in Table 7.10 regarding channel directions. *The strain in <100> channels was not measured, but should be slightly higher than that in <110> channels, as discussed in Sec. 5.2.1.

strong mobility enhancements ranging from 24 to 54%, whereas the transistors with SiN_x/SiO_2 barrier layers actually show mobility decreases -1 to -7%. As for nFETs, the uniaxial-strain induced hole mobility enhancement in the longitudinal and transverse directions is expected to sum to equal the biaxial-strain induced enhancement. For the BPSG-only devices the sum of the uniaxial-strain induced enhancements (longitudinal + transverse) for devices aligned to <100> and <110> are 78% and 60%, respectively. These are slightly more than the 55% mobility enhancement (Table 7.9) observed for biaxially-strained devices. (The biaxial and uniaxial strain levels are, of course, different, so direct comparison is difficult.)

The uniaxially strained pFET results are thus far from conclusive, with the BPSG and barrier layer transistors showing very different results. In the most promising case of <110> uniaxial strain perpendicular to the channel, the BPSG-only devices show the expected performance increase at low electric field, which for μ_{eff} (but not g_m) persists at high field. For <110> strain parallel to the channel, and <100> strains either parallel or perpendicular to the channel, where piezoresistance theory predicts mobility degradation with tensile strain, the barrier layer devices show slight mobility degradation while the BPSG-only devices consistently exhibit strong mobility enhancement. Despite best efforts to minimize source/drain resistance, the existing devices have large parasitic resistances which make accurately extracting mobilities difficult, even using the technique described in Sec. 7.3.2. (Note the non-linear shape of the curves for the BPSG-only devices in Fig. 7.45b.) It is possible that some aspect of the pFET processing (including the surface roughness issue discussed above for nFETs) is affecting the BPSG-only and barrier layer samples differently. Perhaps the epitaxial thickening done on the barrier layer samples has incorporated unintentional doping into the channel that is degrading transistor performance. However it is not clear why this would not similarly affect biaxially-strained pFETs on the same barrier layer samples, which showed mobility enhancements in agreement with the quantum theory (Fig. 7.40 and Table 7.9).

7.4 Summary

In summary, n-channel and p-channel fully-depleted strained SOI MOSFETs have been fabricated. Using island geometry to control strain, uniaxially-strained, biaxially-strained and unstrained silicon transistors were fabricated simultaneously, side-by-side on the same sample. The FET process was optimized to minimize the source/drain resistance in these ultra-thin body transistors. The thermal budget was minimized in order to maintain the initially-developed uniaxial or biaxial strain in the channels. By adding silicon nitride / silicon dioxide barrier layers between the BPSG and the silicon channel, the transistor sub-threshold slope was significantly decreased and the hole and electron mobilities increased, due to a reduced density of states at the back silicon interface and to reduced outdiffusion from the BPSG into the channel. The substrate bias was separately chosen separately for each type of sample in order to ensure full channel depletion.

Biaxially-tensile strained silicon devices show significant electron and hole mobility enhancements, as predicted by quantum theories and observed by other researchers. Uniaxially-strained devices were fabricated in four different configurations, with the channel aligned to <100> or <110>, and with the channel either parallel or perpendicular to the uniaxial strain. It is believed that this is the first report of uniaxially strained n-channel MOSFETs aligned to <100>. For nFETs, uniaxial strain in either the <100> or <110> directions parallel to the channel induces 23-72% electron mobility enhancement that persists at high vertical fields. When a <100> or <110> channel is oriented perpendicular to the strain the maximum electron mobility improvement is less than 15%. It is thought that in addition to strain effects, the long-range channel surface roughness due to buckling (as described in Ch. 6) may also change the electron mobility, due to an unknown effect. For pFETs, the results are less clear. On devices with no barrier layer, all types of uniaxial strain show mobility enhancements of at least +21%, up to +54%. In contrast, the samples with nitride/oxide barrier layers exhibit small (-1 to -11%) mobility decreases with uniaxial tensile strain. The high source/drain resistance of these devices, possibly coupled with other processing effects may be obscuring the strain-induced mobility changes that one would like to observe.

The results show that bulk piezoresistance is insufficient to explain the observed strain dependence of electron and hole mobility for large uniaxial strains of 0.3-0.6%. The differences may be due to 2-D quantum confinement of carriers in the potential well formed at the channel surface at high gate voltages, to long-range surface roughness at the gate oxide interface caused by film buckling, to differences in short-range roughness in the different strain cases, or to some as-yet unknown parameter.

Chapter 8

Conclusions

8.1 Summary

By modifying the island geometry of SiGe islands bonded on compliant BPSG, lateral expansion during high temperature anneals has been used to generate biaxially-stressed, uniaxially-stressed, and relaxed SiGe films on the same substrate. Replacing the single SiGe layer with a Si/SiGe bi-layer, during lateral expansion the two layers come to a force balance. The top SiGe layer can be removed from the bi-layer after lateral expansion by selective etching. The result is relaxed, uniaxially-strained, and biaxially-strained silicon islands located side-by-side on a single wafer. The magnitude of the strain can be well controlled by varying the SiGe composition (and thereby its initial biaxial strain level) and the relative silicon and SiGe layer thicknesses. For the rectangular island geometries which yield uniaxially-strained silicon, the crystal-direction of the island edges also determines the uniaxial silicon strain level. A maximum uniaxial silicon tensile strain of +1.0% has been achieved in the <100> direction. By the Poisson effect the uniaxial silicon strain is always larger than biaxial strain generated from the same original Si/SiGe stack.

The lateral expansion process for both biaxial and uniaxial strain can be modeled numerically. The biaxial strain at the center of a square island of SiGe decreases exponentially according to a time constant that is proportional to the BPSG viscosity and the square of the island edge length, and is inversely proportional to the SiGe and BPSG layer thicknesses. From simulations, it is clear that narrow rectangles, with large length-to-width aspect ratios, have the largest anneal-time process windows for obtaining uniaxial silicon strain. For islands with aspect ratios of less than four, the short and long island directions expand on approximately the same time-scale and it is impossible to achieve the maximum uniaxial strain for the given bi-layer.

Instead of expanding laterally, the strained films can also relieve their strain by buckling out of the plane of the film. This undesirable buckling process, which competes with lateral expansion, can be slowed and the buckling amplitude minimized by thinning the BPSG layer. More work is needed on very thin BPSG films (< 100 nm), as buckling theory predicts that with very thin BPSG, buckling will diminish compared to lateral expansion, allowing for large, flat, strain-controlled SiGe or silicon films.

Another route to reducing the impact of buckling is by using 1-D buckling instead of 2-D buckling. One-dimensional buckling was observed in uniaxially-stressed SiGe films whereas two-dimensional buckling occurs in biaxially-stressed films. Due to the lower 1-D vs 2-D stress in this technology, the observed 1-D buckling was slower and of lower amplitude than the 2-D buckling. This measured result is supported by buckling models using linear perturbation theory and energy minimization.

These strained-silicon films can be used to make mobility enhanced SOI MOSFETs. The use of a double barrier layer of silicon nitride and silicon dioxide effectively prevents outdiffusion of dopants from the BPSG into the silicon channel and improves the electronic quality of the back interface. Biaxially-tensile strained silicon shows enhanced electron and hole mobility. Uniaxially-strained nFETs show moderate mobility enhancement when the channel and strain are parallel, for channels aligned to either <100> or <110>. When the channel and strain are perpendicular, the electron mobility enhancement, while present, is negligibly small. The different surface roughness of differently-strained islands may contribute to these results, which are at odds with the expectations of piezoresistance theory. For pFETs, large hole mobility enhancements are seen for the sample with no barrier layers, but similar improvements are not observed when the nitride/oxide barrier layers are present. This discrepancy may be due to unintentional doping introduced by epitaxial thickening of the strained-silicon channels on the barrier layer samples. Clearly, uniaxial strain can enhance both hole and electron mobilities, but further work is needed to clarify the underlying physical mechanisms governing charge carrier transport in these strained-silicon layers.

8.2 Future Work

There are several avenues for possible future research based on the work in this thesis. First, it is of great technological interest to scale down this strain generation process to the ~100-nm scale (or less), for use in today's advanced CMOS technologies, as has already been discussed in Sec. 5.4. Beyond the challenges of fabricating thinner BPSG layers with sufficiently low viscosity, measuring strain in 100-nm scale islands, and controlling short anneals for lateral expansion, it will be critical to develop auxiliary techniques to maintain the strain during subsequent device processing. While this problem was adequately dealt with for the large (10-100-μm scale) islands used here, it will become much more challenging as the island size is scaled down.

Second, this thesis has been limited to the generation of tensile silicon strain. By using dilute silicon-carbon alloys with low carbon fractions (< 4%) instead of SiGe, it may be possible to generate biaxially- and uniaxially-compressive silicon. For example, a relaxed silicon carbon layer could be used to heteroepitaxially grow a thin biaxially-compressive silicon layer. Or, a thin biaxially-tensile silicon carbon, Si_yC_{1-y}, layer can be used in a bi-layer with silicon to obtain uniaxially-compressively strained silicon by force balance of rectangular islands. As seen from process-induced and mechanically-induced strain experiments, uniaxial compressive strain can increase hole mobilities even at high vertical electric fields. Some minor and unsuccessful efforts have been made toward this goal, but more work is called for.

While the present FET results demonstrate that uniaxial tensile silicon strain generated using lateral expansion can be used to enhance both hole and electron mobilities, more work is needed to clarify the physical mechanisms causing the observed mobility improvements. Specifically, the buckling reduction techniques described in Ch. 6 should be applied to device layers (*i.e.*, using very thin BPSG) to ensure that buckling is not a significant source of gate oxide/Si channel interface roughness. Using a raised source/drain process to decrease resistance to the channel would minimize measurement error, especially for the pFET devices, to make those results more conclusive.

Lastly, the uniaxial strain generation technique developed here should be extended to other material systems, such as III-V and II-VI semiconductors.

Appendix A

Wafer Bonding and Smart-Cut Layer Transfer Process

This appendix presents the wafer bonding process used in this thesis. The work, unless otherwise specified, was performed at the U.S. Naval Research Laboratory in Washington, D.C. The original process was developed there by Karl Hobart; a general description can be found in Refs. [103,104] and in Ch. 3. The process was optimized in February 2005 to bond donor wafers with oxide/nitride capping layers (see Sec. 3.2.2). Wafers bonded earlier with no cap layers were bonded using a simplified process, skipping the plasma treatments and final SC-1 etch. Details on the individual steps are given below in Sec. A.4.

A.1 BPSG Handle Wafer Preparation

We begin by depositing the BPSG, then cleaning and optionally annealing the BPSG-coated handle wafer. See Sec. A.4 for details.

The process flow is:

- Deposit BPSG by chemical vapor deposition (CVD) onto a silicon handle wafer. The BPSG has 4.4% B and 4.1% P by weight. Post-deposition anneal at 800 °C in a wet O_2 atmosphere for 1 hr, followed by a 30-min anneal at 900 °C in N_2. Final wet clean. (These processes done at Northrop Grumman, Linthicum, MD. Due to Northrop's processing requirements, BPSG wafers are minimum 6" diameter.)
- BPSG wafer: clean with CO_2 "snow" gun under bright light on 139 °C hot plate.
- BPSG wafer: SC-1 wet clean, 16 min with ultrasonic agitation, spray rinse with D.I., D.I. tank rinse 10 min, Megasonic rinse, spin dry
- BPSG wafer: Anneal (optional)
    - Load wafer into cool furnace (<300 °C). Set to #600
    - 1.25-hr anneal after temp reaches 800 °C

- Set to #000, wait for cool furnace (<300 °C)
- Pull boat to mouth, wait 10 min. Unload.

A.2 Si/SiGe Donor Wafer Preparation

The SiGe/Si thin films are heteroepitaxially grown on a silicon donor wafer. The wafer is ion implanted for later Smart-Cut™, and then cleaned for wafer bonding. Details on the individual process steps are given below in Sec. A.4.

The process flow is as follows:

- Heteroepitaxial SiGe/Si growth performed by Lawrence Semiconductor Research Laboratory, Tempe, AZ on prime grade silicon wafers.
- Grow SiO_x and/or deposit SiN_x cap layers, as desired (see Ch. 7 for details). These steps done at Princeton University. To enable capping using Princeton facilities, donor wafers are maximum 4" diameter.
- Ion Implantation performed by Implant Science Corp., Wakefield, MA
  - Typical conditions: Species: H+, Energy: 150-180 keV, True dose: 4.5×10^{16} cm^{-2}
- Donor wafer: Piranha clean, D.I. rinse 10x, Megasonic rinse, spin dry

A.3 Wafer Bonding and Layer Transfer Process

The donor and handle wafers are cleaned twice by a sequence of plasma and wet etches, and then physically bonded. The wafer pair is annealed to strengthen the bond and the donor wafer is split off by Smart-Cut™. The residual donor wafer layer is removed by a selective wet etch.

The bonding process follows:

- Donor wafer: O_2 plasma 5 min at 100%
- BPSG wafer: O_2 plasma 2 min at 100%
- Both wafers: SC-1 16 min with ultrasonic agitation, spray rinse with D.I., D.I. tank rinse 10 min or more.

- Donor wafer: Megasonic rinse, spin dry. O_2 plasma 33 sec at 100%, wet clean SC-1 45 sec with ultrasonic agitation, spray rinse with D.I., D.I. tank rinse 10+ min.
- Keep donor wafer in D.I. until D.I. rinse of BPSG wafer has 1 min left, to minimize time donor wafer sits in spin dryer.
- Initially, keep BPSG wafer in D.I. While chamber is venting after donor wafer plasma, Megasonic rinse and spin dry BPSG wafer.
- BPSG wafer: O_2 plasma 33 sec at 100%, wet clean SC-1 45 sec with ultrasonic agitation, spray rinse with D.I., D.I. tank rinse 10 min.
- Donor wafer: Short megasonic rinse, spin dry.
- BPSG wafer: Short megasonic rinse, spin dry.
- Load 4" donor wafer into bonding jig, face up. Minimize movement of donor wafer after placing in jig.
- Load 6" BPSG wafer into bonding jig, face down. Minimize time that donor wafer sits uncovered, without 6" BPSG wafer on top.
- Press wafers together at center and then radially outward, using special tool.
- Inspect the bonded wafers using IR camera
- Clean the backside of the 6" wafer using O_2 plasma, 2 min at 100%.
- Bond strengthening anneal
    - Load into cool furnace (<250 °C)
    - If two wafer pairs are loaded, BPSG wafers should always be on the outside
    - Set furnace to #050 (~250 °C). Anneal a minimum of 4 hrs, maximum 14 hrs
    - Set to #060 (~260 °C). Anneal 1 hr further.
    - Pull wafer boat out to furnace mouth. Set to #000 (~200 °C). Wait 10 min.
    - Unload. Inspect by IR.
- Smart-Cut split
    - Load into cool furnace (<300 °C).
    - Set furnace to #200 (~400 °C)

    - Splitting should occur within 2 min of furnace thermocouple reading 400 °C.
    - As soon as the splitting noise is heard (and hopefully the donor wafer slides off to confirm), set the furnace to #450 (~650 °C).
    - Wait for 650 °C. Anneal 2 hrs at 650 °C.
    - Set to #000 (~200 °C), wait for cool furnace (<300 °C).
    - Pull boat to furnace mouth, wait 10 min.
- Inspect using IR camera. Use CO_2 "snow" gun to clean top surface of bonded 6" wafer.
- Scribe edges perpendicular to major flat, so 6" wafer fits in 1 liter glass beaker
- HF etch until donor wafer area is hydrophobic
- KOH etch until donor wafer area has uniform color

A.4 Lab Process Details

Piranha clean of donor wafers

- Piranha 3:1 H_2SO_4:H_2O_2 30% at 125 °C on hot plate in glass container labeled "P". Heat up sulfuric (about 13 mm deep) then add peroxide.
- Drop wafer face up into bath with dirty glass filled poly tweezers—make sure wafer goes to the bottom and does not float. Piranha clean for 10 min.
- Rinse about 10x using bottom of plastic bottle labeled "CLEAN." Fill using DI spray gun and dump by hand.
- Megasonic rinse, spin dry.
- Load into clean wafer carrier cartridge to await further processing.

Megasonic rinse

- Equipment: Pulse Jet W-357-3MP, Honda Electronics Co., LTD,
- Turn on megasonic water and power so it's vaporizing (1.1A)
- Using "wet" vacuum tweezers, hold wafer within 2 cm of nozzle. Thoroughly clean, about 1 min.

Spin dry

- Equipment: Model WS-400A-6NPP/LITE, Laurell Technologies Corp.
- Make sure chuck is correct for wafer size
- Load wafer into spinner using "wet" vacuum tweezers. Run 3 min at 4 krpm.
- Use "dry" vacuum tweezers to pick up. Always hold vacuum tweezers 90° from flat.

SC-1 wet etch

- Preparation
  - Fill D.I. H_2O bath to operation line, warm to 40 °C, put on proper lid
  - Fill quartz container 5:1:1 D.I. H_2O: 30% H_2O_2 : NH_4OH
  - Slowly lower quartz container into lid opening, opening valve to empty water as needed
  - Use Sonic/Degas for 5 min or more to get solution warm
  - Top off with D.I. if solution evaporates throughout day.
- Etch process
  - Secure wafers on 4" wafer wand(s) using notched slider. Using hanger on ultrasonic cover, immerse wafer(s) in SC-1
  - Etch desired time in SC-1. Use ultrasonic agitation if desired. Meanwhile fill rinse tank with D.I. Turn off when full to minimize D.I. usage.
  - One at a time, unload wafer wands from bath. Spray using DI gun. Put into rinse tank with wand hook balanced at rim. Turn D.I. on, let run 10 min. Turn off D.I.
  - Take out of rinse tank, transfer to "wet" vacuum tweezers.
  - Megasonic rinse. Spin dry.

O_2 plasma etch

- Load wafer into chamber. A 6" wafer lays directly on the chamber surface. A 4" wafer sits on the metal tray.
- Pump down < 100 μm Hg (Note 1 μm Hg = 1 mTorr.)

- Make sure the O_2 gas tank is open. Turn on O_2 gas. Wait for pressure < 240 μm Hg
- Select 100% power setting on side dial
- Press appropriate express time on microwave ("2" or "5" for 2 minutes and 5 minutes, respectively). For 33 seconds, press "TIME COOK", "3"-"3", "START." Turn off lights to monitor plasma.
- Pressure during run should be <240 μm Hg after the initial surge as the plasma forms
- When done, let pressure fall, then rise again to >160 μm Hg. Turn off O_2. Let pressure fall below 100 μm Hg. Vent using the system vacuum "PURGE" setting.
- When at vacuum gauge reaches 0" Hg, open chamber and remove sample. Turn pump off using the system vacuum "OFF" setting.

When done for the day, turn off oxygen button and tank. Open the pyrex lid, open the pump valve using the system vacuum "ON" setting to briefly to vent foreline of pump. Turn off pump and cooling water.

Physical bonding

- See Fig. A.1 for a diagram of the bonding jig.
- The donor wafer is placed face up on the jig, aligned to the outline of the 4" wafer, with the major flat to the left.
- The major flat of the BPSG wafer is pressed up against the leftmost block, and the BPSG wafer is slowly lowered down in place so it is on top of the donor wafer and within the adjustable screws on the far side.
- A special Teflon tool that resembles a miniature bell-headed hammer is used to apply pressure first at the center of the two wafers, then at discrete points moving radially outward.

HF and KOH etching

- Prepare baths
  - In 1 liter glass beaker, using plastic graduated cylinder, mix 45% KOH: D.I. H_2O 1:5 (172 ml : 860 ml)
  - Heat ultrasonic bath to 40 °C. Use top with round cutout. Lower KOH beaker in. Use sonic to heat up KOH bath.
  - Mix dilute 1 : 10 49% HF : D.I. H_2O in poly beaker
  - Set up second glass beaker with D.I. H_2O for rinsing
- Prepare wafer
  - Scribe wafer twice from about 1cm in down to the edge as shown in Fig. A.2.
  - Hold large tweezers in middle, small tweezers on outside, very close to the scribe mark. Gently bend hands apart. Wait for the wafer to crack, don't force it.
  - Use two blue clips to hold wafer opposite flat.
- HF etch
  - Put wafer in D.I. H_2O briefly to hydrate surface
  - Put wafer in HF until hydrophobic (lift out to check)
  - Rinse in D.I. H_2O. Dump H_2O, then refill using side tap.
- KOH etch
  - Use ultrasonic for only about 10 sec to loosen bubbles. Then etch 5 to 8 min until uniform color. Can over etch up to 1 min, etch has 100:1 selectivity.
  - Rinse well in D.I. H_2O. Dry using N_2 gun by hand (prop up against ultrasonic container)
  - Inspect using microscope.

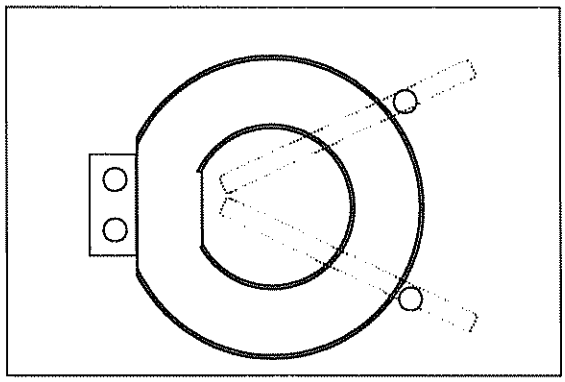


Figure A.1: Top down schematic view of the bonding jig. The bottom is a flat piece of Teflon, about 8" x 10" with two slots cut as shown by the dotted lines. Set into these slots are poly screws, the position of which can be adjusted to fit the wafer size. Outlines of 4" and 6" wafers have been marked on the bottom Teflon, with both major flats aligned to the left. A block of Teflon on the left, secured with screws, provides a hard edge for aligning the 6" wafer flat.

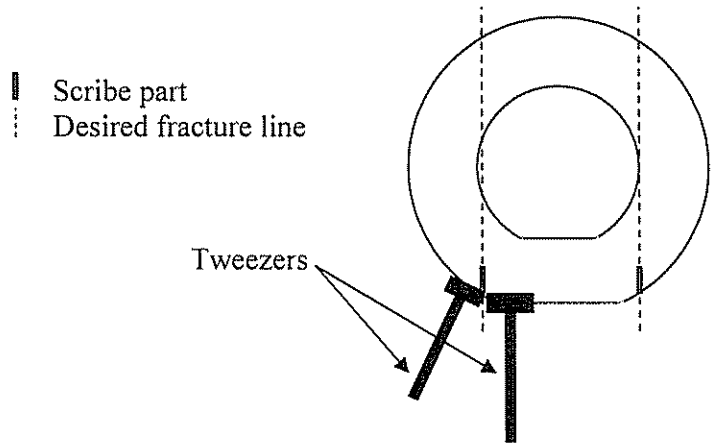


Figure A.2: Top down schematic showing how to scribe the bonded wafer so it will fit in the etch bath beakers. The two concentric circles indicate the 6" BPSG wafer outline with the bonded donor layers on top. The short (red) solid lines indicate the scribe marks, while the dotted lines indicate the desired fracture planes.

Appendix B

Hooke's Law Applied to $Si_{1-x}Ge_x$ with Various Crystal Directions

This appendix describes the application of Hooke's law to diamond lattice semiconductors such as $Si_{1-x}Ge_x$, and defines the elastic stiffness coefficients, c', the elastic compliant coefficients, s', the Young's modulus, E, and Poisson's ratio, ν, as a function of angle within the (001) surface plane of this material.

B.1 Hooke's Law: Relating Film Stress and Strain

The stress and strain state of a material are related by Hooke's law, which in its general form is [197]:

$$\sigma'_{ij} = \sum_{kl} c'_{ijkl} \varepsilon'_{kl}, \tag{B.1}$$

where σ' and ε' are the component stress and strains, and c' are the elastic stiffness coefficients. The primed notations indicates that the axes are in an arbitrary crystal direction, whereas unprimed values refer to axes along the [100], [010] and [001] crystal directions.

By symmetry, the c' matrix is reduced to 6x6 and the 4th-rank tensor notation of c'_{ijkl} is compressed to c'_{ik} according to the standard rule (xx → 1, yy → 2, zz → 3, yz → 4, zx → 5, xy → 6).

B.2 Transformation of Elastic Stiffness Coefficients with Crystal Direction

To relate stress and strain in an arbitrary crystal direction, we need to obtain the c' matrix for that crystal direction. To do so, we transform c' to other axes using [197]:

$$c'_{ijkl} = \sum_{g,h,m,n} T_{ig} T_{jh} c_{ghmn} T_{km} T_{ln}, \tag{B.2a}$$

which when simplified, becomes

$$c'_{ijkl} = c_{ijkl} + c_c \left[\sum_{n=1}^{3} T_{in} T_{jn} T_{kn} T_{ln} - \delta_{ij}\delta_{kl}\delta_{ik} \right], \tag{B.2b}$$

where $c_c = c_{11} - c_{12} - 2c_{44}$ is the elastic anisotropy parameter, and the values of the elastic stiffness constants, c_{11}, c_{12} and c_{44}, are given in Table 3.1. Note that by the crystal symmetry of cubic crystals, only three elastic stiffness constants are needed. As listed in Table 3.1, the values of c_{11}, c_{12} and c_{44} are constant for a given material. From Eqn. B.1, c_{11} relates a uniaxially-applied <100> strain to the resulting parallel stress ($\sigma_{xx}=c_{11}\varepsilon_{xx}$), while c_{12} relates a uniaxial <100> strain to the resulting perpendicular stress, ($\sigma_{yy}=c_{12}\varepsilon_{xx}$), and c_{44} relates the cross stress and strain terms ($\sigma_{xy}=2c_{44}\varepsilon_{xy}$).

The crystal-direction-dependence of the stress-strain relationship is described by the c' matrix, *e.g.*, c'_{11} relates a uniaxial strain in an *arbitrary* crystal direction to the resulting parallel stress ($\sigma'_{xx}=c'_{11}\varepsilon'_{xx}$). In Eqn. B.2, T_{ij} is the direction cosine between the $x'y'z'$ and xyz axes, where the xyz axes are aligned to [100], [010], and [001]. The transform, T, needed to go between the xyz the $x'y'z'$ axes is a 3x3 matrix given by [185] the direction cosines:

$$T = \begin{bmatrix} l_1 & l_2 & l_3 \\ m_1 & m_2 & m_3 \\ n_1 & n_2 & n_3 \end{bmatrix} = \begin{bmatrix} \cos\theta\cos\phi & -\sin\theta & \cos\theta\sin\phi \\ \sin\theta\cos\phi & \cos\theta & \sin\theta\sin\phi \\ -\sin\phi & 0 & \cos\phi \end{bmatrix}, \tag{B.3}$$

where θ is the angle of initial rotation about the z-axis [001] from [100] toward [010], and ϕ is the subsequent amount of rotation about the fixed y' axis, as sketched in Fig. B.1.

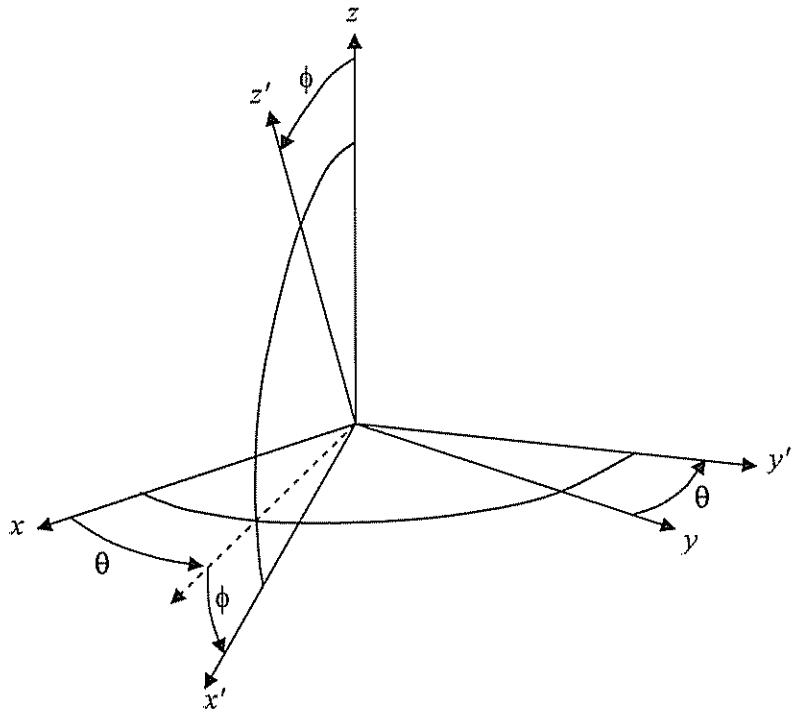


Figure B.1: Definition of the θ and ϕ angles for transformation of the c' matrix, from [185].

For a film with a (001) surface plane, ϕ =0°, and θ is the angle of rotation from [100] toward [010]. The T matrix then takes the form of

$$T = \begin{bmatrix} l_1 & l_2 & l_3 \\ m_1 & m_2 & m_3 \\ n_1 & n_2 & n_3 \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta & 0 \\ sin\theta & cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{B.4}$$

The c' matrix then becomes

$$c' = \begin{bmatrix} c'_{11} & c'_{12} & c'_{13} & 0 & 0 & c'_{16} \\ c'_{12} & c'_{11} & c'_{13} & 0 & 0 & c'_{26} \\ c'_{13} & c'_{13} & c'_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & c'_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c'_{44} & 0 \\ c'_{16} & c'_{26} & 0 & 0 & 0 & c'_{66} \end{bmatrix}, \tag{B.5}$$

where [150]

$$c'_{11} = c_{11} - \frac{c_c}{2}\sin^2(2\theta), \tag{B.6a}$$

$$c'_{12} = c_{12} + \frac{c_c}{2}\sin^2(2\theta), \tag{B.6b}$$

$$c'_{13} = c_{12}, \tag{B.6c}$$

$$c'_{33} = c_{11}, \tag{B.6d}$$

$$c'_{44} = c_{44}, \tag{B.6e}$$

$$c'_{66} = c_{44} + \frac{c_c}{2}\sin^2(2\theta), \tag{B.6f}$$

$$c'_{16} = -\frac{c_c}{4}\sin(4\theta), \text{ and} \tag{B.6g}$$

$$c'_{26} = +\frac{c_c}{4}\sin(4\theta). \tag{B.6h}$$

B.3 Elastic Compliance Coefficients

The elastic compliance coefficients, s'_{ijkl}, are used to relate the strain in a material to its stress, according to [197]

$$\varepsilon'_{ij} = \sum_{kl} s'_{ijkl}\sigma'_{kl}, \tag{B.7}$$

where again the 4th-rank tensor s'_{ijkl} compresses to s'_{ik} and Table 3.1 gives the three compliance constant values needed for cubic crystals, s_{11}, s_{12} and s_{44}, for silicon and $Si_{0.7}Ge_{0.3}$. As for elastic stiffness, the elastic compliance constants s_{11}, s_{12} and s_{44} are constant for a given material. To relate strains and stresses in arbitrary crystal directions, the s' matrix is used.

The s' matrix is simply the inverse of the c' matrix, and the elastic stiffness constant and elastic compliant constant values are related by [197]

$$s_{11} = \frac{c_{11} + c_{12}}{(c_{11} - c_{12})(c_{11} + 2c_{12})}, \tag{B.8a}$$

$$s_{12} = \frac{-c_{12}}{(c_{11} - c_{12})(c_{11} + 2c_{12})}, \text{ and} \tag{B.8b}$$

$$s_{44} = \frac{1}{c_{44}}. \tag{B.8c}$$

Conversely [197],

$$c_{11} = \frac{s_{11} + s_{12}}{(s_{11} - s_{12})(s_{11} + 2s_{12})} \tag{B.9a}$$

$$c_{12} = \frac{-s_{12}}{(s_{11} - s_{12})(s_{11} + 2s_{12})} \tag{B.9b}$$

$$c_{44} = \frac{1}{s_{44}} \tag{B.9c}$$

Because the s' and c' matrices are exact inverses, they will transform in the same way, with s'_{ik} replacing c'_{ik}, s_{ik} replacing c_{ik}, and s_c replacing c_c in Eqn. B.6, where we can define $s_c = s_{11} - s_{12} - \frac{1}{2}s_{44}$, as the compliance anisotropy factor.

B.4 Transformation of Stress and Strain to Different Crystal Directions

The transformation matrix, T, can also be used to transform stress and strain along arbitrary axes within the crystal, according to

$$\varepsilon_{ij} = \sum_k \sum_l T_{ki} T_{lj} \varepsilon'_{kl} \quad \text{and} \tag{B.10}$$

$$\sigma_{ij} = \sum_k \sum_l T_{ki} T_{lj} \sigma'_{kl}\,, \tag{B.11}$$

where again the primed values indicate the arbitrary axes and the unprimed values the [100], [010], and [001] axes.

For example, an arbitrary strain ε'_{xx} and ε'_{yy} along the [110] and [$\bar{1}$10] directions in the (001) plane can be transformed into the reference axes according to

$$\varepsilon = \begin{bmatrix} 1/2\left(\varepsilon'_{xx} + \varepsilon'_{yy}\right) & 1/2\left(-\varepsilon'_{xx} + \varepsilon'_{yy}\right) & 0 \\ 1/2\left(-\varepsilon'_{xx} + \varepsilon'_{yy}\right) & 1/2\left(\varepsilon'_{xx} + \varepsilon'_{yy}\right) & 0 \\ 0 & 0 & \varepsilon'_{zz} \end{bmatrix}. \tag{B.12}$$

B.5 Young's Modulus and Poisson's Ratio vs Crystal Direction

Young's modulus, E, is defined as the ratio of an applied uniaxial stress to the resulting strain in the same direction, that is [150]

$$\frac{1}{E'_{ii}} = \frac{\varepsilon'_{ii}}{\sigma'_{ii}} = s'_{ii}\,, \tag{B.13}$$

where i = 1, 2, or 3. Therefore, we can define the Young's modulus in an arbitrary direction as [125]

$$\frac{1}{E} = s'_{11} = s_{11} - 2S\left(l_1^2 l_2^2 + l_2^2 l_3^2 + l_1^2 l_3^2\right). \tag{B.14}$$

For the (001) surface, with a rotation of θ from the [100] toward the [010] direction, this expression simplifies to

$$\frac{1}{E(\theta)} = s_{11} - \frac{(s_{11} - s_{12} - s_{44}/2)}{2} sin^2(2\theta), \tag{B.15}$$

as plotted in Fig. 3.29.

Poisson's ratio, ν, is the ratio of transverse contraction to elongation in simple tension [150]

$$\nu_{ij}' = -\frac{\varepsilon_{jj}'}{\varepsilon_{ii}'} = -\frac{s_{ij}'}{s_{ii}'}, \tag{B.16}$$

where $i, j = 1, 2, 3$ and $i \neq j$. For $i = 1, j = 2$, we obtain [125]

$$\nu = -\frac{s_{12}'}{s_{11}'} = -\frac{s_{12} + S\left(l_1^2 m_1^2 + l_2^2 m_2^2 + l_3^2 m_3^2\right)}{s_{11} - 2S\left(l_1^2 l_1^2 + l_2^2 l_2^2 + l_3^2 l_3^2\right)}, \tag{B.17}$$

which in the (001) plane with θ rotation from the [100] toward the [010] crystal direction becomes Eqn. 3.11, repeated here:

$$\nu(\theta) = -\frac{2 \cdot s_{12} + (s_{11} - s_{12} - s_{44}/2) \cdot \sin^2(2\theta)}{2 \cdot s_{11} - (s_{11} - s_{12} - s_{44}/2) \cdot \sin^2(2\theta)}. \tag{B.18}$$

Equation B.18 is plotted in Fig. 3.26. Note that the ratio of E to $(1-\nu)$ is constant in the (001) plane [125]:

$$\frac{E}{(1-\nu)_{(001)plane}} = \frac{1}{s_{11} + s_{12}} = c_{11} + c_{12} - 2\frac{c_{12}^2}{c_{11}} \tag{B.19}$$

B.6 Summary of Equations Relating Stress and Strain

Thus, for the (001) plane with θ rotation from the [100] toward the [010] crystal direction, the stress vs strain relations from Eqn. B.1 are:

$$\sigma_{xx}' = c_{11}'\varepsilon_{xx}' + c_{12}'\varepsilon_{yy}' + c_{13}'\varepsilon_{zz}' + c_{16}'\varepsilon_{xy}', \tag{B.20a}$$

$$\sigma_{yy}' = c_{12}'\varepsilon_{xx}' + c_{11}'\varepsilon_{yy}' + c_{13}'\varepsilon_{zz}' + c_{26}'\varepsilon_{xy}', \text{ and} \tag{B.20b}$$

$$\sigma_{zz}' = c_{13}'\varepsilon_{xx}' + c_{13}'\varepsilon_{yy}' + c_{33}'\varepsilon_{zz}', \tag{B.20c}$$

where the values of c'_{ik} are given by Eqn. B.6.

Alternately, we can express the strain in terms of the stress by Eqn. B.7:

$$\varepsilon'_{xx} = s'_{11}\sigma'_{xx} + s'_{12}\sigma'_{yy} + s'_{13}\sigma'_{zz} + s'_{16}\sigma'_{xy}, \tag{B.21a}$$

$$\varepsilon'_{yy} = s'_{12}\sigma'_{xx} + s'_{11}\sigma'_{yy} + s'_{13}\sigma'_{zz} + s'_{26}\sigma'_{xy}, \text{ and} \tag{B.21b}$$

$$\varepsilon'_{zz} = s'_{13}\sigma'_{xx} + s'_{13}\sigma'_{yy} + s'_{33}\sigma'_{zz}, \tag{B.21c}$$

where the values of s'_{ik} are obtained from Eqn. B.6 by replacing c'_{ik} with s'_{ik} and c_c with s_c. In practice, we can neglect the c'_{16} and c'_{26} terms (and s'_{16} and s'_{26} terms) because they are equal to zero for the <100> and <110> directions considered in this work.

Appendix C

Matlab Scripts Used in this Work

This appendix provides *matlab* scripts used for numerical simulations and data processing for the work presented in this thesis. In Sec. C.1 the script used to automate Raman spectroscopy data extract is given. In Sec. C.2 the script used to numerically simulate the lateral expansion of a single SiGe layer is provided, and in Sec. C.3 the script used for buckling parameter calculations is given. Finally, in Sec. C.4, the script for extraction of MOSFET parameters from measured *I-V* data traces is provided.

C.1 Automated Data Extraction from Raman Spectra

The extraction of peak positions from Raman spectra has been automated to ensure consistency and make data analysis more efficient. This section describes the procedure and provide the *matlab* script for extracting the Si-Si phonon peak locations for samples used in this thesis.

C.1.1 Data Extraction Procedure

The peak-fitting algorithm employed is very basic. A specified, constant baseline is subtracted from the spectrum. In the desired wavenumber range for a given Si-Si phonon, the peak intensity is found. Looking on both sides of the peak, the full-width half-maximum (FWHM) points are determined by interpolating between existing data points. The peak position is calculated as the average of the lower and upper FWHM wavenumbers.

For the silicon substrate peak, this procedure is sufficient. For peaks from the SiGe and silicon epi layers, which are of much lower intensity due to the thinness of the layers, a slightly different method is followed. First, the silicon substrate peak position is found or assumed. The Raman spectrum above the peak location (toward higher wavenumbers) is mirrored below the peak to form a silicon substrate spectrum. This

substrate spectrum is subtracted from the measured spectra to yield an epi-only spectrum. This epi-only spectrum is then analyzed using the average FWHM method described above.

The *matlab* script to implement these methods is given below in Sec. C.1.2. The script is used in two different modes. Mode 1 is used for bulk silicon samples or bonded samples with single SiGe layers on BPSG. In this mode, the silicon substrate peak position is found using the baseline + FWHM technique. Then, this peak position is used to subtract the silicon substrate spectrum, and the remaining epi-only spectrum is analyzed by the FWHM method to locate the SiGe layer Raman peak. Mode 2 is used for samples with SiGe/Si bilayers on BPSG. In this mode, the silicon substrate peak position must be already determined from bulk silicon measurements (analyzed by Mode 1) made on the same day. Using the known silicon substrate peak location, the silicon substrate spectrum is again subtracted to yield the epi-only spectrum. The FWHM method is used to located peak positions for the SiGe and silicon epi layers. However, if the silicon epi layer has a small amount of strain, its peak can be obscured in the silicon substrate peak tail. In this case, the baseline + FWHM technique is used on the original spectrum to find the location of the merged silicon substrate and silicon epi peak. Assuming the two layers provide peaks of equal intensity, the merged peak location is then just an average for the two peaks, and the silicon epi peak location can be directly calculated.

The correctness of these methods has been confirmed by comparison with results from the PeakFit software. The *matlab* script was used instead of PeakFit because of the ease and consistency of *matlab* data extraction for the silicon epi layer, which was difficult to handle in PeakFit when obscured by the silicon substrate peak.

Note that changes in the format of the acquired data file (by changing Raman measurement parameters) may necessitate adjustments to the *matlab* script, specifically in the specifications of the wavenumber ranges used to look for peaks.

C.1.2 Matlab Script for Raman Data Extraction

```
% Subtracting Si peak from Raman traces
% File p2.m
% Written by Rebecca L. Peterson
% rev 1, Feb 6, 2004
```

```
close;
clear all;

% Ask for a file name (.dat)
filename=input('Please input the directory\\filename containing data:
','s');

% Read in header info
fid=fopen(filename,'r');
line1=fgets(fid);
sfid=fopen('temp.txt','w');
fprintf(sfid,line1);
fclose(sfid);
[a b c d e f g h j position l m
n]=textread('temp.txt','%s%f%f%f%f%f%f%f%f%f%f%f%f', 'delimiter',',');
fclose(fid);

% Read in numerical data
[x y] = textread(filename,'%f, %f','headerlines',1);
yn=y;
pts=length(x);

% subtract baseline
bl=input('What is the baseline value to subtract? ');
for ii=1:pts
    y(ii)=yn(ii)-bl;
end
yn=y;

% Find FWHM points in x
switch position
    case 532
    ymax=max(y(341:421));
    ii=379;
    case 527
    ymax=max(y(577:657));
    ii=620;
end
yhalfmax=ymax/2;
while y(ii)<yhalfmax
    ii=ii+1;
end
x1=x(ii-1);
y1=y(ii-1);
x2=x(ii);
y2=y(ii);
m=(y2-y1)/(x2-x1);
b=(y2-m*x2);
xlowhalf=(yhalfmax-b)/m;
while y(ii)>yhalfmax
    ii=ii+1;
end
x1=x(ii-1);
y1=y(ii-1);
x2=x(ii);
y2=y(ii);
m=(y2-y1)/(x2-x1);
```

```
b=(y2-m*x2);
xhighhalf=(yhalfmax-b)/m;
xfwhm_at_ymax=(xlowhalf+xhighhalf)/2;

choice=input('How will you determine x_max for the substrate peak?
1=Provide x_max, 2=Calculate x_max from FWHM? ');
% P2=1, P1=2
switch choice
    case 1
        x_at_ymax=input('Please input the Si substrate peak position:
');
        strained_Si_x_at_ymax=2*xfwhm_at_ymax-x_at_ymax;
    case 2
        x_at_ymax=xfwhm_at_ymax;
        strained_Si_x_at_ymax=xfwhm_at_ymax;
end

x_range=max(x)-x_at_ymax;
x_min=x_at_ymax-x_range;

ii=1;
while x(ii)<x_at_ymax
    if x(ii)<x_min
        yn(ii)=0;
        yp(ii)=0;
    else
        x_rel=x(ii)-x_at_ymax;
        x_other=x_at_ymax-x_rel;
        jj=pts;
        while x(jj)>x_other
            jj=jj-1;
        end
        x1=x(jj);
        y1=y(jj);
        x2=x(jj+1);
        y2=y(jj+1);
        m=(y2-y1)/(x2-x1);
        b=(y2-m*x2);
        yp(ii)=m*x_other+b;
        yn(ii)=y(ii)-yp(ii);
    end
    ii=ii+1;
end
while x(ii)<max(x)
    yp(ii)=y(ii);
    yn(ii)=0;
    ii=ii+1;
end
yp(ii)=y(pts);
yn(ii)=0;
plot(x,yn)
axis([490,530,-200,1000]);

% Find SiGe FWHM points in x, yn
switch position
    case 532
    ynmax=max(yn(341:379));
```

```
    ii=341;
    case 527
    ynmax=max(yn(577:619));
    ii=577;
end
ynhalfmax=ynmax/2;
while yn(ii)<ynhalfmax
    ii=ii+1;
end
x1=x(ii-1);
y1=yn(ii-1);
x2=x(ii);
y2=yn(ii);
m=(y2-y1)/(x2-x1);
b=(y2-m*x2);
xnlowhalf=(ynhalfmax-b)/m;
while yn(ii)>ynhalfmax
    ii=ii+1;
end
x1=x(ii-1);
y1=yn(ii-1);
x2=x(ii);
y2=yn(ii);
m=(y2-y1)/(x2-x1);
b=(y2-m*x2);
xnhighhalf=(ynhalfmax-b)/m;
x_at_ynmax=(xnlowhalf+xnhighhalf)/2;

% Find tensile Si FWHM points in x, yn
switch position
    case 532
    yomax=max(yn(379:421));
    ii=379;
    case 527
    yomax=max(yn(619:657));
    ii=619;
end
yohalfmax=yomax/2;
while yn(ii)<yohalfmax
    ii=ii+1;
end
x1=x(ii-1);
y1=yn(ii-1);
x2=x(ii);
y2=yn(ii);
m=(y2-y1)/(x2-x1);
b=(y2-m*x2);
xolowhalf=(yohalfmax-b)/m;
while yn(ii)>yohalfmax
    ii=ii+1;
end
x1=x(ii-1);
y1=yn(ii-1);
x2=x(ii);
y2=yn(ii);
m=(y2-y1)/(x2-x1);
b=(y2-m*x2);
```

```
xohighhalf=(yohalfmax-b)/m;
x_at_yomax=(xolowhalf+xohighhalf)/2;

% Taken from data with Si substrate peak subtracted off
fprintf(1,'Si-Si peak location of SiGe layer                    :
%8.2f\n',x_at_ynmax);
% Taken from raw data
fprintf(1,'Si-Si peak location of tensile Si (from yn)         :
%8.2f\n',x_at_yomax);
% Taken from raw data
fprintf(1,'Si-Si peak location of tensile Si (from FWHM of y):
%8.2f\n',strained_Si_x_at_ymax);
% Taken from raw data
fprintf(1,'Si-Si peak location of Si substrate                 :
%8.2f\n',x_at_ymax);

% Save data into a file
savefilename=input('Please input the filename to save data:','s');
sfid = fopen(savefilename,'w');
fprintf(sfid,'Original filename: %s\n',filename);
fprintf(sfid,'%s, %s, %s, %s\n','Wavenumber','New Raman trace','Peak
trace','Measured data');
for jj=1:pts
    fprintf(sfid,'%f, %f, %f, %f\n',x(jj),yn(jj),yp(jj),y(jj));
end
fprintf(sfid,'Program p2.m\n');
fprintf(sfid,'Choice: %f\n',choice);
fprintf(sfid,'Peak location of Si substrate Si-Si peak:
%f\n',x_at_ymax);
fprintf(sfid,'Peak location of SiGe layer Si-Si peak:
%f\n',x_at_ynmax);
fprintf(sfid,'Peak location of tensile Si (from yn) Si-Si peak:
%f\n',x_at_yomax);
fprintf(sfid,'Peak location of tensile Si (from FWHM of y):
%f\n',strained_Si_x_at_ymax);
fclose(sfid);
```

C.2 Numerical Simulation of Lateral Relaxation of a Single SiGe Layer

This script is used to numerically simulate the lateral relaxation of a rectangular island consisting of a single $Si_{0.7}Ge_{0.3}$ layer. The equations used in this program are given in Chapter 4 (Eqns. 4.3 and 4.5). This script has been adapted from an original script provided by Rui Huang [142,198], which was valid for square geometries. For this work, the script was expanded to be valid for rectangular geometries of any aspect ratio, and the data output was enhanced. There is one line that requires adjustment to specify at which simulation points the data should be saved.

C.2.1 Matlab Script for Lateral Relaxation

```
% relaxation of SiGe film on glass, 2D model
% film9.m

clear;

% SiGe composition
ge = 0.3;
si = 1 - ge;

% elastic constants
c11 = 16.48*si + 12.85*ge;
c12 =  6.35*si +  4.83*ge;
c66 =  7.90*si +  6.68*ge;

% c_hat
ct11 = c11 - c12^2/c11;
ct12 = c12 - c12^2/c11;

% c_bar
cb11 = ct11/c11;
cb12 = ct12/c11;
cb66 = c66/c11;

% initial mismatch strain, assume Si0.7Ge0.3
e0 = -0.012;

% Normalize average thickness strain
e0z=-2*e0*c12/c11;
% Normalize displacement
un=-e0/2;

% space discretization
% M,N should be even
% M is for x-direction, N is for y-direction
% A is aspect ratio
A=input('Enter the aspect ratio (# of squares) of the island: ');
M=60;
N=round(A*M);
dx = 1/M;
dy = dx;

% initial displacement
u = zeros(M+3,N+3);
v = zeros(M+3,N+3);

% time integration
tfinal=input('Enter the final time in units of 1/tL (e.g. 0.01): ');
dt = 0.0001;
NT = round(tfinal/dt)+1;

% create x1, y1 matrix with dimensions of (M+3)x(N+3) for plotting x1,
% y1 go between -0.5 and +0.5 in units of x/Lx and y/Ly
for i=1:M+3
    for j=1:N+3
        x1(i,j)=(i-2-M/2)/M;
```

```
        y1(i,j)=A*(j-2-N/2)/N;
    end
end

% create x2, y2 matrix with dimensions of (M+1)x(N+1) for plotting
% x2, y2 go between -0.5 and +0.5 in units of x/Lx and y/Ly
for i = 1:M+1
    for j = 1:N+1
        x2(i,j)=(i-1-M/2)/M;
        y2(i,j)=A*(j-1-N/2)/N;
    end
end

for k = 1:NT
    fprintf(1,'%d ',k)
    t_tE(k)=dt*(k-1);

    if k>1
       % displacements of the fictitious nodes to satisfy boundary
conditions
       % set values for 8 edge pts right next to four corners by
relationship
       % to 2nd nearest neighbors in same direction
        % exx = 0
        u(1,2) = u(3,2) + e0*dx*2;
        v(1,2) = v(3,2);
        u(M+3,2) = u(M+1,2) - e0*dx*2;
        v(M+3,2) = v(M+1,2);
        u(1,N+2) = u(3,N+2) + e0*dx*2;
        v(1,N+2) = v(3,N+2);
        u(M+3,N+2) = u(M+1,N+2) - e0*dx*2;
        v(M+3,N+2) = v(M+1,N+2);

        % eyy = 0
        u(2,1) = u(2,3);
        v(2,1) = v(2,3) + e0*dy*2;
        u(M+2,1) = u(M+2,3);
        v(M+2,1) = v(M+2,3) + e0*dy*2;
        u(2,N+3) = u(2,N+1);
        v(2,N+3) = v(2,N+1) - e0*dy*2;
        u(M+2,N+3) = u(M+2,N+1);
        v(M+2,N+3) = v(M+2,N+1) - e0*dy*2;

        % Assign values for four corners equal to nearest neighbors in
        % opposite direction
        u(1,1) = u(1,2);
        v(1,1) = v(2,1);
        u(1,N+3) = u(1,N+2);
        v(1,N+3) = v(2,N+3);
        u(M+3,1) = u(M+3,2);
        v(M+3,1) = v(M+2,1);
        u(M+3,N+3) = u(M+3,N+2);
        v(M+3,N+3) = v(M+2,N+3);

        % Create values for rest of edges
        for i = 3:M+1
            % exy = 0
```

```
        u(i,1) = u(i,3) + v(i+1,2) - v(i-1,2);
        % sigma_yy = 0
        v(i,1) = v(i,3) + 2*dx*e0*(1+ct12/ct11) +
                 ct12/ct11*(u(i+1,2)-u(i-1,2));
        % exy = 0
        u(i,N+3) = u(i,N+1) - (v(i+1,N+2) - v(i-1,N+2));
        % sigma_yy = 0
        v(i,N+3) = v(i,N+1) - 2*dx*e0*(1+ct12/ct11) -
                 ct12/ct11*(u(i+1,N+2)-u(i-1,N+2));
    end
    for j = 3:N+1
        % sigma_xx = 0
        u(1,j) = u(3,j) + 2*dx*e0*(1+ct12/ct11) +
                 ct12/ct11*(v(2,j+1)-v(2,j-1));
        % exy = 0
        v(1,j) = v(3,j) + u(2,j+1) - u(2,j-1);
        % sigma_xx = 0
        u(M+3,j) = u(M+1,j) - 2*dx*e0*(1+ct12/ct11) -
                 ct12/ct11*(v(M+2,j+1)-v(M+2,j-1));
        % exy = 0
        v(M+3,j) = v(M+1,j) - (u(M+2,j+1) - u(M+2,j-1));
    end
else
end

% Strains of the real nodes
for i = 1:M+1
    for j = 1:N+1
        % Equation 4.2a
        ex(i,j) = e0 + (u(i+2,j+1) - u(i,j+1))/dx/2;
        % Equation 4.2b
        ey(i,j) = e0 + (v(i+1,j+2) - v(i+1,j))/dy/2;
        % Equation 3.8
        ez(i,j) = -c12/c11*(ex(i,j) + ey(i,j));
    end
end

% displacement rate of the real nodes
for i = 2:M+2
    for j = 2:N+2
        % Equation 4.1a
        du(i,j) = cb11*(u(i+1,j)-2*u(i,j)+u(i-1,j))/dx^2 +...
                  cb66*(u(i,j+1)-2*u(i,j)+u(i,j-1))/dy^2 +...
                  (cb12+cb66)*(v(i+1,j+1)-v(i+1,j-1)-v(i-
                  1,j+1)+v(i-1,j-1))/dx/dy/4;
        % Equation 4.1b
        dv(i,j) = cb11*(v(i,j+1)-2*v(i,j)+v(i,j-1))/dy^2 +...
                  cb66*(v(i+1,j)-2*v(i,j)+v(i-1,j))/dx^2 +...
                  (cb12+cb66)*(u(i+1,j+1)-u(i+1,j-1)-u(i-
                  1,j+1)+u(i-1,j-1))/dx/dy/4;
    end
end

% update displacements of the real nodes
for i = 2:M+2
    for j = 2:N+2
        u(i,j) = u(i,j) + du(i,j)*dt;
```

```
            v(i,j) = v(i,j) + dv(i,j)*dt;
        end
    end

    % After strains and positions are calculated

    % thickness strain at the center
    el(k) =ez(M/2+1,N/2+1);
    exc(k)=ex(M/2+1,N/2+1);
    eyc(k)=ey(M/2+1,N/2+1);

    % average thickness strain across full area;
    % average x, y strain across center slices of island
    ebz(k) = 0;
    ebx(k) = 0;
    eby(k) = 0;
    for i = 1:M
        ebx(k)=ebx(k)+ex(i,N/2+1)*dx;
        for j = 1:N
            ebz(k) = ebz(k) + (ez(i,j) + ez(i+1,j) + ez(i,j+1) +
            ez(i+1,j+1))*dx*dy/4/A;
            if i==M/2+1
                eby(k)=eby(k)+ey(M/2+1,j)*dy/A;
            else
            end
        end
    end

    % If t is at a designated time, plot, save data, etc.
    t=round(t_tE(k)*1e4)/1e4;
    % THE BELOW LINE MUST BE CHANGED TO SPECIFY POINTS AT WHICH TO SAVE
DATA
    if (t==6)+(t==10)+(t==0.0015)
        fprintf(1,'\nt_tE = %f\n',t);
        % Calculate cross-sections
        % should only consider u, v for indices 2:N+2 (not 1, not N+3)
        for i=2:M+2
            uxfinal(i-1)=u(i,N/2+1);
            ezxfinal(i-1)=ez(i-1,N/2+1);
            exfinal(i-1)=ex(i-1,N/2+1);
            x(i-1)=x1(i,N/2+1);
        end
        for i=2:N+2
            vyfinal(i-1)=v(M/2+1,i);
            ezyfinal(i-1)=ez(M/2+1,i-1);
            eyfinal(i-1)=ey(M/2+1,i-1);
            y(i-1)=y1(M/2+1,i);
        end

        ymax=max(y);
        ymin=min(y);

        % Like Fig 3 (a)
        subplot(3,3,4);
        plot(x,uxfinal/un)
        axis([-0.5 +0.5 -1.5 1.5])
        xlabel('x/L_x')
```

```
ylabel('Normalized x-displacement')
subplot(3,3,5);
plot(y,vyfinal/un)
axis([ymin ymax -1.5 1.5])
xlabel('y/L_x')
ylabel('Normalized y-displacement')
% Like Fig 3 (b)
subplot(3,3,1);
plot(x,ezxfinal/e0z)
axis([-0.5 +0.5 0 1])
xlabel('x/L_x')
ylabel('Normalized thickness strain')
subplot(3,3,2);
plot(y,ezyfinal/e0z)
axis([ymin ymax 0 1])
xlabel('y/L_x')
ylabel('Normalized thickness strain')
% full 2D
subplot(3,3,7);
surf(x2,y2,ex/e0,'EdgeColor','none')
colormap(cool)
camlight left
lighting phong
axis([-0.5 +0.5 ymin ymax -1 1])
xlabel('x/L_x')
ylabel('y/L_x')
zlabel('Normalized x-strain')

subplot(3,3,8);
surf(x2,y2,ey/e0,'EdgeColor','none')
colormap(cool)
camlight left
lighting phong
axis([-0.5 +0.5 ymin ymax -1 1])
xlabel('x/L_x')
ylabel('y/L_x')
zlabel('Normalized y-strain')

subplot(3,3,3);
surf(x2,y2,ez/e0z,'EdgeColor','none')
colormap(cool)
camlight left
lighting phong
view(-15,65)
axis([-0.5 +0.5 ymin ymax 0 1])
xlabel('x/L_x')
ylabel('y/L_x')
zlabel('Normalized thickness strain')
% Like Fig 4
subplot(3,3,9);
plot(t_tE,ebz/e0z)
axis([0 tfinal 0 1])
xlabel('t/t_E')
ylabel('Normalized average thickness strain')

% Save data into a file
```

```
        savefilename=input('Please input the filename to save
data:','s');
        sfid = fopen(savefilename,'w');
        fprintf(sfid,'Save filename: \t%s\n',savefilename);
        fprintf(sfid,'Program \tfilm9.m\n');
        fprintf(sfid,'x-spatial dimension, M: \t%f\n',M);
        fprintf(sfid,'y-spatial dimension, N: \t%f\n',N);
        fprintf(sfid,'dx: \t%f\n',dx);
        fprintf(sfid,'dy: \t%f\n',dy);
        fprintf(sfid,'Number of time increments, k: \t%f\n',k);
        fprintf(sfid,'Time increment, dt: \t%f\n',dt);
        fprintf(sfid,'tfinal [t/tE]: \t%f\n',t);
        fprintf(sfid,'ez_areaavg(tfinal): \t%f\n',ebz(k)/e0z);
        fprintf(sfid,'ex_midavg(tfinal): \t%f\n',ebx(k)/e0);
        fprintf(sfid,'ey_midavg(tfinal): \t%f\n',eby(k)/e0);
        fprintf(sfid,'ez_center(tfinal) : \t%f\n',e1(k)/e0z);
        fprintf(sfid,'ex_center(tfinal) : \t%f\n',exc(k)/e0);
        fprintf(sfid,'ey_center(tfinal) : \t%f\n',eyc(k)/e0);

        fprintf(sfid,'\n%s\t%s\t%s\t%s\n','x/L','u_xdirmid','ez_xdirmid
        ', 'ex_mid');
        for i=1:M+1
            fprintf(sfid,'%f\t%f\t%f\t%f\n',x(i),uxfinal(i)/un,
            ezxfinal(i)/e0z,exfinal(i)/e0);
        end

         fprintf(sfid,'\n%s\t%s\t%s\t%s\n','y/L','v_ydirmid','ez_ydirmi
        d', 'ey_mid');
        for i=1:N+1
            fprintf(sfid,'%f\t%f\t%f\t%f\n',y(i),vyfinal(i)/un,
            ezyfinal(i)/e0z,eyfinal(i)/e0);
        end

         fprintf(sfid,'\n%s\t%s\t%s\t%s\t%s\t%s\t%s\n','t/tE','ez_areaa
        vg(t)',
        'ex_midavg(t)','ey(midavg(t)','ez_center(t)','ex_center(t)',
        'ey_center(t)');
        for i=1:k

            fprintf(sfid,'%f\t%f\t%f\t%f\t%f\t%f\t%f\n',t_tE(i),ebz(i)/
            e0z, ebx(i)/e0,eby(i)/e0,e1(i)/e0z,exc(i)/e0,eyc(i)/e0);
        end
        fprintf(sfid,'\n%s\n','columns: x/L, rows: y/L, array:
ez/e0z');
        fprintf(sfid,'\t');
        for i=1:M+1
            fprintf(sfid,'%f\t',x(i));
        end
        fprintf(sfid,'\n');
        for j=1:N+1
            fprintf(sfid,'%f\t',y(j));
            for i=1:M+1
                fprintf(sfid,'%f\t',ez(i,j)/e0z);
            end
            fprintf(sfid,'\n');
        end
        fprintf(sfid,'\n%s\n','columns: x/L, rows: y/L, array: ex/e0');
```

```
        fprintf(sfid,'\t');
        for i=1:M+1
            fprintf(sfid,'%f\t',x(i));
        end
        fprintf(sfid,'\n');
        for j=1:N+1
            fprintf(sfid,'%f\t',y(j));
            for i=1:M+1
                fprintf(sfid,'%f\t',ex(i,j)/e0);
            end
            fprintf(sfid,'\n');
        end
        fprintf(sfid,'\n%s\n','columns: x/L, rows: y/L, array: ey/e0');
        fprintf(sfid,'\t');
        for i=1:M+1
            fprintf(sfid,'%f\t',x(i));
        end
        fprintf(sfid,'\n');
        for j=1:N+1
            fprintf(sfid,'%f\t',y(j));
            for i=1:M+1
                fprintf(sfid,'%f\t',ey(i,j)/e0);
            end
            fprintf(sfid,'\n');
        end
        fclose(sfid);

        hold=input('Save fig, emf and close Fig window, then press
        enter to plot x-strain: ');
        surf(x2,y2,ex/e0,'EdgeColor','none')
        colormap(cool)
        camlight left
        lighting phong
        axis([-0.5 +0.5 ymin ymax -1 1])
        xlabel('x/L_x')
        ylabel('y/L_x')
        zlabel('Normalized x-strain')
        hold=input('Save fig, emf, then press enter to plot y-strain:
');
        surf(x2,y2,ey/e0,'EdgeColor','none')
        colormap(cool)
        camlight left
        lighting phong
        axis([-0.5 +0.5 ymin ymax -1 1])
        xlabel('x/L_x')
        ylabel('y/L_x')
        zlabel('Normalized y-strain')
        hold=input('Save fig, emf, then press enter to continue
        simulation: ');
    else
    end
end

% After final positions are calculated
hold=input('Done. Press enter to finish: ');
```

C.3 Buckling Model

This script is used to calculate buckling time constants for 1-D and 2-D buckling of a thin $Si_{0.7}Ge_{0.3}$ film on BPSG, using Eqns. 6.3-6.8 and 6.22.

C.3.1 Matlab Script for Linear Perturbation Model

```
%Program buckling

%Initialization and Input
format compact
close
clear all
warning off

% SiGe thickness, m
hf=1e-9*input('SiGe thickness in nm: ');

% SiGe strain (compressive<0, tensile>0), assume 30% SiGe
eo=-0.012;

angledeg=input('Angle for <100> in (001) plane, in degrees: ');
angle=(pi/180)*angledeg;

% For (001) surface plane, 30% SiGe
s11=8.24;
s12=-2.28;
s44=13.27;
s=(s11-s12-0.5*s44);

% SiGe Poisson Ratio, unitless
v=-(2*s12+s*(sin(2*angle))^2)/(2*s11-s*(sin(2*angle))^2);

% SiGe Young's modulus, N/m/m
E=(1/(s11-0.5*s*(sin(2*angle))^2))*1e12;

sigmao=E*eo/(1-v);

% c, unitless, eyy=(1-c)*eo
OneDor2D=menu('Buckling type','1D','2D');
switch OneDor2D
   case 1
      c=1+v;
      Btype='1D';
   case 2
      c=0;
      Btype='2D';
end
fprintf(1,'%s\n',Btype);

n=input('Viscosity, N*sec/m/m=');
```

```
% Critical wavenumber 1/nm
kc=sqrt(-12*eo*(1+v-v*c))/hf*1e-9;

% lambda in units of um
lambdac=2*pi/kc/1e3;

hgmenu=menu('hg:','range','specific value');
switch hgmenu
    case 1
        hgnm=10:10:1100;
    case 2
        hgnm=input('Hg thickness in nm: ');
end
% BPSG thickness, nm --> m
hg=hgnm*1e-9;
lengthhg=length(hg);
% Wavenumber 1/m
k=0:2e4:3e7;
lengthk=length(k);

for ii=1:lengthhg
    for jj=1:lengthk
        % Huang and Suo (2002-IJSS)
        gamma11(jj)=0.5*(sinh(2*k(jj)*hg(ii))-
        2*k(jj)*hg(ii))/((k(jj)*hg(ii))^2+(cosh(k(jj)*hg(ii)))^2);

        gamma22(jj)=0.5*(sinh(2*k(jj)*hg(ii))+2*k(jj)*hg(ii))/((k(jj)*h
        g(ii)) ^2+(cosh(k(jj)*hg(ii)))^2);

        gamma12(jj)=(k(jj)*hg(ii))^2/((k(jj)*hg(ii))^2+(cosh(k(jj)*hg(i
        i)))^2 );
        alphanew(jj)=E*k(jj)*hf/24/n/(1-v^2)*(-12*eo*(1+v-v*c)-
        (k(jj)*hf)^2)*gamma11(jj);
        betanew(jj)=E*k(jj)*hf/2/n/(1-v^2)*gamma22(jj);
        S1new(jj)=0.5*(alphanew(jj)-betanew(jj)+sqrt((alphanew(jj)-
        betanew(jj))^2+4*alphanew(jj)*betanew(jj)*(1-
        gamma12(jj)^2/gamma11(jj)/gamma22(jj))));
        if jj>1
            dS1newdk(jj)=(S1new(jj)-S1new(jj-1))/(k(jj)-k(jj-1));
        else
        end
    end

    % S1new in units of 1/sec
    maxS1new(ii)=max(S1new);
    % kmnew in units of 1/nm
    [i,j]=find(S1new==maxS1new(ii));
    kmnew(ii)=k(j)*1e-9;
    % lambdamnew in units of um
    lambdamnew(ii)=2*pi/kmnew(ii)/1e3;
    % TauS1new in units of sec
    TauS1new(ii)=1/maxS1new(ii);
end

% Save data into a file
savefilename=input('Please input the filename to save data:','s');
```

```
sfid = fopen(savefilename,'w');
fprintf(sfid,'Save filename: \t%s\n',savefilename);
fprintf(sfid,'Program \tbuckling.m\n');
fprintf(sfid,'SiGe thickness [nm]: \t%f\n',hf*1e9);
fprintf(sfid,'Angle (degrees): \t%f\n',angledeg);
fprintf(sfid,'SiGe strain (compressive<0, tensile>0): \t%f\n',eo);
fprintf(sfid,'SiGe Poisson Ratio [unitless]: \t%f\n',v);
fprintf(sfid,'SiGe Young''s modulus [N/m/m]: \t%f\n',E);
fprintf(sfid,'Buckling type: \t%s\n',Btype);
fprintf(sfid,'C: \t%f\n',c);
fprintf(sfid,'BPSG viscosity [N*sec/m/m]: \t%f\n',n);
fprintf(sfid,'kc [1/nm]: \t%f\n',kc);
fprintf(sfid,'Lambda c [um]: \t%f\n',lambdac);

switch hgmenu
case 1
case 2
   fprintf(sfid,'%s\t%s\t%s\t%s\t%s\t%s\t%s\t%s\t%s\n','kh','k [1/m]',
   'lambda [um]','gamma11','gamma22','gamma12','alpha [1/sec]','beta
   [1/sec]','S1 [1/sec]');
   for jj=1:lengthk
   fprintf(sfid,'%f\t%f\t%f\t%f\t%f\t%f\t%f\t%f\t%f\n',k(jj)*hf,k(jj),
   2*pi*1e6/k(jj),gamma11(jj),gamma22(jj),gamma12(jj),alphanew(jj),
   betanew(jj),S1new(jj));
   end
end

fprintf(sfid,'%s\t%s\t%s\t%s\t%s\n','hg [nm]','kmnew
[1/nm]','lambdamnew [um]','maxS1new [1/sec]','TauS1new [sec]');
for ii=1:lengthhg

   fprintf(sfid,'%f\t%f\t%f\t%f\t%f\n',hgnm(ii),kmnew(ii),lambdamnew(ii
   ), maxS1new(ii),TauS1new(ii));
end
fclose(sfid);
ii=1;
fprintf(1,'%f%s\t%f%s\t%f%s\n',hgnm(ii),' nm',TauS1new(ii),'
sec',TauS1new(ii)/60,' min');
```

C.4 Automated Analysis of MOSFET I-V Data

This script is used to analyze measurements of MOSFET current-voltage characteristics, to extract mobility, threshold voltage, and sub-threshold slope, as described in Sec. 7.3.2, and to output the data and extracted parameter values to a text file.

C.4.1 Matlab Script for MOSFET I-V Analysis

```
% Plotting and analyzing IV data from HP4155A
% for one file of I-VG, one VDS, one Vsub

close;
clear all;
warning off;

% Ask for a file name
filename=input('Please input the directory\\filename: ','s');
ch=menu('Channel type:','n','p');
switch ch
    case 1
        chsign=1;
        var2(1)=+0.1;
    case 2
        chsign=-1;
        var2(1)=-0.1;
end

% Read in header info
fid=fopen(filename,'r');
line1=fgets(fid);
line2=fgets(fid);
line3=fgets(fid);
line4=fgets(fid);
%line5=fgets(fid);
sfid=fopen('temp.txt','w');
fprintf(sfid,line2);
fprintf(sfid,line3);
fclose(sfid);
[var minv a maxv b step c]=textread('temp.txt','%s %f %s %f %s %f
%s',1);
fclose(fid);

% Process header data
var1pts=abs((maxv(1)-minv(1))/step(1))+1;
var2sweeps=1;
minvar1=min(maxv(1),minv(1));
maxvar1=max(maxv(1),minv(1));

% Read in numerical data
[no Vtmp IDtmp] = textread(filename,'%f %f %f','headerlines',4);

% Reorganize numerical data
for ii=1:var2sweeps
    for jj=1:var1pts
        V(jj,ii)=minv(1)+step(1)*(jj-1);
        if -chsign*IDtmp(jj+var1pts*(ii-1))>0
            ID(jj,ii)=chsign*1e-12;
            IDorig(jj,ii)=IDtmp(jj+var1pts*(ii-1));
        else
            ID(jj,ii)=IDtmp(jj+var1pts*(ii-1));
            IDorig(jj,ii)=IDtmp(jj+var1pts*(ii-1));
        end
    end
```

```
    VDS=var2(ii);
end

% Determine whether it's ID-VDS or ID-VGS
if length(var{1})==4
    fprintf(1,'File contains I-VDS data\n');
    type=1;
elseif length(var{1})==3
    %fprintf(1,'File contains I-VGS data\n');
    type=2;
end

% Take critical data points / make important calculations
switch type
   case 1
      % I-VDS
      % Determine ID,max and ID,min for each value of VGS
      IDmin=min(ID);
      IDmax=max(ID);
      VT=input('Please input VT (Volts): ');
   case 2
      Sample=input('Sample =','s');
      Quadrant=input('Quadrant =','s');
      island=input('Island size =','s');
      direction=input('Island direction | or / =','s');
      L=1e-4*input('Please input L (um): ');
      transistor=input('Transistor L or T =','s');
      W=1e-4*input('Please input W (um): ');
      % Assume 32 nm SiO2, Cox in F/cm/cm
      Cox=1.08e-7;

    % I-VGS
    % Create smoothed version of ID for gm and subslp calculations
    % sm is the number of points over which the average will be taken
(odd #)
    sm=5;
    for ii=1:var2sweeps
        for jj=1:((sm-1)/2)
           IDsm(jj,ii)=ID(jj,ii);
        end
        for jj=((sm+1)/2):(var1pts-(sm-1)/2)
           tally=0;
           for kk=((1-sm)/2):((sm-1)/2)
              tally=ID(jj+kk,ii)+tally;
           end
           IDsm(jj,ii)=tally/sm;
        end
        for jj=(var1pts-(sm+1)/2):var1pts
           IDsm(jj,ii)=ID(jj,ii);
        end
    end
    % Calculate gm and sub-VT slope vs. VGS
    % Also determine IDmin and IDmax
    for ii=1:var2sweeps
        for jj=1:(var1pts-1)
           gm(jj,ii)=(IDsm(jj+1,ii)-IDsm(jj,ii))/(V(jj+1,ii)-V(jj,ii));
           if V(jj,ii)>-14
```

```
            localgm(jj)=gm(jj,ii);
        else
        end
        if gm(jj,ii)>0
            Fl(jj,ii)=chsign*IDsm(jj,ii)/sqrt(gm(jj,ii));
        else
            Fl(jj,ii)=0;
        end
        localFl(jj)=Fl(jj,ii);
        if IDsm(jj+1,ii)==IDsm(jj,ii)
            subslp(jj,ii)=100000;
        else
            subslp(jj,ii)=-chsign*1000*((V(jj,ii)-
            V(jj+1,ii))/(log10(IDsm(jj+1,ii)/IDsm(jj,ii))));
        end
        if subslp(jj,ii)<0
            subslp(jj,ii)=1000;
        elseif subslp(jj,ii)>1000
            subslp(jj,ii)=1000;
        end
        localsubslp(jj)=subslp(jj,ii);
        sqrtID(jj,ii)=sqrt(-ID(jj,ii));
    end
    sqrtID(jj+1,ii)=sqrt(-ID(jj+1,ii));
    gm(jj+1,ii)=gm(jj,ii);
    Fl(jj+1,ii)=Fl(jj,ii);
    subslp(jj+1,ii)=subslp(jj,ii);
    [gmmax(ii), indexgmax(ii)]=max(localgm);
    [Flmax(ii), indexFlmax(ii)]=max(localFl);
    [subslpmin(ii), indexsubslpmin(ii)]=min(localsubslp);
end
IDmax=max(ID);
IDmin=min(ID);
% determine the gate voltage for maximum gm
% determine the threshold voltage using the linear Id vs Vgs
% determine the threshold voltage and mobility using Fl=ID/sqrt(gm)

for ii=1:var2sweeps
    fprintf(1,'%s%4.0f\n','Index for Gmmax = ',indexgmax(ii));
    fprintf(1,'%s%4.0f\n','Max Index = ',var1pts);
    theindex(ii)=input('Please input index for Vt determination:
');
    range=abs(0.5/step(1));
    % range is in units of index numbers

    % Calculates VT and mobility from linear fit of Fl-V at
    % VGS(gmmax) plus 2V, 0.5V
    % Calculates VT from linear fit of ID-VGS at VGS(gmmax) plus
2V, 0.5V
    if (((theindex(ii)+3*range)>0) &
(theindex(ii)+5*range)<(var1pts))

        [P2,S2]=polyfit(V((theindex(ii)+3*range):(theindex(ii)+5*ra
        nge),
        ii),Fl((theindex(ii)+3*range):(theindex(ii)+5*range),ii),1)
        ;
        F2Vt(ii)=-P2(2)/P2(1);
```

```
            F2A(ii)=(P2(1))^2;
            %F2A has units of (Amps/Volts)
            mob2(ii)=chsign*F2A(ii)*L/Cox/W/var2(ii);
            F2error(ii)=0;
            for iii=1:2*range+1
                F2error(ii)=F2error(ii)+abs(1-polyval(P2,V(theindex(ii)
                +3*range+iii-1))/F1(theindex(ii)+3*range+iii-1));
            end

            [X2,Z2]=polyfit(V((theindex(ii)+3*range):(theindex(ii)+5*ra
            nge),
            ii),ID((theindex(ii)+3*range):(theindex(ii)+5*range),ii),1)
            ;
            vt2(ii)=roots(X2);
            u2(ii)=X2(1)*L/W/Cox/var2(ii);
        end
    end
end

% Assign IDmax and min correctly with regards to sign
% (IDmax has larger amplitude)
for ii=1:var2sweeps
    IDsign(ii)=sign((IDmin(ii)+IDmax(ii))/2);
    if IDsign(ii)<0
        tempvar=IDmax(ii);
        IDmax(ii)=IDmin(ii);
        IDmin(ii)=tempvar;
    else
    end
    for jj=1:var1pts
        ueff(jj,ii)=chsign*(IDsm(jj,ii)*L)/(W*Cox*(V(jj)-F2Vt(ii)-
        VDS/2)*VDS);
        if chsign*V(jj)>chsign*F2Vt(ii)+1.0
            Flarray(jj)=F1(jj,ii);
            ueffarray(jj)=ueff(jj,ii);
        else
            Flarray(jj)=0;
            ueffarray(jj)=0;
        end

    end
    [Flmax(ii), indexFlmax(ii)]=max(Flarray);
    [ueffmax(ii), indexueffmax(ii)]=max(ueffarray);
    ueffplus0(ii)=ueffarray(theindex(ii));
    ueffplus2(ii)=ueffarray(theindex(ii)+4*range);
    ueffplus5(ii)=ueffarray(theindex(ii)+10*range);
    if (((theindex(ii)+19*range)>0) &
(theindex(ii)+21*range)<(var1pts))
        ueffplus10(ii)=ueffarray(theindex(ii)+20*range);
    else
        ueffplus10(ii)=0;
    end
    high=0;
    low=0;
    low2=0;
    jj=var1pts;
    while high==0
```

```
        if chsign*V(jj)<chsign*F2Vt(ii)
            high=1;
            Vhigh=V(jj);
            Ihigh=IDtmp(jj);
            jjj=jj;
            subslparray(jjj-jj+1)=subslp(jj,ii);
            jj=jj-1;
        else
            jj=jj-1;
        end
    end
    while low==0
        if chsign*IDtmp(jj)<chsign*Ihigh/1e3
        %if chsign*IDtmp(jj)<chsign*Ihigh/5e2
            low=1;
            Vlow=V(jj);
            Ilow=IDtmp(jj);
            subslparray(jjj-jj+1)=subslp(jj,ii);
            jj=jj-1;
        else
            subslparray(jjj-jj+1)=subslp(jj,ii);
            jj=jj-1;
        end
    end
    while (low2==0)&(jj~=0)
        if chsign*IDtmp(jj)<4e-12
            %if chsign*IDtmp(jj)<1e-10
            low2=1;
        else
            subslparray(jjj-jj+1)=subslp(jj,ii);
            jj=jj-1;
        end
    end
    subslpmin(ii)=min(subslparray);
    subslpeff(ii)=-chsign*1000*((Vhigh-Vlow)/(log10(Ilow/Ihigh)));
end

% Determine y-axis graph limits
 maxabsID=max(abs(max(IDtmp)),abs(min(IDtmp)));
 minabsID=min(abs(max(IDtmp)),abs(min(IDtmp)));
 pwr=floor(log10(maxabsID));
 numb=1+floor(maxabsID/10^pwr);
 IDmax_graph_max=IDsign(ii)*numb*10^pwr;
 IDmax_log_max=IDsign(ii)*10^(pwr+1);

 clear pwr numb;
 IDlin=IDmax(1);
 pwr=floor(log10(IDlin));
 numb=1+floor(IDlin/10^pwr);
 IDlin_graph=numb*10^pwr;

 switch type
 case 1
 case 2
 clear pwr numb;
 F1maxlin=F1max(1);
 pwr=floor(log10(F1maxlin));
```

```
numb=1+floor(F1maxlin/10^pwr);
F1maxlin_graph=numb*10^pwr;
%F1maxlin_graph=0.001;

clear pwr numb;
gmmaxlin=gmmax(1);
pwr=floor(log10(gmmaxlin));
numb=1+floor(gmmaxlin/10^pwr);
gmmaxlin_graph=numb*10^pwr;

clear pwr numb;
ueffmaxlin=ueffmax(1);
pwr=floor(log10(ueffmaxlin));
numb=1+floor(ueffmaxlin/10^pwr);
ueffmaxlin_graph=numb*10^pwr;

end


% Plot numerical data
% sp is the relative spacing between data output values
% of is the relative offset of ID-VGS data
sp=6;
of=6;
switch type
case 1
    % plot of ID vs. VDS
    subplot(2,3,1)
    plot(V,IDorig);
    xlabel('VDS (Volts)');
    title(['    ID vs. VDS']);
    axis([minvar1,maxvar1,0,0.0008]);
    ylabel('-ID (Amps)');
    axis square;
    grid;
    text(maxvar1+0.2*abs(maxvar1-
    minvar1),(1+1/sp)*abs(IDmax_graph_max),[' ',grtitle]);
    text(maxvar1+0.2*abs(maxvar1-
    minvar1),(1+of/sp)*abs(IDmax_graph_max),['VT=',num2str(VT)]);
    for ii=1:var2sweeps
            text(maxvar1+0.2*abs(maxvar1-minvar1),(1+(of-ii)/sp)
            *abs(IDmax_graph_max),[' ',num2str(IDmax(ii)),' A, for
            VGS-VT=',num2str(var2(ii)-VT),' V']);
    end
case 2
    % plot of ID (log) vs VGS
    subplot(3,3,1)
    semilogy(V,chsign*IDorig);
    xlabel('VGS (Volts)');
    title(['    ID vs VGS']);
    axis([minvar1,maxvar1,1e-14,abs(IDmax_log_max)]);
    ylabel('-ID (Amps)');
    axis square;
    grid;
    % plot of ID (linear) vs VGS
    subplot(3,3,2)
    plot(V,chsign*IDorig);
```

```
    xlabel('VGS (Volts)');
    title(['    ID vs. VGS']);
    axis([minvar1,maxvar1,0,abs(IDlin_graph)]);
    ylabel('-ID (Amps)');
    axis square;
    grid;
    % plot of F1 vs. VGS
    subplot(3,3,5)
    plot(V,F1);
    xlabel('VGS (Volts)');
    title(['      F1 vs. VGS']);
    ylabel('-F1');
    axis([minvar1,maxvar1,0,F1maxlin_graph]);
    axis square;
    grid;
    text(maxvar1+0.2*abs(maxvar1-
     minvar1),F1maxlin_graph*(1+(of+1)/sp),[Sample,Quadrant]);
    text(maxvar1+0.2*abs(maxvar1-
     minvar1),F1maxlin_graph*(1+(of)/sp),[island,' island,
     ',num2str(L*1e4),transistor,'x',num2str(W*1e4),' ',direction,'
     transistor']);
    text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
     1)/sp),[filename]);
    of=of+1;
    for ii=1:var2sweeps
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10+6)/sp),[' for VDS= ',num2str(var2(ii)),' V']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10+5)/sp),[' IDmax= ',num2str(IDmax(ii)),' A']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10+4)/sp),[' IDmin= ',num2str(IDmin(ii)),' A,
        Imax/Imin=',num2str(IDmax(ii)/IDmin(ii))]);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10+3)/sp),[' gmmax= ',num2str(gmmax(ii)),' A/V']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10+2)/sp),[' SubVT slope= ',num2str(subslpmin(ii)),'
        mV/dec']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10+1)/sp),[' SubVt slope eff= ', num2str(subslpeff(ii)),'
        mV/dec']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10+0)/sp),[' mobility eff max= ', num2str(ueffmax(ii)),'
        cm*cm/V/sec']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10-1)/sp),[' Voltage at chosen index =
        ',num2str(V(theindex(ii))),' V']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10-4)/sp),[' VTlin #2= ', num2str(vt2(ii)),' V']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10-5)/sp),[' mobilitylin #2= ', num2str(u2(ii)),' V']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10-6)/sp),[' VTlin fit #2= ', num2str(F2Vt(ii)),' V']);
        text(maxvar1+0.2*abs(maxvar1-minvar1),F1maxlin_graph*(1+(of-
        ii*10-7)/sp),[' mobility fit #2= ', num2str(mob2(ii)),'
        cm*cm/V/sec']);
    end
end
```

```
% Plot data

switch type
case 1
    % plot of IG vs. VDS
    subplot(2,3,4)
    plot(V,IG);
    xlabel('VDS (Volts)');
    title(['      IG vs. VDS']);
    ylabel('IG (Amps)');
    axis([minvar1,maxvar1,-40e-12,+40e-12]);
    axis square;
    grid;
case 2
    % plot of ueff vs. VGS
    subplot(3,3,8)
    plot(V,ueff);
    xlabel('VGS (Volts)');
    ylabel('ueff (cm*cm/Volts/sec)');
    title(['    ueff vs. VGS']);
    axis([minvar1,maxvar1,0,ueffmaxlin_graph]);
    axis square;
    grid;
    % plot of gmlin vs. VGS
    subplot(3,3,7)
    plot(V,gm);
    xlabel('VGS (Volts)');
    ylabel('-gmlin (Amps/Volts)');
    title(['    gm vs. VGS']);
    axis([minvar1,maxvar1,0,gmmaxlin_graph]);
    axis square;
    grid;
    % plot of sub-VT slop vs. VGS
    subplot(3,3,4)
    semilogy(V,subslp);
    xlabel('VGS (Volts)');
    ylabel('-Sub-Threshold Slope (mV/dec)');
    title(['    Sub-VT slope vs. VGS']);
    axis([minvar1,maxvar1,10,2000]);
    axis square;
    grid;
end

switch type
    case 1
    case 2
        switch ch
            case 1
                subplot(3,3,1)
                ylabel('ID (Amps)');
                subplot(3,3,2)
                ylabel('ID (Amps)');
                subplot(3,3,5)
                ylabel('F1');
                subplot(3,3,8)
                ylabel('ueff (cm*cm/Volt-sec)');
```

```
                subplot(3,3,7)
                ylabel('gmlin (Amps/Volts)');
                subplot(3,3,4)
                ylabel('Sub-Threshold Slope (mV/dec)');
            case 2
        end
end

orient landscape;

% Save data into a file that is formatted for Origin or Excel
% (each data set it it's own column)
savefilename=input('Please input the filename to save iv data for
origin or excel:','s');
sfid = fopen(savefilename,'w');
fprintf(sfid,'\t%s%s\n','Original filename: ',filename);
fprintf(sfid,'%s%s%s%s%s%s%s%s%s%s%s%s%s%s\n',Sample,Quadrant,',
',filename,', ',island,' island,
',num2str(L*1e4),transistor,'x',num2str(W*1e4),' ',direction,'
transistor');
fprintf(sfid,line2);
fprintf(sfid,line3);

switch type
case 1
    fprintf(sfid,'%s\t%e\n','VT = ',VT);
fprintf(sfid,'%s\t','VDS');
for ii=1:var2sweeps
    fprintf(sfid,'%s\t%s\t','ID','IG');
end
fprintf(sfid,'\n');
fprintf(sfid,'%s\t','V');
for ii=1:var2sweeps
    fprintf(sfid,'%s\t%s\t','A','A');
end
fprintf(sfid,'\n');
fprintf(sfid,'%s\t','VGS-VT');
for ii=1:var2sweeps
    fprintf(sfid,'%f\t%f\t',var2(ii)-VT,var2(ii)-VT);
end
fprintf(sfid,'\n');
for jj=1:var1pts
        fprintf(sfid,'%e',V(jj,1));
        for ii=1:var2sweeps
           fprintf(sfid,'\t%e\t%e',IDorig(jj,ii),IG(jj,ii));
        end
        fprintf(sfid,'\n');
   end
case 2
fprintf(sfid,'%s\t%f\n','L(um)=',L*1e4);
fprintf(sfid,'%s\t%f\n','W(um)=',W*1e4);
fprintf(sfid,'%s\t%e\n\n','Cox(F/cm/cm)=',Cox);
for ii=1:var2sweeps
        fprintf(sfid,'%s\t%s\t%s\n',' for VDS= ',num2str(var2(ii)),'
V');
        fprintf(sfid,'%s\t%s\t%s\n',' IDmax= ',num2str(IDmax(ii)),'
A');
```

```
          fprintf(sfid,'%s\t%s\t%s\t%s\n',' IDmin=
          ',num2str(IDmin(ii)),' A,
          Imax/Imin=',num2str(IDmax(ii)/IDmin(ii)));
          fprintf(sfid,'%s\t%s\t%s\n',' gmmax= ',num2str(gmmax(ii)),'
A/V');
          fprintf(sfid,'%s\t%s\t%s\n',' SubVT slope=
          ',num2str(subslpmin(ii)),' mV/dec');
          fprintf(sfid,'%s\t%s\t%s\n',' SubVT slope eff=
          ',num2str(subslpeff(ii)),' mV/dec');
          fprintf(sfid,'%s\t%s\t%s\n',' mobility eff max= ',
          num2str(ueffmax(ii)),' cm*cm/V/sec');
          fprintf(sfid,'%s\t%4.0f\n','Chosen index = ',theindex(ii));
          fprintf(sfid,'%s\t%4.3f\t%s\n','Voltage at chosen index =
          ',V(theindex(ii)),' Volts');
          fprintf(sfid,'%s\t%s\t%s\n',' VTlinfit #2= ',
          num2str(F2Vt(ii)),' V');
          fprintf(sfid,'%s\t%s\t%s\n',' VTlin #2= ', num2str(vt2(ii)),'
V');
          fprintf(sfid,'%s\t%s\t%s\n\n',' mobilityfit #2= ',
          num2str(mob2(ii)),' cm*cm/V/sec');
          fprintf(sfid,'%s\t%s\t%s\n',' mobility lin #2= ',
          num2str(u2(ii)),' cm*cm/V/sec');
          fprintf(sfid,'%s\t%s\t%s\n','F2 error =
          ',num2str(F2error(ii)*100),' %');
          fprintf(sfid,'%s\t%s\t%s\n\n','mobility eff at #2=
          ',num2str(ueffplus2(ii)),' cm*cm/V/sec');
       end
      fprintf(sfid,'%s\t','VGS');
 for ii=1:var2sweeps

fprintf(sfid,'%s\t%s\t%s\t%s\t%s\t%s\t','ID','gm','subslp','ueff','IDsm');
 end
 fprintf(sfid,'\n');
 fprintf(sfid,'%s\t','V');
 for ii=1:var2sweeps
     fprintf(sfid,'%s\t%s\t%s\t%s\t%s\t%s\t','A','A/V','mV/dec','cm*cm/V-
     sec','A');
 end
 fprintf(sfid,'\n');
     for jj=1:varlpts
          fprintf(sfid,'%e',V(jj,1));
          for ii=1:var2sweeps

             fprintf(sfid,'\t%e\t%e\t%e\t%e\t%e',IDorig(jj,ii),gm(jj,ii)
             , subslp(jj,ii),ueff(jj,ii),IDsm(jj,ii));
          end
          fprintf(sfid,'\n');
     end
 end

fclose('all');
```

Appendix D

RTCVD Growth Sequences Used In This Work

This appendix provides the rapid thermal chemical vapor deposition (RTCVD) growth sequences used in this work. The growth sequences are for use with the DAQ Factory control software, which was installed in August 2003 to replace the Control-EG program. Sec. D.1 provides a recipe for epitaxially regrowing single-crystal silicon to thicken the strained-silicon channels. In Sec. D.2 and D.3, the sequences needed to deposit n+ and p+ poly silicon for the gate contact are specified. In each section, two sequences are given, Sequence 1 and Sequence 6. Sequence 1 runs an initialization program to start up (Sequence 0), sets up hydrogen flow and stablizies the chamber pressure, calls Sequence 6, which contains the actual growth recipe, and, when Seuqnce 6 has finished, calls a shut down program (Sequence 7).

D.1 RTCVD growth sequence for epitaxial silicon regrowth, #3844

D.1.1 Sequence 1, #3844

```
Time  0
   // Sequence_1
   EndSeq SEQUENCE_0
   // pre-flow H2
   STATUS_MESSAGE = "Pre-flow H2"
   DO15_VACUUM = 1
   DO01_H2_SEL = 1
   AO00_MAIN = 0.1
   AO11_LP_SELECT = 1
   WaitFor AI28_PRES_LOW > 0.5,  0.300
   AO00_MAIN = 0.617
   AO11_LP_SELECT = 1
   AO08_PRESS = 1.0
   STATUS_MESSAGE = "Pressure Stablizing"
   WaitFor AI28_PRES_LOW > 9.5,  0.300
   // call main sequence
   SP2 = 0
   BeginSeq Sequence_6
   WaitFor SP2 > 0.5,  0.300
   EndSeq Sequence_6
   BeginSeq SEQUENCE_7
```

D.1.2 Sequence 6, #3844

```
Time  0
   // Sequence_6
   // SAMPLE #3844
   LAMPPOWER_MAX = 0.26
   LAMPPOWER_RATE = 0.40
   T_CA00 = 0.6
   T_CA01 = 2.13
   T_CA03 = 2
   T_CA04 = 2
   // cold transmission acquisition
   STATUS_MESSAGE = "Press SOFT_GO for Cold Values"
   WaitFor SOFT_GO > 0.5,  0.300
   SP3 = 1
   Wait 1
   SP3 = 0
   // Start Gas Flows (H2 to vent)
   AO06_DCS = 0.534
   AO00_MAIN = 0.617
   // Ramp up to 10T
   AO08_PRESS = 1.0
   STATUS_MESSAGE = "Ramping up pressure to 10 Torr"
   WaitFor AI28_PRES_LOW>9.50,  0.300
   DO07_DCS_SEL = 1
   // Ramp up to 16% lamp power
   STATUS_MESSAGE = "At 10T, RAMPING SP7 UP to 0.16"
   SP1 = 0
   RAMP_GOAL[0] = 0.16
   RAMP_RATE[0] = 0.4
   BeginSeq RAMP_SP7
   WaitFor SP1  > 0.5,  0.300
   Var.wait_time = 30
   Wait 30
   // Ramp up to 19% lamp power
   STATUS_MESSAGE = "At 10T, RAMPING SP7 UP to 0.19"
   SP1 = 0
   RAMP_GOAL[0] = 0.19
   RAMP_RATE[0] = 0.4
   BeginSeq RAMP_SP7
   WaitFor SP1  > 0.5,  0.300
   Var.wait_time = 60
   Wait 60
   // Ramp up to 25% lamp power
   STATUS_MESSAGE = "RAMPING SP7 UP to 0.25"
   SP1 = 0
   RAMP_GOAL[0] = 0.25
   RAMP_RATE[0] = 0.4
   BeginSeq RAMP_SP7
   WaitFor SP1  > 0.5,  0.300
   STATUS_MESSAGE = "2 min at 25% (800C)"
   Var.wait_time = 120
   Wait 120
   STATUS_MESSAGE = "Press SOFT_GO if done at 800C"
   WaitFor SOFT_GO > 0.5,  0.300
   // Set 6 Torr
   AO08_PRESS = 0.6
```

```
   STATUS_MESSAGE = "Ramping down pressure to 6 Torr"
   WaitFor AI28_PRES_LOW<6.50,  0.300
   // Ramp down to 19% lamp power
   STATUS_MESSAGE = "RAMPING SP7 DOWN to 0.19, change 1.55um lower to
0.1*upper"
   SP1 = 0
   RAMP_GOAL[0] = 0.19
   RAMP_RATE[0] = -0.4
   BeginSeq RAMP_SP7
   WaitFor SP1  > 0.5,  0.300
   T_CA04 = 1
   STATUS_MESSAGE = "Press SOFT_GO to start auto control at 700C (when
Ofac1.5 and LIA are OK)"
   WaitFor SOFT_GO > 0.5,  0.300
   // ************* SP5 for 700C ***************
   SP5 = 3.487
   SP4 = 1
   Var.wait_time = 30
   Wait 30
   STATUS_MESSAGE = "Press SOFT_GO when 700C to start epi growth"
   WaitFor SOFT_GO > 0.5,  0.300
   DO13_DCSandSi2H6_INJ = 1
   STATUS_MESSAGE = "Growing epi-Si layer 21 min"
   Var.wait_time = 1260
   Wait 1260
   STATUS_MESSAGE = "Press SOFT_GO to end epi growth"
   WaitFor SOFT_GO > 0.5,  0.300
   DO13_DCSandSi2H6_INJ = 0
   // 6T 1 slpm H2
   AO00_MAIN = 0.2
   // Ramp lamps down
   SP4 = 0
   STATUS_MESSAGE = "Ramp lamps down"
   SP1 = 0
   RAMP_GOAL[0] = 0.00
   RAMP_RATE[0] = -0.4
   BeginSeq RAMP_SP7
   WaitFor SP1  > 0.5,  0.300
   DO07_DCS_SEL = 0
   // End
   STATUS_MESSAGE = "Done with Growth Sequence"
   SP2 = 1
```

D.2 RTCVD growth sequence for p+ poly silicon, #3849

D.2.1 Sequence 1, #3849

```
Time  0
   // Sequence_1
   EndSeq SEQUENCE_0
   // pre-flow H2
   STATUS_MESSAGE = "Pre-flow H2"
   DO15_VACUUM = 1
   DO01_H2_SEL = 1
```

```
AO00_MAIN = 0.1
AO11_LP_SELECT = 1
WaitFor AI28_PRES_LOW > 0.5,  0.300
AO00_MAIN = 0.618
AO11_LP_SELECT = 1
AO08_PRESS = 0.6
STATUS_MESSAGE = "Pressure Stablizing"
WaitFor AI28_PRES_LOW > 5.5,  0.300
// call for cleaning squence
SP2 = 0
BeginSeq Sequence_6
WaitFor SP2 > 0.5,  0.300
EndSeq Sequence_6
BeginSeq SEQUENCE_7
```

D.2.2 Sequence 6, #3849

```
Time  0
   // Sequence_6
   // SAMPLE #3849 p+ poly Si on 19V samples NP1,2,3,4
   LAMPPOWER_RATE = 0.40
   T_CA00 = 0.55
   T_CA01 = 2.20
   T_CA03 = 1
   T_CA04 = 1
   // pre-flow 3 slpm H2
   STATUS_MESSAGE = "Pre-flow H2"
   DO15_VACUUM = 1
   DO01_H2_SEL = 1
   AO00_MAIN = 0.618
   AO11_LP_SELECT = 1
   AO06_DCS = 0.534
   WaitFor AI28_PRES_LOW > 0.5,  0.300
   AO08_PRESS = 0.6
   STATUS_MESSAGE = "Pressure Stablizing"
   WaitFor AI28_PRES_LOW > 5.5,  0.300
   // cold transmission acquisition
   STATUS_MESSAGE = "Start Logfile, Press SOFT_GO for Cold Values"
   WaitFor SOFT_GO > 0.5,  0.300
   // H2 3 slpm
   AO00_MAIN = 0.618
   // B2H6 high flow on to vent
   AO03_B2H6_HIGH = 0.5
   DO04_B2H6_SEL = 1
   // SiH4 on to vent
   AO01_SiH4 = 0.16
   DO02_SiH4_SEL = 1
   Wait 5
   SP3 = 1
   Wait 1
   SP3 = 0
   // ramp up
   STATUS_MESSAGE = "Ramp Up Lamp"
   SP1 = 0
   RAMP_GOAL = 0.18
   RAMP_RATE = 0.4
   BeginSeq RAMP_SP7
```

```
   WaitFor SP1 > 0.5,  0.300
   STATUS_MESSAGE = "2 minutes at 18% lamp power"
   Var.wait_time = 120
   Wait 120
   // ************** SP5 for 700C ***************
   SP5 = 3.557
   SP4 = 1
   STATUS_MESSAGE = "Wait 1 minute to stabilize at 700C"
   Var.wait_time = 60
   Wait 60
   STATUS_MESSAGE = "Press SOFT_GO when 700C achieved for poly-Si
growth"
   WaitFor SOFT_GO > 0.5,  0.300
   // SiH4 and B2H6 inject on
   STATUS_MESSAGE = "SiH4 and B2H6 Inject On"
   DO09_SiH4_INJ = 1
   DO11_B2H6_INJ = 1
   STATUS_MESSAGE = "Growing p+ poly-Si for 25min"
   Var.wait_time = 1500
   Wait 1500
   // SiH4 and B2H6 inject off
   STATUS_MESSAGE = "SiH4 and B2H6 Inject and Select Off"
   DO11_B2H6_INJ = 0
   DO04_B2H6_SEL = 0
   DO09_SiH4_INJ = 0
   DO02_SiH4_SEL = 0
   // ramp down
   SP4 = 0
   STATUS_MESSAGE = "Ramp Down Lamp"
   SP1 = 0
   RAMP_GOAL = 0
   RAMP_RATE = -0.4
   BeginSeq RAMP_SP7
   WaitFor SP1 > 0.5,  0.300
   STATUS_MESSAGE = "Done with poly-Si growth sequence"
   SP2 = 1
```

D.3 RTCVD growth sequence for n+ poly silicon, #3854

D.3.1 Sequence 1, #3854

```
Time  0
   // Sequence_1
   EndSeq SEQUENCE_0
   // pre-flow H2
   STATUS_MESSAGE = "Pre-flow H2"
   DO15_VACUUM = 1
   DO01_H2_SEL = 1
   AO00_MAIN = 0.1
   AO11_LP_SELECT = 1
   WaitFor AI28_PRES_LOW > 0.5,  0.300
   AO00_MAIN = 0.618
   AO11_LP_SELECT = 1
   AO08_PRESS = 0.6
```

```
    STATUS_MESSAGE = "Pressure Stablizing"
    WaitFor AI28_PRES_LOW > 5.5,  0.300
    // call for cleaning squence
    SP2 = 0
    BeginSeq Sequence_6
    WaitFor SP2 > 0.5,  0.300
    EndSeq Sequence_6
    BeginSeq SEQUENCE_7
```

D.3.2 Sequence 6, #3854

```
Time  0
    // Sequence_6
    // SAMPLE #3854 n+ poly Si on 19V samples NN1,2,3,4
    LAMPPOWER_RATE = 0.40
    T_CA00 = 0.55
    T_CA01 = 2.2
    T_CA03 = 1
    T_CA04 = 1
    // pre-flow 3 slpm H2
    STATUS_MESSAGE = "Pre-flow H2"
    DO15_VACUUM = 1
    DO01_H2_SEL = 1
    AO00_MAIN = 0.618
    AO11_LP_SELECT = 1
    AO06_DCS = 0.534
    WaitFor AI28_PRES_LOW > 0.5,  0.300
    AO08_PRESS = 0.6
    STATUS_MESSAGE = "Pressure Stablizing"
    WaitFor AI28_PRES_LOW > 5.5,  0.300
    // cold transmission acquisition
    STATUS_MESSAGE = "Start logfile, Press SOFT_GO for Cold Values"
    WaitFor SOFT_GO > 0.5,  0.300
    // H2 3 slpm
    AO00_MAIN = 0.618
    // PH3 high flow on to vent
    AO04_PH3_HIGH = 0.9
    DO05_PH3_SEL = 1
    // SiH4 on to vent
    AO01_SiH4 = 0.16
    DO02_SiH4_SEL = 1
    Wait 5
    SP3 = 1
    Wait 1
    SP3 = 0
    // ramp up
    STATUS_MESSAGE = "Ramp Up Lamp"
    SP1 = 0
    RAMP_GOAL = 0.18
    RAMP_RATE = 0.4
    BeginSeq RAMP_SP7
    WaitFor SP1 > 0.5,  0.300
    STATUS_MESSAGE = "2 minutes at 18% lamp power"
    Var.wait_time=120
    Wait 120
    // ************* SP5 for 700C ***************
    SP5 = 3.557
```

```
   SP4 = 1
   STATUS_MESSAGE = "Wait 1 minute to stabilize at 700C"
   Var.wait_time = 60
   Wait 60
   STATUS_MESSAGE = "Press SOFT_GO when 700C achieved for poly-Si
growth"
   WaitFor SOFT_GO > 0.5,  0.300
   // SiH4 and B2H6 inject on
   STATUS_MESSAGE = "SiH4 and PH3 Inject On"
   DO09_SiH4_INJ = 1
   DO12_PH3_INJ = 1
   STATUS_MESSAGE = "Growing n+ poly-Si for 44min"
   Var.wait_time = 2640
   Wait 2640
   // SiH4 and PH3 inject off
   STATUS_MESSAGE = "SiH4 and PH3 Inject and Select Off"
   DO12_PH3_INJ = 0
   DO05_PH3_SEL = 0
   DO09_SiH4_INJ = 0
   DO02_SiH4_SEL = 0
   // ramp down
   SP4 = 0
   STATUS_MESSAGE = "Ramp Down Lamp"
   SP1 = 0
   RAMP_GOAL = 0
   RAMP_RATE = -0.4
   BeginSeq RAMP_SP7
   WaitFor SP1 > 0.5,  0.300
   STATUS_MESSAGE = "Done with poly-Si growth sequence"
   SP2 = 1
```

Appendix E

Optimizing RTCVD Temperature Control

This appendix describes the computer-based temperature control system of the Sturm Group rapid-thermal chemical vapor deposition (RTCVD) tool. Specifically, it presents methods for optimizing temperature control for growth on thick wafers and/or at low temperatures. The previous Control-EG computer software was replaced in August 2003 by DAQ Factory, running in Windows XP. The full details of the DAQFactory software configuration, its operation and use, are detailed in extensive documentation written by Michael Pasqual, who was the primary architect of the change during his summer 2003 employment in the group. The computer controls chamber pressure, gas flow, and wafer temperature via the lamp output. Here, we focus solely on the temperature control sub-system, particularly on the computer control variables used to effect automatic temperature control via DAQFactory feedback loops.

E.1 Temperature Control System Design and Principles

The temperature control system used in the Sturm Group RTCVD equipment is schematically drawn in Fig. E.1. A silicon wafer substrate for deposition is loaded inside a quartz tube. The wafer is heated by tungsten lamps under the tube, and the radiative heat is reflected back by a gold-coated reflector assembly surrounding the tube. Two lasers, of wavelengths 1.30 and 1.55 μm, are modulated using square waves of different frequencies, f_1, and f_2 (about 10.3 and 11.0 kHz). The two lasers are coupled into a single optical fiber, which is used to direct the light onto the wafer surface by a lens outside the reflector assembly. An InGaAs photodetector placed opposite the lens, under the reflector assembly, is used to collect the laser light transmitted through the wafer. The detector output is broken into the two frequency components using lock-in amplifiers referencing the original square wave signals. Two lock-in amplifiers are used for each wavelength to

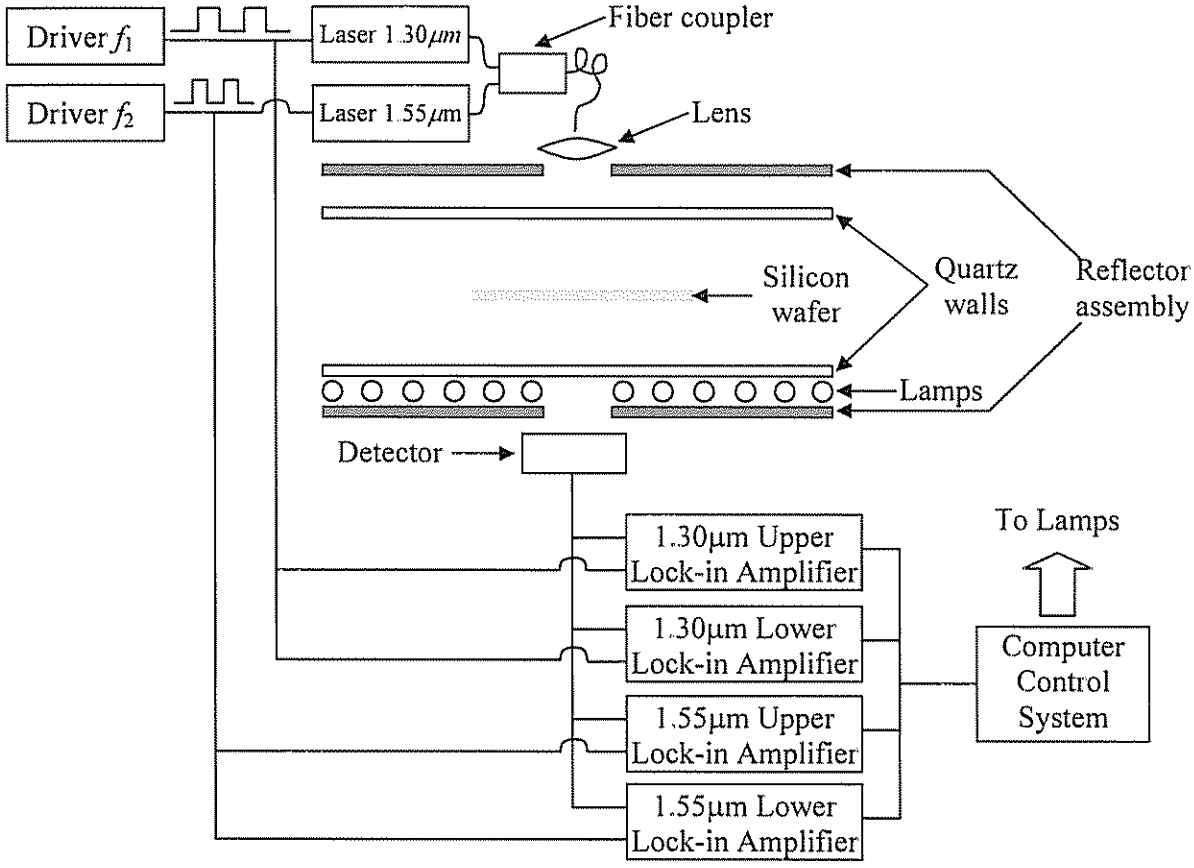


Figure E.1: Schematic cross-section of the RTCVD growth chamber, with the components for temperature control specified.

enable precise measurement of transmission across several orders of magnitude. One lock-in amplifier is tuned to the upper voltage range, and the other to a range one or two decades lower magnitude. The lock-in amplifier outputs are sent to the computer control system, which uses PID control loops to set the lamp power.

The temperature control system is based on the measurement of 1.30- and 1.55-μm laser transmission through the wafer. The ratio of the "hot" transmission (at temperatures of 400-800°C) to the "cold" transmission (at room temperature) of a silicon wafer varies predictably over several orders of magnitude. This ratio is referred to as the normalized transmission, NT_λ, and is plotted in Fig. E.2 for 500- and 600-μm thick silicon wafers. At room temperature, the wafers absorb very little of the laser light at these wavelengths, and the normalized transmission is by definition equal to one. As the temperature increases, bandgap absorption and free-carrier absorption increase and the normalized transmission decreases. In the temperature range of interest, the absorption of 1.30-μm light is dominated by bandgap absorption [174]. For a 500-μm wafer at 650°C the normalized transmission is very small, ~10^{-3}; this is the maximum temperature for which the 1.3-μm light is useful. Absorption of 1.55-μm light, in contrast, is dominated by free carrier absorption [174]. A significant fraction of 1.55-μm light is transmitted at temperatures of up to ~800°C for a 500-μm wafer, as shown in Fig. E.2. Thus, the 1.30-μm signal is typically used to measure lower temperatures (< 650°C), while the 1.55-μm signal is used to measure higher temperatures (650-800°C).

To first order, the only variable that controls the normalized transmission of a silicon wafer, besides temperature, is the wafer thickness. Comparing the normalized transmission curves for 500-μm and 600-μm wafers in Fig. E.2, it is clear that thicker wafers absorb more light. Based on curves like those shown in Fig. E.2, if the wafer thickness is known, the temperature can be determined (and thus controlled) by measuring the hot/cold transmission ratio. In Table E.1, the normalized transmission of silicon wafers of various thicknesses are tabulated for λ=1.30 μm and 1.55 μm. The fundamental absorption processes and methods used to obtain the normalized transmission curves are described in Ref. [172-174].

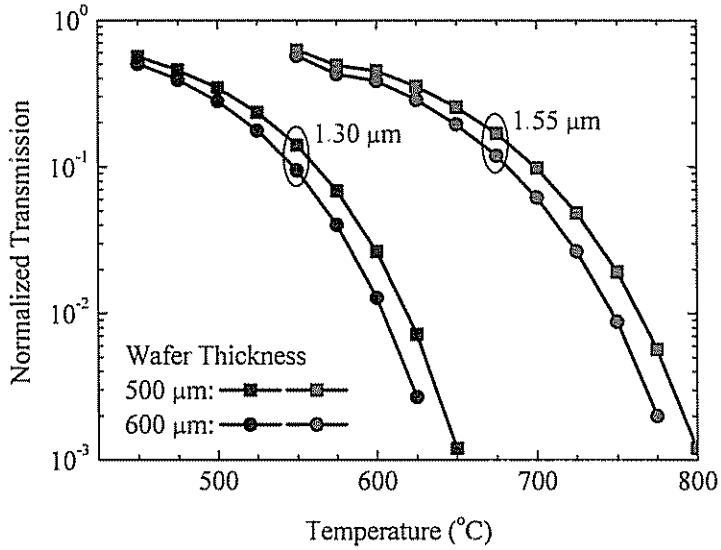


Figure E.2: Normalized transmission of 1.30- and 1.55-μm light through 500- and 600-μm wafers. The 1.55-μm light transmits at higher temperatures (~700°C) at which the 1.30-μm light is fully absorbed. Thicker wafers absorb more light than thinner wafers. After Ref. [172-174].

$\lambda = 1.30$ μm Normalized Optical Transmission

Temp (° C)	Wafer Thickness (μm)																
	440	450	460	470	480	490	500	510	520	530	540	550	560	570	580	590	600
450	0.6040	0.5970	0.5900	0.5840	0.5770	0.5700	0.5640	0.5570	0.5510	0.5450	0.5390	0.5320	0.5260	0.5200	0.5150	0.5090	0.5030
475	0.5030	0.4950	0.4880	0.4800	0.4730	0.4650	0.4580	0.4510	0.4440	0.4370	0.4300	0.4240	0.4170	0.4100	0.4040	0.3980	0.3920
500	0.3930	0.3850	0.3770	0.3690	0.3610	0.3530	0.3460	0.3390	0.3320	0.3250	0.3110	0.3100	0.3050	0.2980	0.2920	0.2860	0.2800
525	0.2810	0.2730	0.2650	0.2580	0.2500	0.2430	0.2360	0.2300	0.2230	0.2170	0.2100	0.2050	0.1980	0.1930	0.1876	0.1823	0.1770
550	0.1780	0.1710	0.1650	0.1580	0.1520	0.1460	0.1410	0.1350	0.1300	0.1250	0.1200	0.1160	0.1110	0.1070	0.1028	0.0988	0.0950
575	0.0950	0.0900	0.0850	0.0810	0.0770	0.0730	0.0690	0.0653	0.0620	0.0587	0.0556	0.0527	0.0500	0.0474	0.0449	0.0426	0.0404
600	0.0410	0.0380	0.0350	0.0330	0.0307	0.0285	0.0265	0.0247	0.0230	0.0213	0.0198	0.0185	0.0172	0.0160	0.0148	0.0138	0.0128
625	0.0130	0.0118	0.0107	0.0097	0.0088	0.0079	0.0072	0.0065	0.0058	0.0054	0.0049	0.0044	0.0040	0.0036	0.0033	0.0030	0.0027
650	0.0027	0.0024	0.0021	0.0018	0.0016	0.0014	0.0012	0.0011	~0	~0	~0	~0	~0	~0	~0	~0	~0

$\lambda = 1.55$ μm Normalized Optical Transmission

Temp (° C)	Wafer Thickness (μm)																
	440	450	460	470	480	490	500	510	520	530	540	550	560	570	580	590	600
550	0.6630	0.6570	0.6510	0.6450	0.6390	0.6330	0.6270	0.6210	0.6150	0.6090	0.6040	0.5980	0.5930	0.5870	0.5820	0.5760	0.5710
575	0.5370	0.5290	0.5220	0.5150	0.5070	0.5000	0.4930	0.4860	0.4800	0.4730	0.4660	0.4600	0.4530	0.4470	0.4410	0.4340	0.4280
600	0.4960	0.4880	0.4800	0.4730	0.4650	0.4580	0.4510	0.4440	0.4370	0.4300	0.4230	0.4160	0.4100	0.4030	0.3970	0.3910	0.3840
625	0.4000	0.3920	0.3840	0.3760	0.3680	0.3600	0.3530	0.3460	0.3390	0.3320	0.3250	0.3180	0.3120	0.3050	0.2990	0.2930	0.2870
650	0.3020	0.2940	0.2860	0.2780	0.2710	0.2640	0.2560	0.2500	0.2430	0.2360	0.2300	0.2240	0.2180	0.2120	0.2060	0.2000	0.1950
675	0.2100	0.2030	0.1960	0.1890	0.1820	0.1760	0.1697	0.1638	0.1580	0.1530	0.1470	0.1420	0.1370	0.1320	0.1280	0.1230	0.1190
700	0.1300	0.1240	0.1185	0.1130	0.1080	0.1031	0.0984	0.0940	0.0897	0.0856	0.0818	0.0781	0.0750	0.0710	0.0680	0.0648	0.0619
725	0.0700	0.0658	0.0620	0.0584	0.0550	0.0517	0.0487	0.0458	0.0432	0.0406	0.0383	0.0360	0.0339	0.0320	0.0300	0.0283	0.0266
750	0.0310	0.0286	0.0265	0.0245	0.0226	0.0210	0.0193	0.0178	0.0165	0.0152	0.0141	0.0130	0.0120	0.0111	0.0103	0.0095	0.0088
775	0.0106	0.0096	0.0086	0.0078	0.0070	0.0063	0.0057	0.0051	0.0046	0.0042	0.0038	0.0034	0.0031	0.0028	0.0025	0.0023	0.0020
800	0.0027	0.0023	0.0020	0.0018	0.0016	0.0014	0.0012	0.0010	~0	~0	~0	~0	~0	~0	~0	~0	~0

Table E.1: Normalized transmission vs wafer thickness and temperature for λ=1.30 and 1.55 μm. From Sturm group RTCVD manual.

E.2 Computerized Temperature Control

The computerized control of the temperature consists of four basic steps in a continuously running feedback loop: (1) Input the normalized transmission values given by the lock-in amplifiers as described above; (2) Determine whether the 1.30-μm or 1.55-μm transmission should be observed; (3) Use a PID loop to match the observed normalized transmission to the desired value specified by the user in the run sequence; (4) From the PID loop, output the new lamp power value needed to bring the observed and specified normalized transmissions into agreement. As the lamp power changes, the wafer temperature changes, modifying the normalized transmission under observation, and the cycle continues.

In this section, we will focus on the second and third steps. The principle is very simple: the program reads in the normalized transmission values and determines which one is likely to be in the correct range for temperature control. If the 1.55-μm *NT* is below a certain value, it is used, whereas if the 1.30-μm *NT* is above a certain value, it is used. A problem occurs because these requirements are not mutually exclusive and thus it is possible that for certain wafer thicknesses and certain temperature ranges, both laser signals or neither signal will be used in the temperature control algorithm, which can lead to poor temperature control. A method to reduce this possibility will be described below.

At the beginning of the sequence, the user generally includes instructions for the computer to record the "cold" transmission values, T_{cold}, in the variables *CA09* and *CA10*:

$$CA09 = Cold1.3 = \log_{10} T_{1\ 30\mu m,\ cold} \tag{E.1a}$$

$$CA10 = Cold1.5 = \log_{10} T_{1\ 55\mu m,\ cold} \tag{E.1b}$$

As the temperature increases, the computer obtains the "hot" transmission at 1.30 and 1.55 μm from the lock-in amplifiers, and must choose between them. It makes this choice through the variables *CA01* = *Lim1.3* and *CA00* = *Lim1.5*, which have typical values of 2.5 and 0.7, respectively. If the base-10 logarithm of the 1.55-μm normalized transmission, *NT*, is less than –Lim1.5, then the log of the 1.55-μm *NT* is added to the total signal, otherwise the Lim1.5 value itself is added:

$$\text{If } \log_{10}T_{1\ 55\mu m,\ hot} - \log_{10}T_{1\ 55\mu m,\ cold} = \log_{10}NT_{1\ 55\mu m} < -Lim1.5$$

$$\text{then } CA16 = Tmp1.5L = -\log_{10}NT_{1\ 55\mu m}$$

$$\text{else } CA16 = Tmp1.5L = Lim1.5 \qquad \text{(E.2)}$$

Simultaneously, if the $\log_{10}$ of the 1.30-μm normalized transmission is greater than –Lim1.3, then the log of the 1.30-μm *NT* is added to the total signal, otherwise the Lim1.3 value itself is added.

$$\text{If } \log_{10}T_{1\ 30\mu m,\ hot} - \log_{10}T_{1\ 30\mu m,\ cold} = \log_{10}NT_{1\ 30\mu m} > -Lim1.3$$

$$\text{then } CA15 = Tmp1.3L = -\log_{10}NT_{1\ 30\mu m}$$

$$\text{else } CA15 = Tmp1.3L = Lim1.3 \qquad \text{(E.3)}$$

The total control signal is then the sum of *CA15* and *CA16* (*Tmp1.5L* + *Tmp1.3L*). This control signal is compared to the PID setpoint value, SP5, specified by the user. Before the program starts, the user has calculated and set SP5:

$$SP5 = |\log_{10}NT_{\text{desired }\lambda,\text{ wafer thickness}} - Lim_{\text{opposite }\lambda}| \qquad \text{(E.4)}$$

The PID loop modifies the lamp power until SP5 and the sum of *CA15* and *CA16* (*Tmp1.5L* + *Tmp1.3L*) are equal.

To illustrate this procedure, take the typical example of a 500-μm wafer heated to 700°C. From Fig. E.2, it is clear that the 1.55-μm laser should be used to control at this temperature. Therefore, using the normalized transmission value from Table E.1, $NT_{1\ 55\mu m,\ 500\mu m} = 0.0984$, and $Lim1.3 = 2.5$, $Lim1.5 = 0.7$, we can calculate from Eqn. E.4 the SP5 value to be specified by the user: SP5=3.51. Now, we look at the computer's temperature control. When the wafer is at 700°C, according to Eqns. E.2 and E.3, $Tmp1.5L = -\log_{10}NT_{1\ 55\mu m} = +1.01$ and $Tmp1.3L = Lim1.3 = 2.5$, so as expected $Tmp1.5L + Tmp1.5L = SP5 = 3.51$. At this temperature, only the 1.55-μm transmission is being used in the calculation because $\log_{10}NT_{1\ 55\mu m} = -1.01 < -Lim1.5 = -0.7$. Conversely, at 625°C, assuming the 1.30-μm laser will be used, the SP5 value is 2.84. At 625°C, $\log_{10}NT_{1\ 30\mu m} = -2.14 > -Lim1.3 = -2.5$. Therefore the 1.30-μm transmission will indeed be used to control the tempereature, and again $Tmp1.5L + Tmp1.5L = SP5$. Both of these cases illustrate clear-cut temperature control by use of a single laser transmission value.

However, consider the situation of controlling the temperature of this same wafer at 650°C. From Table E.1 and Fig. E.2, it seems that either the 1.30-μm or 1.55-μm

transmission can be used. Let us choose the 1.55-μm transmission. Thus SP5 = 3.09. According to Eqns. E.2 and E.3, when the wafer is at 650°C, *Tmp1.5L* = *Lim1.5* = 0.7, and *Tmp1.3L* = *Lim1.3* = 2.5, and their sum is *Tmp1.5L* + *Tmp1.5L* = 3.2 ≠ SP5. Neither laser transmission value is included in the sum, *i.e.*, the laser output has been effectively disconnected from the PID feedback loop. Thus, it is impossible for the system to accurately control at this temperature. This situation is illustrated graphically in Fig. E.3 where we expand the plot of Fig. E.2 around the temperature range of interest. Dashed lines indicate $NT = 10^{-Lim}$ for the standard values (*Lim1.3* = 2.5 and *Lim1.5* = 0.7). There is clearly a large window, from 636°C, where the 1.30-μm control stops, to 665°C, where the 1.55-μm control begins, where neither laser signal is being used to control the temperature. Between these two points, the temperature control will be poor. By changing the values of *Lim1.3* and *Lim1.5* to 2.65 and 0.55, respectively, as indicated by the dotted lines in Fig. E.3, this window can be narrowed to ~3°C around 640°C. Now, good temperature control is achieved through the entire region.

Clearly, it is important to consider the choice of *Lim1.3* and *Lim1.5* for a specific wafer thickness and desired deposition temperature(s), and to ensure that the transition between the two wavelengths is smooth and occurs far from the deposition temperatures. The previously used values of 2.5 and 0.7 work well for the typical case of a 500-μm wafer at 700°C and 625°C, as shown above, but for thicker wafers and/or temperatures between these values, *Lim1.3* and *Lim1.5* should be chosen to minimize the window between 1.3- and 1.55-μm laser transmission control, without allowing the two regions to overlap. In the new program, an output has been added which specifies the lock-in amplifier signal being used (*e.g.*, "Upper 1.30μm", "Lower 1.55μm", "Both", "Neither"). Users should observe and log this value to make sure it agrees with their expectation.

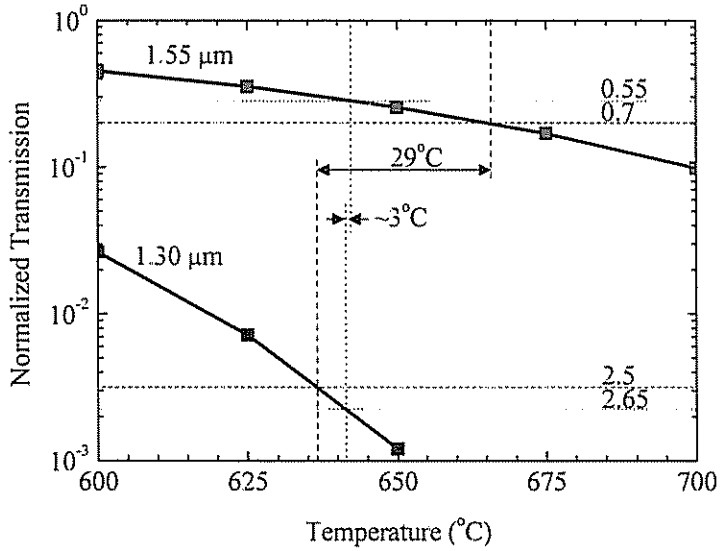


Figure E.3: Normalized transmission of 1.30- and 1.55-μm light through a 500-μm wafer. The dashed lines indicate the standard *Lim1.3* and *Lim1.5* values of 2.5 and 0.7, respectively, and their intersections with the normalized transmission curve. Using these *Lim* values, there is a 29°C window over which neither laser will be used to control the wafer temperature. By changing *Lim 1.3* and *Lim 1.5* to 2.65 and 0.55, respectively, that window is closed to ~3°C, assuring much better control, as indicated by the dotted lines.

E.3 Thick wafers

The chart of Table E.1 shows normalized transmission for wafers up to 600 μm thick. This was perfectly sufficient at the time this chart was made (early 1990's), when 100-mm wafers, with thicknesses around 500 μm were dominant. Today however, many samples, including our bonding samples, are fabricated on 150-mm (or larger) wafers which are usually thicker, in our case around 670 μm. Thus, it was imperative for this work that the normalized transmission chart be extended to greater wafer thicknesses to control the temperature during strained-silicon regrowth and poly-silicon gate deposition by RTCVD.

As has been observed previously [172,174], the normalized transmission of a silicon wafer at these infrared frequencies is proportional to $e^{-\alpha d}$, where α is the absorption coefficient and d is the wafer thickness. The absorption coefficients are calculated from the tabulated NT values, and are plotted vs temperature in Fig. E.4. From these values, the absorption coefficients and existing data points can be used to calculate the normalized transmission for any wafer thickness, according to:

$$NT(d) = NT(d_o) \cdot e^{-\alpha(d-d_o)} \tag{E.5}$$

From example, for a 670-μm wafer at 700°C, $\alpha = +46.4$ cm^{-1}, and using $d_0 = 600$ μm, the normalized transmission for a 670-μm wafer is calculated to be 0.0448.

Of course, whenever a new wafer thickness is used, the *Lim1.3* and *Lim1.5* values should be checked to make sure the temperature control will cleanly transition between the 1.30- and 1.55-μm laser signals. For a 670-μm wafer, *Lim1.3* and *Lim1.5* values of 2.65 and 0.55 will result in a small overlapping window where the system will try to use both laser transmission values from 615 to 618°C. This is a rather trivial overlap, but one wants to eliminate it, values of *Lim1.3* = 2.5 and *Lim1.5* =0.55 can be used. This results in a very small gap from 612 to 615 °C, between the use of the 1.30- and 1.55-μm laser transmissions to control temperature.

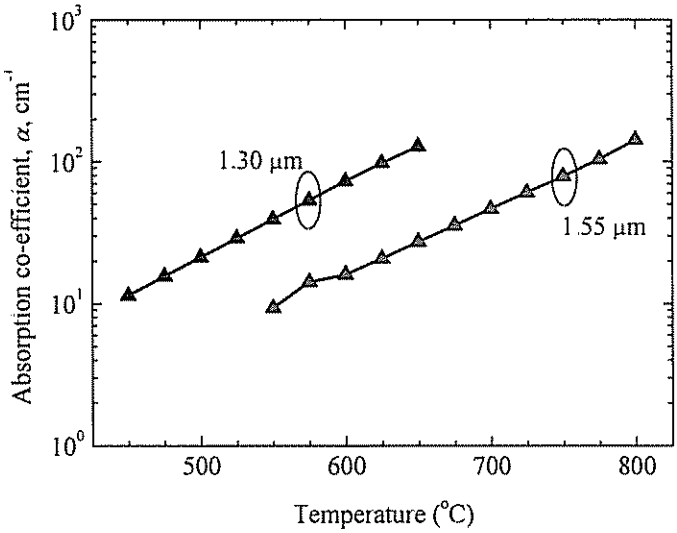


Figure E.4: Absorption coefficients (cm^{-1}) vs temperature for λ=1.30 and 1.55 μm. The solid symbols and solid lines indicate values from the existing tables, after Ref. [172,174].

E.4 Fluctuation of Cold Values

We have already seen how the normalized transmission increases and reaches a plateau at unity as the deposition temperature decreases. This implies that the error in controlling the temperature is also much larger at low temperatures. For example, if the 1.30-μm normalized transmission through a 500-μm wafer is randomly varying by 10%, at 625°C this will only result in a ±1.6°C variation in the perceived temperature, a negligible amount. However if the same wafer is being controlled using the 1.3-μm laser at 500°C or even 450°C, 10% variation in normalized transmission causes the perceived temperature to change ±7.7°C or ±13°C, respectively. Clearly, to control growth at low temperatures, it is critical to control random fluctuations in the laser transmissions.

During the course of other work with the RTCVD system, it was discovered that the "cold" laser transmission values show significant fluctuations when the tool is shut down and no intended perturbations are present. A typical "cold" value measurement is plotted in Fig. E.5. The 1.3-μm transmission fluctuates by ±11.3% while the 1.55-μm transmission fluctuates by ±5.4%, with a regular period of 7.0 min. This phenomenon was consistently observed over several weeks. Eventually the cause was isolated to cyclical variations in the room temperature caused by the building heating and cooling system. In Fig. E.6, the room temperature is plotted vs time alongside the laser transmissions, and it is clear that the two cycles are directly related. The lasers have individual thermistors and Peltier coolers to maintain each laser at a constant temperature. The thermistor and cooling voltages likewise are simultaneously fluctuating in time, as shown in Fig. E.6, as would be expected if the room temperature was changing. The room temperature has such a strong effect because a ventilation outlet is unfortunately located immediately above the lasers, the laser cooler circuitry, and the fiber coupler. Since the Peltier coolers seem to be responding appropriately to the room temperature changes, the primary source of the observed laser output fluctuations is probably temperature-dependent attenuation in the fiber coupler and its connections.

When the ventilation outlet was redirected away from the optical components, and the heating and ventilation system was fine-tuned to minimize temperature variations, the

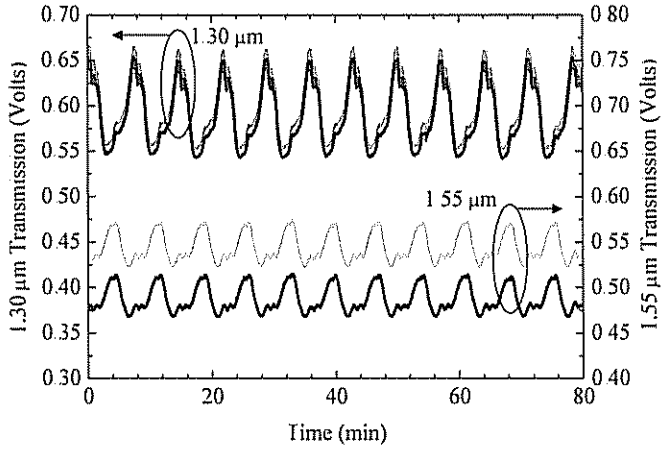


Figure E.5: Measured fluctuations in the "cold" 1.30- and 1.55-μm laser transmission with no intended perturbations to the system. (The RTCVD tool is turned off.) The fluctuations are clearly periodic, with a period of 7.0 min.

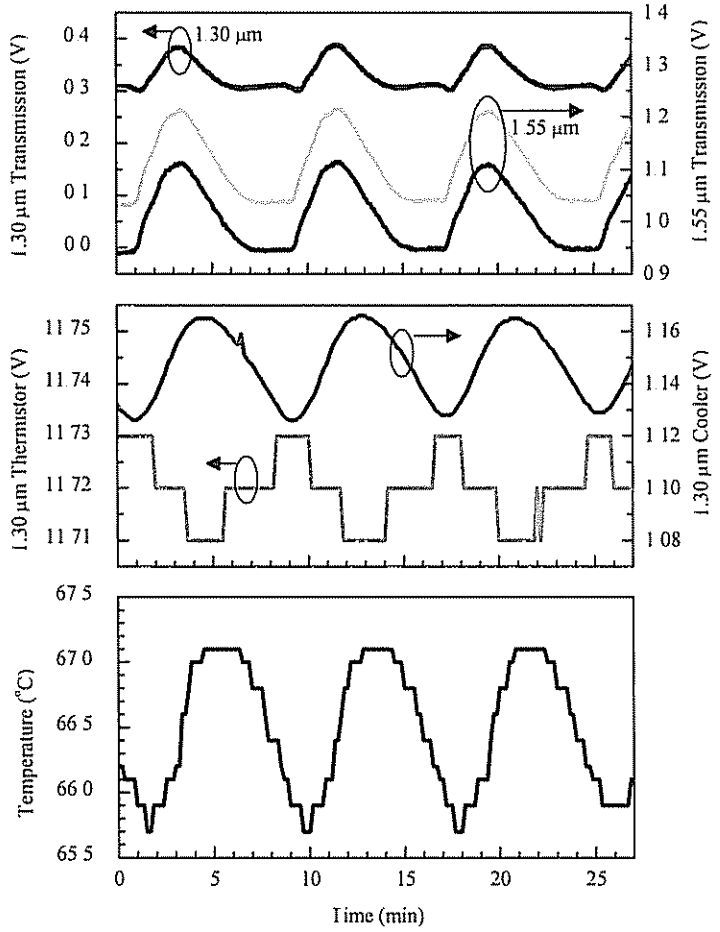


Figure E.6: Measured fluctuations in the laser transmission values, the 1.30-μm thermistor and Peltier cooler voltage values, and the room temperature, before any improvements were made.

observed fluctuations in the 1.30- and 1.55-μm laser transmission values were significantly reduced. Typical variations after these improvements are shown in Fig. E.7, where the period of fluctuations is relatively unchanged at 7.6 min, but the percentage variation in the transmission values have now been reduced to ±1.4% and ±0.5% for the 1.30- and 1.55-μm lasers, respectively.

E.5 Lock-in Amplifier Issues

Finally, we noted in Sec. E.2 that it is important to correctly choose the values of *Lim1.3* and *Lim1.5* to ensure that there is a smooth transition between temperature control with the 1.3- and 1.55-μm lasers. It is also important to choose correctly the lock-in amplifier settings to ensure the maximum resolution of the measured transmission, and thereby minimize the normalized transmission error and thus temperature control error, as described in the previous section. There are three areas where attention needs to be paid. First, the conversion factors and offsets used in the software to correct the lock-in amplifier values, *AI32*, *AI33*, *AI34* and *AI35*, should be checked before each run. The conversion equations for the lock-in amplifiers allow the user to correct for lock-in amplifier anomalies which may occur such as DC offsets or discrepancies between lock-in amplifier values (*e.g.*, as seen in Fig. E.5 for the 1.5-μm upper and lower lock-in amplifiers.) Second, the number of decades between the upper and lower lock-in amplifier ranges, as well as their absolute voltage ranges, should be chosen appropriately and the number of decades coded in the control software using the variables *Ofac1.3* and *Ofac1.5*. For maximum resolution the voltage ranges should be as low as possible for the loaded wafer, while allowing for sufficient increase in the transmission during typical cleaning and silicon buffer layer growth, due to the smoothing of the wafer surface. Alternately, the voltage ranges can be chosen (or double-checked) after the buffer layer growth, just before the cold transmission values are taken. Finally, the voltage ranges at which the software switches between the upper and lower lock-in amplifiers are set by the variables *SwDec13*, *SwInc13*, *SwDec15* and *SwInc15*. Normally the *SwDec* values are 0.55 and the *SwInc* values are 0.65. If the software is currently reading the upper lock-in

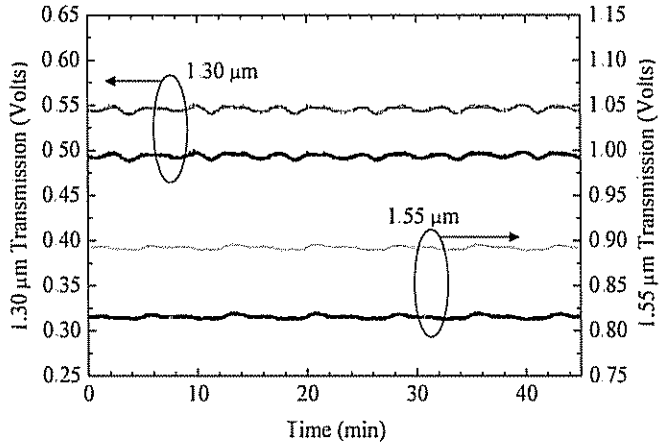


Figure E.7: Measured fluctuations in the laser transmission values after the ventilation output was redirected away from the optical components.

amplifier, it will switch to the lower lock-in only if the measured transmission, as a fraction of the lower lock-in amplifier range, is larger than a constant set by *SwDec*:

$$\frac{T_\lambda}{1.5 \times lower\ lockin\ range} < \frac{10^{SwDec\lambda}}{5} = 71\% \qquad \text{(E.6)}$$

Similarly, if the software is currently reading the lower lock-in amplifier, it will only switch to the upper lock-in if the measured transmission divided by the lower lock-in amplifier range, is larger than a constant specified by *SwInc*:

$$\frac{T_\lambda}{1.5 \times lower\ lockin\ range} > \frac{10^{SwInc\lambda}}{5} = 89\%$$

Note that hysteresis is built into the system so that when the transmission is in the middle of the lower lock-in amplifier range (71-89%), the program continues to read whichever lock-in it is currently reading, and therefore the program does not toggle rapidly between the two. The specific lock-in amplifier used by the temperature control system is output to the screen (and can be logged) during sequences. The user should insure that the desired lock-in amplifier is being used for temperature control. Normally, *SwDec* and *SwInc* should not need changing.

E.6 Summary

In this appendix the RTCVD temperature control system has been explained in detail, and suggestions have been given for how to improve temperature control. By correct selection of the variables *Lim1.3* and *Lim1.5*, the process temperature window where both or neither of the lasers are in use can be minimized, for optimal transitions between the two lasers. By assuming exponential dependence of the transmission on the wafer thickness, the temperature of thick wafers can be well controlled. By minimizing swings in room temperature near the optical components, fluctuations in the cold transmission values have been minimized, allowing for more precise temperature control particularly at low temperatures. Finally, the selection of the lock-in amplifier settings were discussed. Equipped with a good understanding of the RTCVD system, it is possible to obtain excellent control of the deposition temperature as shown in Fig. 7.10.

Appendix F

Bonding Sample List

This appendix describes samples available for wafer bonding.

F.1 BPSG coated wafers

The BPSG was deposited by Northrop Grumman, courtesy of Anthony Margarella, unless otherwise noted. The BPSG thickness is measured immediately after deposition; the final thickness may be thicker due to the wet or dry oxidation step that follows BPSG deposition. These wafers are kept at Naval Research Laboratory by Karl Hobart.

Northrop Processing Date	*BPSG thickness*	*Wafer diameter*	*# wafers received*	*# wafers left*	*Notes*
June 2002	1 μm	6"	10	2	
Feb 2003	200 nm	6"	10	6	
Feb 2003	50 nm	6"	10	0	(1)
March 2005	25 nm	6"	8	7	(2)
Nov 2004	200 nm	6"	20	7	
-	200 nm	4"	25	17	(3)

Table F.1: BPSG coated wafers available for wafer bonding at the Naval Research Lab.
Notes:

1. The BPSG thickness listed was measured after CVD deposition of BPSG. Following BPSG deposition, the wafers were wet oxidized to densify the BPSG. This increased the BPSG thickness of 95 nm (as measured by optical reflectometry) and increased the viscosity by ~1000x as described in Sec. 4.2 and 6.2.3.
2. In March 2005, Northrop used a wet etch to strip the BPSG from the wafers described in Note 1, and redeposited 25-nm BPSG, followed by a dry oxygen anneal. The 25-nm BPSG also has a high viscosity (see Sec. 6.2.3).
3. These 8" wafers were ordered from Wafernet, and were trimmed to 4" by Unisil. Karl Hobart has found that these wafers do not bond well, even after pre-bonding anneals of up to 1000°C.

F.2 Si/SiGe wafers

F.2.1 Wafers from 2004 Epitaxy

These 4" wafers were grown by Lawrence Semiconductor Research Laboratory (LSRL) in 2004 on quote #1426R for Princeton University, where they are now kept. The starting materials are prime-grade, single-side polished 4" (100) p-type silicon wafers with resistivity of > 1 Ω-cm. LSRL grew a $Si_{0.7}Ge_{0.3}$ layer capped with a silicon layer. Sometimes additional $Si_{1-y}C_y$ (y<1%) and $Si_{0.7}Ge_{0.3}$ layers were grown in between the outer SiGe base and top silicon cap layers. The specifications are given below in Table F.2.

From calibration samples run immediately before and after the epitaxy growth, in the SiGe layer the oxygen concentration is 1-4x10^{18} cm^{-3} and the boron concentration 2-4x10^{17} cm^{-3}.

Specification	t_{Si} *top (nm)*	t_{SiGe} *30% (nm)*	t_{SiC} *(nm)*	*C %*	t_{SiGe} *30% (nm)*	*# wafers recv'd*	*# wafers left*	*Proton Implant ?*	*Wafer numbers*
1426R-1	2	0	0	-	30	2	2	No	51119 A,B
1426R-2	10	0	0	-	30	9	7	No	51119 E,F,G, H,I,J,K
1426R-3	15	0	0	-	30	9	7	No	51119 N,O,P, Q,R,S,T
1426R-4	25	0	0	-	30	9	7	No	51119 W,X,Y; 51120 A,B,C,D
1426R-5	30	0	0	-	30	9	7	No	51120 G,H,I,J,K,L,M
1426R-6	10	0	50	0.4%	10	4	3	No	51120 O,P,Q
1426R-7	25	4	70	0.4%	10	4	3	No	51120 S,T,U
1426R-8	25	4	70	0.8%	10	4	3	No	51120 W,X,Y

Table F.2: Si/SiGe wafers available for wafer bonding at Princeton University.

F.2.2 Wafers from Previous Epitaxy

These 4" wafers were grown by LSRL during previous epitaxy orders. They are stored at Naval Research Lab; the below list is current as of April 2005. The wafers listed in Table F.3 have not yet had a proton implant. The wafers listed in subsequent tables have been processed in some way since the epitaxial growth.

Specification	t_{Si} *(nm)*	t_{SiGe} *(nm)*	*Ge content*	*# wafers recv'd*	*# wafers left*	*Proton Implant ?*	*Comments*
50144 spec 1	2	30	30%	20	7	No	50144 N,O,P,Q,R,T,S
50145 spec 2	5	30	30%	20	13	No	50145 H,I,J,K,L,M, N,O,P,Q,R,S,T
50146 spec 3	2	10	50%	5	2	No	50146 D,E
50147 spec 4	0	5	60%	5	4	No	50147 B,C,D,E; have visible texture in Nomarski and could not be bonded
50148 spec 5	0	30	30%	10	5	No	50148 F,G,H,I,J
30055 F, G	50	30	30%	--	2	No	
30055 A, B	100	30	30%	--	2	No	
160219 T, U-3	4	30	30%	--	2	No	
160219 V, W, X-4	2	30	30%	--	3	No	
160219 Q, R-2	9	30	30%	--	2	No	
160219 AA, BB-3	4	30	30%	--	2	No	<100> off orientation
30059 C, D, E	10	30	30%	--	3	No	(211) oriented, off orientation

Table F.3: Si/SiGe wafers for wafer bonding, which have not been proton implanted or otherwise processed.

Specification	t_{SiNx} *(nm)*	t_{Si} *(nm)*	t_{SiGe} *(nm)*	*Ge content*	*# wafers left*	*Proton Implant?*	*Comments*
30055P	5.5	10	30	30%	1	IS #8441 5/03	P-clean Feb 2005, slot #8

Table F.4: Si/SiGe wafers for wafer bonding that have been proton implanted and wet cleaned, and have a 5.5-nm SiN_x cap layer, from a box labeled "IS-Princeton 3" kept at Naval Research Lab.

Specification	t_{Si} *(nm)*	t_{SiGe} *(nm)*	*Ge content*	*# wafers left*	*Proton Implant?*	*Comments*
F35A-826 spec 2	5	30	30%	1	IS #8175 1/03	Slot #6
F35A-888 spec 2	5	30	30%	1	IS #8175 1/03	Slot #7
F35A-020 spec 2	5	30	30%	1	IS #8175 1/03	Slot #8
F34A-603 spec 3	2	10	50%	1	IS #8175 1/03	Slot #9
E66A-344 spec 3	2	10	50%	1	IS #8175 1/03	Slot #10
E67A-329 spec 5	0	30	30%	1	IS #8175 1/03	Slot #11
E67A-336 spec 5	0	30	30%	1	IS #8175 1/03	Slot #12

Table F.5: Si/SiGe wafers for wafer bonding that have been proton implanted, from a box labeled "IS-Princeton 2" kept at Naval Research Lab.

Specification	t_{SiOx} *(nm)*	t_{Si} *(nm)*	t_{SiGe} *(nm)*	*Ge content*	*# wafers left*	*Proton Implant?*	*Comments*
E63A-565 spec 1	200	2	30	30%	1	IS #30/7685 3/02	Slot #4, P-clean 11/21
F35A-006 spec 2	200	5	30	30%	1	IS #30/7685 3/02	Slot #6
F35A-004 spec 2	200	5	30	30%	1	IS #30/7685 3/02	Slot #7
F35A-898 spec 2	200	5	30	30%	1	IS #30/7685 3/02	Slot #8
E66A-145 spec 4	200	0	5	60%	1	IS #30/7685 3/02	Slot #10, P-clean 11/21
E66A-078 spec 5	200	0	30	30%	1	IS #30/7685 3/02	Slot #11, P-clean 11/21
E67A-343 spec 5	200	0	30	30%	1	IS #30/7685 3/02	Slot #12
E67A-337 spec 5	200	0	30	30%	1	IS #30/7685 3/02	Slot #13, P-clean 11/21

Table F.6: Si/SiGe wafers for wafer bonding that have been proton implanted and capped with APCVD SiO_2, from a box labeled "IS #30" kept at Naval Research Lab.

Appendix G

Publications and Presentation Resulting from this Thesis

Referred Journal and Conference Papers

1. R. L. Peterson, K. D. Hobart, H. Yin, F. J. Kub, and J. C. Sturm, "Maximizing uniaxial tensile strain in large-area silicon-on-insulator islands on compliant substrates," J. Appl. Phys. **99**, in press (2006).
2. R. L. Peterson, K. D. Hobart, F. J. Kub, H. Yin and J. C. Sturm, "Reduced buckling in one dimension vs two dimensions of a compressively strained film on a compliant substrate," Appl. Phys. Lett. **88**, 201913 (2006).
3. R. L. Peterson and J. C. Sturm, "Dynamics of uniform Si/SiGe uniaxial strain generation on compliant insulating substrates," Digest of the Third International SiGe Technology and Device Meeting (ISTDM), 2006, pp. 254-255.
4. R. L. Peterson, K. D. Hobart, F. J. Kub, and J. C. Sturm, "Comment on 'Fabrication of strained silicon on insulator by strain transfer process' [Appl. Phys. Lett. 87, 051921 (2005)]," Appl. Phys. Lett. **88**, 146101 (2006).
5. H. Yin, K. D. Hobart, R. L. Peterson, F. J. Kub and J. C. Sturm, "Ultra-thin strained-silicon-on-insulator by stress balance on compliant substrates and FET performance," IEEE Trans. on Elec. Dev. **52**, 2207 (2005).
6. H. Yin, K. D. Hobart, R. L. Peterson, S. R. Shieh, T. S. Duffy, and J. C. Sturm, "Tunable uniaxial vs. biaxial in-plane strain in integrated silicon and silicon-germanium thin films using compliant substrates," Appl. Phys. Lett. **87**, 061922 (2005).
7. R. L. Peterson, K. D. Hobart, F. J. Kub, and J. C. Sturm, "Buckling time-scale for compressively-strained thin films on compliant layers of various thickness," Electronic Materials Conference 2005 Tech. Prog., Santa Barbara, CA, June 2005, pp. 60-61.

8. R. L. Peterson, K. D. Hobart, H. Yin and J. C. Sturm, "Crystal-direction dependence of uniaxial tensile strain in ultra-thin SOI," Proc. IEEE SOI Conference, Charleston, SC, Oct. 2004, pp. 39-41.
9. (Invited) J. C. Sturm, H. Yin, R. L. Peterson, K. D. Hobart, and F. J. Kub, "High-perfection approaches to Si-based devices through strained layer epitaxy," Proc. International Conference on Solid State Devices and Materials (SSDM), Tokyo, Japan, Sept. 2004, pp. 220-221.
10. R. L. Peterson, H. Yin, K. D. Hobart, T. S. Duffy, and J. C. Sturm, "Uniaxially-tensile strained ultra-thin silicon-on-insulator with up to 1.1% strain," Electronic Materials Conference 2004 Tech. Prog., Notre Dame, IN, June 2004, pp. 33-34.
11. (Invited) J. C. Sturm, H. Yin, R. L. Peterson, K. D. Hobart, and F. J. Kub, "Strain engineering in SiGe/Si-on-insulator structures using compliant substrate and stress balance approaches," Second International SiGe Technology and Device Mtg. (ISTDM), Frankfurt, Germany, May 2004, pp. 29-30.
12. R. L. Peterson, H. Yin, J. C. Sturm, "Island Scaling Effects on Photoluminescence of Strained SiGe/Si (100)", Mat. Res. Soc. Symp. Proc. **809**, 133 (2004).
13. H. Yin, K. D. Hobart, S. R. Shieh, R. L. Peterson, T. S. Duffy, and J. C. Sturm, "Interference-enhanced Raman Scattering in Strain Characterization of Ultra-thin Strained SiGe and Si Films on Insulator," Mat. Res. Soc. Symp. Proc. **809**, 115 (2004).
14. H. Yin, K. D. Hobart, R. L. Peterson, F. J. Kub, S. R. Shieh, T. S. Duffy, and J. C. Sturm, "Fully-depleted Strained-Si on Insulator NMOSFETs without Relaxed SiGe Buffers," Technical Digest International Electron Devices Mtg. (IEDM), Washington, DC, Dec. 2003, pp. 3.2.1-3.2.4.
15. H. Yin, R. L. Peterson, K. D. Hobart, S. R. Shieh, T. S. Duffy, and J. C. Sturm, "Relaxed SiGe Layers with High Ge Content by Compliant Substrates," Mat. Res. Soc. Symp. Proc. **768**, G1.7.1 (2003).
16. H. Yin, K. D. Hobart, R. L. Peterson, S. R. Shieh, T. S. Duffy and J. C. Sturm, "Strained-Si-on-Insulator MOSFET without Relaxed SiGe Buffer Layer," ICSI3: The SiGe Conference Digest, Santa Fe, NM, Mar. 2003, pp. 181-183.

Conference Presentations

1. R. L. Peterson and J. C. Sturm, "Dynamics of uniform Si/SiGe uniaxial strain generation on compliant insulating substrates," Third International SiGe Technology and Device Meeting (ISTDM), Princeton, NJ, May 2006.
2. R. L. Peterson, K. D. Hobart, F. J. Kub, and J. C. Sturm, "One-dimensional vs. two-dimensional buckling of compressively-strained films on a compliant substrate," Material Research Society Fall Symposium, Boston, MA, Nov. 2005.
3. R. L. Peterson, K. D. Hobart, F. J. Kub, and J. C. Sturm, "Buckling time-scale for compressively-strained thin films on compliant layers of various thickness," 47th Electronic Materials Conference, Santa Barbara, CA, June 2005.
4. R. L. Peterson, K. D. Hobart, H. Yin and J. C. Sturm, "Crystal-direction dependence of uniaxial tensile strain in ultra-thin SOI," IEEE SOI Conference, Charleston, SC, Oct. 2004.
5. J. C. Sturm, H. Yin, R. L. Peterson, K. D. Hobart, and F. J. Kub, "High-perfection approaches to Si-based devices through strained layer epitaxy," International Conference on Solid State Devices and Materials (SSDM), Tokyo, Japan, Sept. 2004.
6. R. L. Peterson, H. Yin, K. D. Hobart, T. S. Duffy, and J. C. Sturm, "Uniaxially-tensile strained ultra-thin silicon-on-insulator with up to 1.1% strain," 46th Electronic Materials Conference 2004, Notre Dame, IN, June 2004.
7. R. L. Peterson, H. Yin, J. C. Sturm, "Island Scaling Effects on Photoluminescence of Strained SiGe/Si (100)", Material Research Society Spring Symposium, San Francisco, CA, Apr. 2004.
8. H. Yin, K. D. Hobart, S. R. Shieh, R. L. Peterson, T. S. Duffy, and J. C. Sturm, "Interference-enhanced Raman Scattering in Strain Characterization of Ultra-thin Strained SiGe and Si Films on Insulator," Material Research Society Spring Symposium, San Francisco, CA, Apr. 2004.
9. H. Yin, K. D. Hobart, R. L. Peterson, F. J. Kub, S. R. Shieh, T. S. Duffy, and J. C. Sturm, "Fully-depleted Strained-Si on Insulator NMOSFETs without Relaxed SiGe Buffers," International Electron Devices Mtg. (IEDM), Washington, DC, Dec. 2003.

10. H. Yin, K. D. Hobart, R. L. Peterson, S. R. Shieh, T. S. Duffy, F. J. Kub, and J. C. Sturm, "Strain engineering on compliant substrates," Material Research Society Fall Symposium, Boston, MA, Nov. 2003.
11. H. Yin, R. L. Peterson, K. D. Hobart, S. R. Shieh, T. S. Duffy, and J. C. Sturm, "High Ge content (~0.6) relaxed SiGe layers by compliant substrate approaches," Material Research Society Spring Symposium, Boston, MA, April 2003.
12. H. Yin, K. D. Hobart, R. L. Peterson, S. R. Shieh, T. S. Duffy, and J. C. Sturm, "Strained-Si-on-Insulator MOSFETs without relaxed SiGe buffer layer," Third International Conference on SiGe(C) Epitaxy and Heterostructure, Santa Fe, NM, Mrach 2003.

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