

interference lengths. In this paper, we investigate a two-fold generalization of Viterbi algorithm and show, by analysis and computer simulation, that the constraint lengths used in the Viterbi algorithm may be chosen somewhat independently of the constraint lengths of codes or the interference lengths of channels and, if this observation is coupled with the notion of list decoding; in the Viterbi algorithm, then we can decode convolutional codes having long constraint lengths or equalize channels having long interference lengths with a moderate increase of the memory size and the amount of computation and with good performances.

OPTIMUM SEQUENCE DETECTION OF ASYNCHRONOUS MULTIPLE ACCESS COMMUNICATIONS, Sergio Verdu, Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL. 61801, U.S.A.. The receiver commonly employed for the detection of asynchronous multiple-access (e.g. direct-sequence spread-spectrum) communications is optimal only asymptotically for low SNR. In this paper, an optimum coherent receiver that provides MAP bit sequence detection for asynchronous K-user communications is obtained and analyzed under the assumptions of binary antipodal signalling of equal duration for every user, equiprobable and independent bits, unconstrained decision delay and knowledge of signal set. The optimum detector consists of a matched filter for every user followed by a maximum-likelihood decision system implementable by a Viterbi algorithm with 2^K states and with a K-dimensional version of the branch metric employed in the maximum-likelihood sequence detection of communications through linear channels with finite impulse response. A union-bound analysis of the error probability of the optimum sequence detector shows that the performance in the high SNR region is determined by the set of minimum error energies (Euclidean distances) for each user, and that for signal sets with only moderate cross-correlation properties there is no degradation due to the presence of other users in the asymptotic effective SNR of each user. (This work was supported by the U.S. Army Research Office under Contract DAAG-81k-0062).

ANALYSIS OF DPLL WITH CLOCK QUANTIZATION AND NONLINEAR OPERATIONS ON THE SAMPLED INPUT, Carlos A. Pomalaza, Clarkson College of Technology, Department of Electrical and Computer Engineering, Potsdam, New York, 13676, U.S.A. and Clare D. McGillem, Purdue University, School of Electrical Engineering, West Lafayette, Indiana, 47907, U.S.A.. A model of a Digital Phase Lock Loop (DPLL) taking into account (1) the discrete nature of the digital clock and (2) nonlinear zero memory operations on the sampled input is reduced to a finite markov chain problem. Both first and second order models are analyzed. The phase error steady state pdf, mean time to skip a cycle and mean time to reach acquisition are obtained for phase step and frequency step signal plus gaussian and nongaussian noise. It is shown that nonlinear operations on the sampled input improve the loop performance even in the cases when the noise is gaussian. These nonlinear operations can be made to take into account any ADC quantization function. The results obtained suggest little or no advantage in