

YU-YUAN CHEN

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EDUCATION

- Princeton University** 9/1/2006 — present
3rd year PhD, Department of Electrical Engineering, GPA 3.80
- National Taiwan University (NTU)** 9/1/2000 — 6/30/2004
B.S., Department of Electrical Engineering, GPA 3.90

CURRENT RESEARCH

- PALMS research assistant (Advisor: [Ruby B. Lee](#))** 9/1/2007 — present
(Princeton Architecture Laboratory for Multimedia and Security)
- Improve system security by making minimal modifications to modern computer systems without losing usability and performance. Currently investigating ways to take advantage of multicore chips to enhance the security of computer systems. Projects undertaken include:
 - Hardware implementation of Secret Protection (SP) architecture
 - Modified the vi text editor to incorporate ORCON access control policy on the SP architecture as the Trusted Software Module (TSM). (On-going)
 - Trust-partitioning of user-level applications. (On-going)
 - Explore the security architecture for multi-core environment. Extend SP architecture to multi-core. (On-going)
 - Protecting the security of a Dynamic Binary Translator (DBT)
 - Fast encryption/hashing engine in FPGA.

WORK EXPERIENCE

- Technical Intern, Intel, Hillsboro, Oregon** 6/2/2008 — 8/29/2008
SeCoE (Security Center of Excellence), Supervisor: [Keen W. Chan](#)
- Security evaluation of Intel® Upgrade Service 2008**
- Participated in the security evaluation of Intel® Upgrade Service 2008 architecture, which allows for aftermarket upgrade of platform capabilities after initial sale to end-customers. Performed extensive code review, debugging and code tracing. Carried out several attacks including man-in-the-middle attack, flash-overwrite, eavesdropping. Identified several flaws and vulnerabilities in the architecture.
- Technical Intern, Intel, Santa Clara, California** 6/4/2007 — 8/31/2007
PSL (Programming Systems Lab), Supervisor: [Youfeng Wu](#)
- Security issues with Dynamic Binary Translator (DBT)**
- Examined potential security issues with DBT. Investigated the operations of DBT, including code discovery, code caching, trace formation, etc., to see if several security functions of the translated program may have been compromised. Tested several programs with security features like self-checksumming, anti-debugging, address space randomization, etc., on Intel's DBT infrastructure, identified some bugs of current DBT and proposed possible solutions.
- Interceptor Controller Technician (ICT), Chinese Air Force, Taipei, Taiwan** 11/21/2004 — 2/21/2006
- Working in the major radar control station governing the strategic air traffic over Taiwan Strait.

PUBLICATIONS

1. **Yu-Yuan Chen**, Youfeng Wu, Shiliang Hu, Ruby B. Lee, "Impact of Dynamic Binary Translators on Security", *1st Workshop on Architectural and Microarchitectural Support for Binary Translation*, International Symposium on Computer Architecture (ISCA), June 2008.
2. **Yu-Yuan Chen**, Ruby B. Lee, "SP-PAX: Hardware implementation of SP module with PAX cryptoprocessor", Princeton University Department of Electrical Engineering Technical Report CE-L2008-004, April 2008.
3. R.B. Lee, A.M. Fiskiran, M. Wang, Y. Hilewitz and **Y. Chen**, "PAX: A Cryptographic Processor with Parallel Table Lookup and Wordsize Scalability", journal submission, 2007.
4. R.B. Lee, **Y. Chen**, "Improving Software AES Performance while Eliminating Cache Side-Channel Attack", submitted to *International Workshop on Fast Software Encryption 2009*.

UNDERGRADUATE RESEARCH EXPERIENCE

- Analog VLSI** 1/1/2004 — 6/30/2004
- Designed a novel burst-mode clock/data recovery circuit.
- Electronic devices** 9/1/2003 — 1/31/2004
- Researched the theory and fabricated a Metal-Oxide-Semiconductor (MOS) temperature sensor
- Nano technology** 2/1/2003 — 6/30/2003
- Simulated and studied the characteristics of the electron in Single-Electron-Transistor (SET).

TECHNICAL SKILLS

- | <i>Software</i> | <i>Hardware</i> | <i>Security</i> |
|---|--|--|
| - <i>C, C++, Java, Python, MATLAB, Bochs emulator</i> | - <i>Verilog, VHDL, HSpice, Cadence, Debussy, SpectreRF, Advanced Design System (ADS), ARM Developer Suite (ADS), QuartusII, MaxPlusII, ModelSim</i> | - <i>IDA Pro, Paros, Wireshark, NMap</i> |

AWARDS AND HONORS

- Second Prize, 13th NTU Engineering Technology Contest 3/1/2004
Modeled the operations of Single Electron Transistors (SET) in MATLAB.
- NTU Presidential Award, Ranking within top 5% 2004
Awarded to the top 5% of the Electrical Engineering department.