The Control Register controls four Counter operating modes and three maskable interrupts. It also reports the status of three interrupt conditions.

**R6500/1 COUNTER MODES**

**INTERVAL TIMER (MODE 0)**
In this mode the Counter is free-running, and decrements at the $\varphi 2$ clock rate. The CNTR line is held high in the high state.

**PULSE GENERATOR (MODE 1)**
In this mode the Counter is free-running, and decrements at the $\varphi 2$ clock rate. The CNTR line toggles from one state to the other when Counter overflow occurs.

**EVENT COUNTER (MODE 2)**
In this mode the CNTR line is used as an event input line. The Counter decrements each time a rising edge is detected on CNTR.

**PULSE WIDTH MEASUREMENT (MODE 3)**
This mode allows accurate measurement of the duration of a low state on the CNTR line. The Counter decrements at the $\varphi 2$ clock rate as long as the CNTR is held in the low state, and stops when CNTR switches to the high state.

**Note:** In all modes Counter overflow sets the Control Register CTRO status bit and causes the Counter to be preset to the Latch value.

**PROCESSOR PROGRAMMING MODEL**

**MACHINE INSTRUCTIONS**

- **ADC** Add Memory to Accumulator with Carry
- **AND** AND Memory with Accumulator
- **ASL** Shift Left One Bit (Memory or Accumulator)
- **BCC** Branch on Carry Clear
- **BCS** Branch on Carry Set
- **BEQ** Branch on Result Zero
- **BIT** Test Bits in Memory with Accumulator
- **BMI** Branch on Result Minus
- **BNE** Branch on Result Not Zero
- **BPL** Branch on Result Plus
- **BRK** Force Break
- **BVC** Branch on Overflow Clear
- **BVS** Branch on Overflow Set
- **CLC** Clear Carry Flag
- **CLD** Clear Decimal Mode
- **CLI** Clear Interrupt Disable Bit
- **CLV** Clear Overflow Flag
- **CMP** Compare Memory and Accumulator
- **CPX** Compare Memory and Index X
- **CPY** Compare Memory and Index Y
- **DEC** Decrement Memory by One
- **DEX** Decrement Index X by One
- **DEY** Decrement Index Y by One
- **EOR** Exclusive-OR Memory with Accumulator
- **INC** Increment Memory by One
- **INX** Increment Index X by One
- **INY** Increment Index Y by One
- **JMP** Jump to New Location
- **JSR** Jump to New Location Saving Return Address
- **LDA** Load Accumulator with Memory
- **LDX** Load Index X with Memory
- **LDY** Load Index Y with Memory
- **LSR** Shift Right One Bit (Memory or Accumulator)
- **NOP** No Operation
- **ORA** OR Memory with Accumulator
- **PHA** Push Accumulator on Stack
- **PHP** Push Processor Status on Stack
- **PLA** Pull Accumulator from Stack
- **PLP** Pull Processor Status from Stack
- **ROL** Rotate One Bit Left (Memory or Accumulator)
- **ROR** Rotate One Bit Right (Memory or Accumulator)
- **RTI** Return from Interrupt
- **RTS** Return from Subroutine
- **SBC** Subtract Memory from Accumulator with Borrow
- **SEC** Set Carry Flag
- **SED** Set Decimal Mode
- **SEI** Set Interrupt Disable Status
- **STA** Store Accumulator in Memory
- **STX** Store Index X in Memory
- **STY** Store Index Y in Memory
- **TAX** Transfer Accumulator to Index X
- **TAY** Transfer Accumulator to Index Y
- **TSX** Transfer Stack Pointer to Index X
- **TXA** Transfer Index X to Accumulator
- **TXS** Transfer Index X to Stack Pointer
- **TYA** Transfer Index Y to Accumulator

### COMPARE INSTRUCTION RESULTS

<table>
<thead>
<tr>
<th>Condition</th>
<th>N</th>
<th>Z</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>A, X, or Y &lt; Memory</td>
<td>1*</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>A, X, or Y = Memory</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>A, X, or Y &gt; Memory</td>
<td>0*</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

*An invalid value for C is complement of N.