Arnab Sinha

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Department of Computer Science & Engineering, IIT Kharagpur

Education:

- **[July 2002 to May 2007] Indian Institute of Technology Kharagpur, West Bengal**

5-year Dual Degree (Integrated B.Tech and M.Tech) in Computer Science & Engineering
CGPA: **9.44/10**. Ranked **1st** in the Department. Ranked **2nd** in the institute.

- **[July 2000 - May 2002] Ramakrishna Mission Residential College, Narendrapur**

Higher Secondary Examination (Aggregate): **89.7%**

- **[July 1994 - May 2000] Ramakrishna Mission Vidyalaya, Narendrapur**

Secondary Examination (Aggregate): **90.0%**

Publications:

Anupam Chattopadhyay, **Arnab Sinha**, Diandian Zhang, Rainer Leupers, Gerd Ascheid, Heinrich Meyr, *"ADL-driven Automatic Test Pattern Generation for Functional Verification of Embedded Processors"* ***To appear in 12th IEEE European Test Symposium, Frieburg May 20-24, 2007.***

Anupam Chattopadhyay, **Arnab Sinha**, Diandian Zhang, Rainer Leupers, Gerd Ascheid, Heinrich Meyr, *"Integrated Verification Approach during ADL-Driven Processor Design"* rsp, pp. 110-118, ***Seventeenth IEEE International Workshop on Rapid System Prototyping (RSP'06), 2006. held at Chania, Crete, on June 14-16, 2006.***

Bhaskar Pal, **Arnab Sinha**, Pallab Dasgupta, P. P. Chakrabarti, Kaushik De"*Hardware Accelerated Constrained Random Test Generation"*, accepted by IET Computers & Digital Techniques**.**

Arnab Sinha, Bhaskar Pal, "*Stensor: A Novel Stochastic Algorithm for Placement of Sensors in a Rectangular Grid*", Presented in paper-presentation competition "Eureka" in Kshitij, IIT Kharagpur, Feb 1-4, 2007. [**Secured 1st position**]

Internship and Training:

1. Summer internship: Institute for Integrated Signal Processing (ISS), RWTH, Aachen, Germany
Under: Prof. Rainer Leupers. (May-July, 2006) in the area of processor verification.

2. Summer internship: Institute for Integrated Signal Processing (ISS), RWTH, Aachen, Germany
Under: Prof. Rainer Leupers. (May-July, 2005) in the area of processor verification.

3. Summer internship: Advanced VLSI Design Laboratory, IIT Kharagpur
Under: Faculties of Electrical Engineering and Computer Science (May-July, 2004)
(Performance was certified to be 'Very Good'.)

Previous Research Experience: (Please refer to my webpage for the abstracts and the final reports)

1. M.Tech Project: Some Novel Methods for Design Intent Verification
Guide: Dr. Pallab Dasgupta, Dept. of Computer Science & Engineering, IIT Kharagpur.

2. Design Lab Project: A Novel Stochastic Algorithm for Placement of Sensors in a Rectangular Field
Guide: Dr. Niloy Ganguly, Dept. of Computer Science & Engineering, IIT Kharagpur.

3. B.Tech Project: Synthesis and Model Extraction of A Constrained Random Testbench
Guide: Dr. Pallab Dasgupta, Dept. of Computer Science & Engineering, IIT Kharagpur.
(***Synopsys*** funded this project. This project was nominated for the Best Undergraduate B.Tech Project Award) [thesis]

Fellowships and Scholarships / Job Offer:

- Recipient of following fellowships from the Graduate Schools of USA:
  - Gordon Y.S. Wu Fellowship from Princeton University,
  - Carnegie Institute of Technology Dean's Tuition Fellowship from Carnegie Mellon University,
  - Cornell Fellowship from Cornell University,
  - Microelectronics and Computer Development (MCD) Fellowship University of Texas, Austin,
  - Open Offer from University of Illinois, Urbana Champaign.
- Received job offer from **Microsoft, India Development Center**, Hyderabad
- Merit cum Means (MCM) Scholarship (For four consecutive years 2002-2006) from IIT Kharagpur
- 5th (in state) in maths aptitude test by Association for Improvement of Mathematics Teaching(AIMT) in X
- C.V.Raman Scholarship for hobby activities in Mathematics in School

Skills:

Natural Languages: English, German, Hindi, Bengali
Computer Languages: Proficient in C/C++, Java, Verilog, Python.
Operating Systems: Linux, Solaris, Windows.
Architectures: DEC-Alpha, Sun Solaris, 8085 Microprocessor.
Softwares: Latex, Circuit-Maker, Design Analyzer, Xilinx Integrated Software Environment, Logic Analyzer(ATE), Design Compiler (Synopsys) as a part of the training on VLSI Design.

Other Academic Achievements:

- **33rd in WBJEE** (2002) (**99.9 percentile** of approx 50,000 aspirants)
- Selected in **Indian Statistical Institute**, Kolkata for the B.Stat program, 2002
- Cleared State Level of the **National Talent Search Examination**
- Cleared **Regional Mathematical Olympiad** (RMO) IN 2000 AND 2001 (4th in the region) and participated in INMO (2000, 2001)

Extra Curricular Activities:

- **1st** in the **State** (organized in Kolkata), **Regional** (Bhopal), and **National** (New Delhi) **Level Debate Competition** organized by **NCERT**.
- **2nd** in "**Opensoft**", Inter-Hall Software Development Competition, IIT Kharagpur, 2007.
- **2nd** (2006) and **3rd** (2004) in a marketing strategy game "**Exemplar**" in Techno-Management fest Kshitij, IIT.
- **3rd** in "**Case-a-Franca**" (consultancy project on 3G mobile market in India) in Kshitij, 2006,
- Member of the **problem design team** for annual online programming contest, **BITWISE** 2006,
- Nominated as the B.Tech **representative for placements**, 2005-06 for the Department of CSE.
- **Student-counselor** in the counseling program of the UG students (successful candidates of IIT-JEE, 2004), in June 29-July 2, 2004.