16.7 A 65nm Sub-V_t Microcontroller with Integrated SRAM and Switched-Capacitor DC-DC Converter

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Sub-threshold operation has proven beneficial for energy-constrained systems, as it enables minimum energy consumption in logic circuits during active computation [1], and reduces leakage current in components that must be constantly powered. Previous sub-V_t research, for example a 0.13μm processor with an 8b ALU and 2Kb SRAM [2], has demonstrated substantial energy savings. However, process scaling presents a new challenge in the form of heightened intra-die variation. Efficient power conversion and delivery is another essential consideration for a micro-power system. This paper presents a 65nm sub-V_t SoC featuring a microcontroller core and custom 128Kb SRAM functional in sub-threshold, powered by a switched capacitor DC-DC converter that delivers variable load voltages from 0.3V to 0.6V.

The sub-V_t microcontroller implements a 16b RISC architecture with unified instruction and data memory, supporting 27 instructions and 7 addressing modes based on the standard MSP430 instruction set. GPIO ports and a watchdog timer are included as peripherals. A JTAG interface enables controlling the CPU externally and allows programming of the SRAM at start-up. The system features three low power modes in which clocks to the CPU and peripherals are shut off as indicated in Fig. 16.7.1.

The logic is divided into two power domains; unused blocks are power-gated during standby using an on-chip PMOS sleep transistor as shown in Fig. 16.7.1. At this time, the SRAM and key CPU states can be powered at 300mV for data retention while minimizing leakage. The oscilloscope plot of Fig. 16.7.6 illustrates the core logic emerging from standby after power has been restored to the gated components. Additionally, the memory interface provides a one-entry cache, where a 64b memory row is stored during a single memory read. Successive 16b accesses to the same row require no further memory activity.

Logic design must account for the exponential effect of V_t variation on sub-V_t currents. At the 65nm node, even a static CMOS logic style does not guarantee functionality in sub-V_t, as illustrated by Monte Carlo simulations in Fig. 16.7.2. Process variation can randomly weaken the pull-up or pull-down network, thus degrading noise margins of logic gates. In a sub-V_t register, inverters with reduced output levels decrease the hold SNM of latches and affect data retention. Moreover, as shown in the transient simulation of Fig. 16.7.2, a clock buffer with reduced output swing can cause contention, thus impeding signal propagation.

A custom cell library was developed to address the above challenges. Logic gates were sized to provide sufficient noise margins in Monte Carlo simulation as per [3]. The maximum fan-in was restricted to 3, allowing logic to be synthesized efficiently while avoiding excessive stacking. Several register designs were evaluated in sub-V_t, and the multiplexer-based static register was chosen for robustness. The cross-coupled inverters and clock buffers were sized appropriately to avoid the above failure modes.

To minimize leakage power in the memory, this system includes a 128Kb SRAM designed to operate down to the same minimum V_{DD} as the core logic. The 8T bit-cell consists of a 6T cell and a 2T read-buffer, which removes read SNM limitations by isolating the storage node from the read bitline. To improve readability, sub-V_t read-line leakage is eliminated by controlling the feet of all un-accessed read-buffers. To improve write-ability, peripheral write drivers lower the cell supply voltage to weaken the internal cell feedback, while boosting the wordline by 50mV strengthens the access devices. The SRAM is primarily based on [4] with two main modifications: the number of bit-cells in a column is reduced to 64 from

256 to improve speed and read reliability; devices in the read-buffer are lengthened to achieve higher speed and lower read current variability in sub-V_t.

A custom timing closure approach was developed to account for increased delay variability in sub-V_t. As shown in Fig. 16.7.3, delay distributions of timing paths in the microcontroller can have similar means but drastically different variances. Furthermore, setup and hold time distributions of various register types are not well-modeled by canonical forms. To address these issues while keeping simulation times reasonable, a custom script was applied to an exhaustive list of timing paths generated by commercial software, in order to select a subset of paths for detailed analysis. The paths are first binned by nominal hold time margin. Within each bin, the script then estimates the delay variation (σ/μ) of each path, considering both device sizes and logic depth. Finally, paths with the highest σ/μ from each bin undergo Monte Carlo simulation, which gives accurate delay distributions and indicates whether extra buffering is necessary for satisfying hold time constraints.

An efficient DC-DC converter supplying ultra-low voltages is essential for realizing full power savings in sub-V_t. In this system, a switched-capacitor (SC) DC-DC converter with on-chip charge-transfer (flying) capacitors can provide voltages from 0.3V to 1.1V, although the logic and SRAM only utilize voltages up to 0.6V. The SC converter, shown in Fig. 16.7.4, improves upon a 0.18μm prototype described in [5]. The converter employs five different gain settings to maintain nearly constant efficiency with change in load voltage. A suitable gain setting (G<4:0>) is chosen depending on the load voltage being delivered. Charge-recycling techniques are added to this implementation to mitigate the loss in efficiency due to bottom-plate parasitics. The charge recycling block employs an on-chip bond-wire inductor and a 30pF charge-recycling capacitor. The converter uses an all-digital Pulse Frequency Modulation control method to regulate the output voltage. The enable signal enW<2:0> adjusts the width of the switches to reduce switching losses when the load power delivered scales down. The converter achieves a peak efficiency of 78% at 530mV load voltage and 182μA load current. Its efficiency while delivering 500mV load voltage is provided in Fig. 16.7.4. The SC converter together with the charge-transfer capacitors occupy 0.12mm² in total area and can deliver load power levels up to 400μW.

Figure 16.7.5 summarizes the performance of the fabricated SoC shown in Fig. 16.7.7. The minimum energy point occurs at 500mV, where the logic and memory together consume 27.3pJ/cycle operating at 434kHz. The DC-DC converter achieves 75% efficiency at the corresponding power level with the microcontroller as a load. During standby mode, the DC-DC converter enables dynamically scaling V_{DD} to 300mV, where the combined power for core logic and SRAM is less than 1μW, as plotted in Fig. 16.7.6. Accounting for the efficiency loss at ultra-low power levels, this provides a 2.1× leakage power reduction compared to keeping V_{DD} constant at 500mV during standby.

References:
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[2] B. Zhai, et al., "A 2.60pJ/Inst Subthreshold Sensor Processor for Optimal Energy Efficiency," *IEEE Symp. VLSI Circuits*, pp. 154-155, June 2006.
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[4] N. Verma and A. P. Chandrakasan, "A 65nm 8T Sub-V_t SRAM Employing Sense-Amplifier Redundancy," *ISSCC Dig. Tech. Papers*, pp. 328-329, Feb. 2007.
[5] Y. K. Ramadass and A. P. Chandrakasan, "Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applications," *IEEE Power Electronics Specialists Conference*, pp. 2353-2359, June 2007.
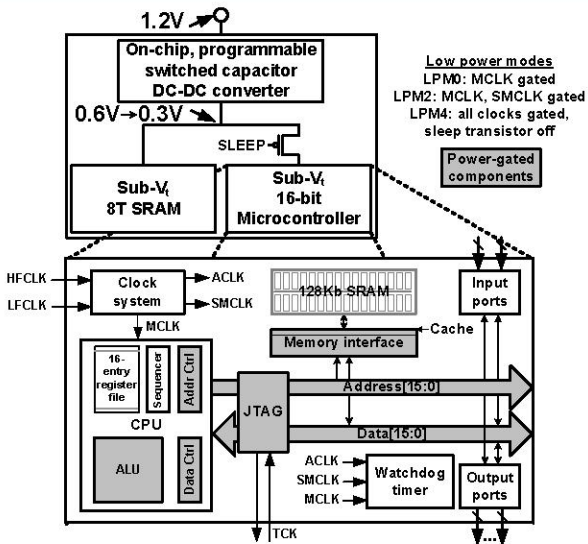
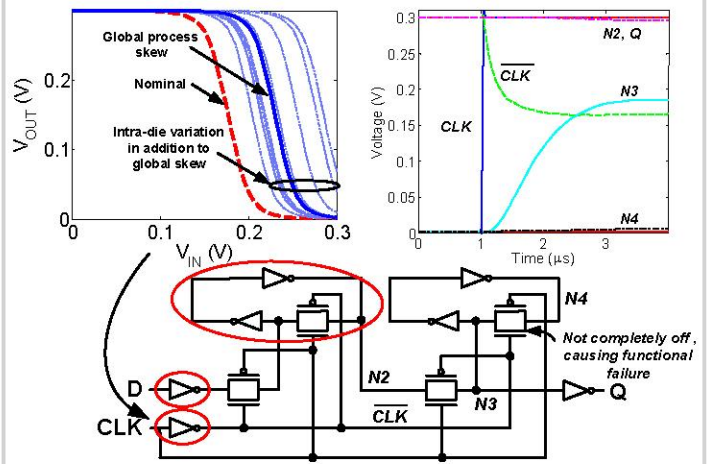Figure 16.7.1: Block diagram of sub-V_t microcontroller.

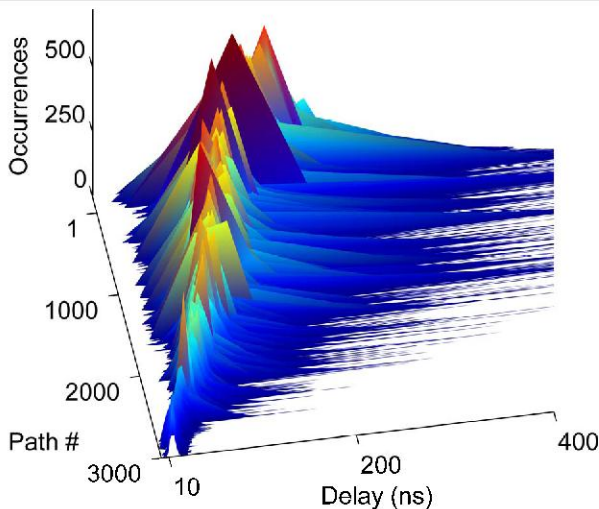Figure 16.7.2: Process variation degrades noise margins in logic circuits, leading to functional failures.

Figure 16.7.3: Simulated delay distributions of 3000 timing paths in the microcontroller at 0.3V, fast corner. Each horizontal cross-section plots the distribution of one path under intra-die variation.
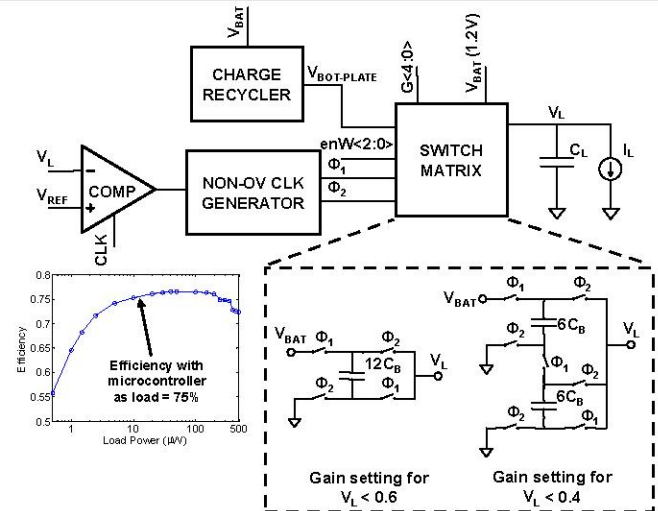

Figure 16.7.4: DC-DC converter architecture and measured efficiency while delivering 500mV. Two of five different gain settings incorporated into the switch matrix are shown in the inset.

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Sub-V_t Test-Chip Summary	
Process Technology	65nm CMOS
Area	
DC-DC Converter	0.12mm²
SRAM	1.36mm²
Logic	0.14mm²
Performance	
Minimum Energy Point	V_{DD} = 500mV
Minimum Functional Voltage	V_{DD} = 300mV
Peak DC-DC Converter Efficiency	78%

V_{DD}	Energy/Cycle	Frequency
500mV	27.3pJ	434kHz
550mV	28.1pJ	651kHz
600mV	29.9pJ	1.04MHz

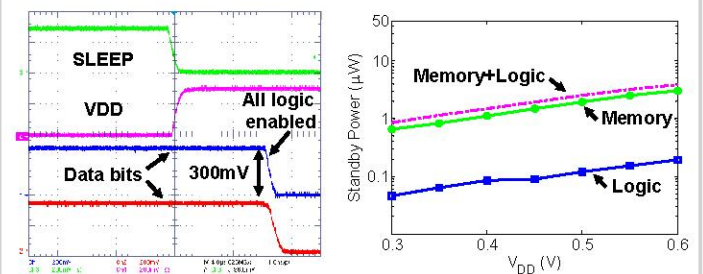Figure 16.7.5: Performance summary of sub-V_t test-chip.

Figure 16.7.6: Oscilloscope plot of sub-V_t core logic emerging from standby mode and plot of standby power. Unused logic blocks are power-gated and all clocks are gated during standby.
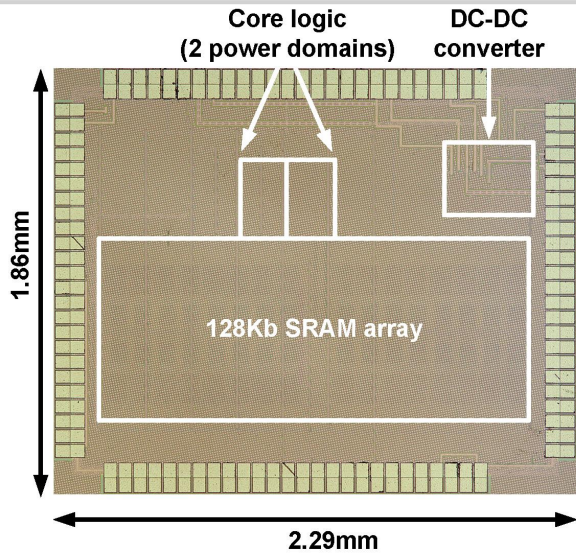
Core logic
(2 power domains)

DC-DC
converter

1.86mm

128Kb SRAM array

2.29mm

Figure 16.7.7: Die micrograph of sub-V_t test-chip.