Specification

for

90nm Generic Process Design Kit (gpdk090) Rev 4.4

Author: John Goelz

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1 Executive Summary

Process Design Kits are one of the four essential pillars that make up a Design Environment or Platform. The other being flows, tools and libraries.This document provides the specification for the 90nm Generic Process Design Kit (gpdk090) for future CIC product releases 6.x. The GPDK needs to support the following Cadence Design Systems, Inc. products (see section 3 for a complete list):

- IC613
  - VSE-L
  - VSE-XL
  - ADE-L
  - ADE-XL
  - VLS-L
  - VLS-XL
  - VLS-GXL
- FINALE71
- IUS81
- MMSIM70
- ASSURA32
- EXT71
- ANLS71
- SOC71

Design kits have always been required in support of product testing and demos and examples to customers. These design kits have typically been very rudimentary and loosely supported. Now that the Cadence desires to have a design kit with its products, a more comprehensive and robust design kit is required to support the Custom IC Platform.

The GPDK090 will address the following requirements:

- Provide foundation for flow development and testing of Custom IC Platform.
- Provide foundation for CIC product demos and flows
- Aid customers in PDK development
- Improve CIC Product Validation engineering's ability to test the products and defined flow.
- Provide Product R&D a more practical design kit to use for their testing and product development.
- Help ES and customer support in answering questions regarding design kits relative to our CIC products and flow(s).
- Provide a generic PDK which does not contain any 3rd party IP and can be freely distributed.
- The GPDK090 should be as realistic as legally possible.

2 Overview

2.1 High-level Product Description

REQ 2.1.1 :

GPDK090 is a complete design kit based on a fictitious 90nm BiCMOS process. The elements of the design kit will support a CIC front to back design flow based on the Custom IC Platform.

REQ 2.1.2 :

The GPDK090 for the CIC platform should target a 90nm 1.8V/2.5V BiCMOS process.

2.2 Problem Statement

Currently the Custom IC product line does not have a consistent design kit that can support flow testing, flow demos, flow training and flow evaluations of our products as well as for Methodology Services in delivering services to customers and practical examples from which R&D can test their code.

2.3 Goal

Provide a 90nm Generic Process Design Kit that is robust, complete and available. The GPDK090should support the Custom IC Platform release.

3 Supported Tools

The following tools should be supported by the GPDK. Some tools may not require any data to be provided by the PDK.

Tool	Key Products	Data provided by GPDK
Design Creation and Simulation	**IC61 (VSE-L, VSE-XL,ADE-L, ADE-XL)** **MMSIM61** **IUS61**	
Composer	Schematic Editor	Symbol views, CDFs, & callbacks
ADE	Analog Design Environment	-
Spectre/Spectre RF	Spectre Circuit Simulator	Device Models, Simulation Views, & Netlisting Information
AMS	Analog Mixed Signal Simulator	Uses Spectre Info
Ultrasim	Fast Circuit Simulator	Uses Spectre Info
Physical Implementation	**IC61 (VLS-L, VLS-XL,VLS-GXL)**	
Virtuoso L	Layout Editor	Technology File, Display Resource File
Virtuoso XL	Schematic Driven Layout	Technology File, CDFs, & Pcells
Toolbox	Layout Editor Toolbox	Technology File
VLO	Layout Editor Optimize	Technology File
VLM	Layout Migrate	External QTT file
DRD	Design Rule Driven Layout	Technology File
Xstream	GDSII in/out	Stream Mapping File
Modgens	Module Generators	Technology File
Analog Placer	Layout Custom Placer	Technology File

CCAR	Chip Assembly Router	Technology File
Qcells	***Layout Quick Cells***	***Technology File***
Place & Route	**SOC71** **FINALE72**	
LEF/DEF		LEF File
Finale	Cadence Spaced Based Router	LEF File
Physical Verification	**IC61** **ASSURA316** **EXT62** **ANLS62**	
Assura DRC	Design Rule Checker	Assura DRC deck
Assura LVS	Layout vs Schematic Checker	Assura LVS files
Assura RCX	Parasitic Extraction Tool	Assura RCX files
Diva DRC	Design Rule Checker	Diva DRC deck
Diva Extract	Device Extraction Tool	Diva Extract File
Diva LVS	Layout vs Schematic Checker	Diva Compare File
EXT	EXT Techgen Extraction	Tool Technology File
SubstrateStorm		Tool Technology File
Fire&Ice QX		Tool Technology File
VoltageStorm		Tool Technology File
ElectronStorm		Tool Technology File

Tools in ***italic*** are not supported in the current version of the GPDK.

4 Design Creation and Simulation

4.1 Schematic Capture (Composer)

REQ 4.1.1 :
A *symbol* view for each device in the device list.
REQ 4.1.2 :
Skill callbacks to check for invalid inputs and calculations of derived parameters. (e.g ad,as,).
REQ 4.1.3 :
Support for inherited connections.
REQ 4.1.4 :
Symbols must contain cdsTerm(), cdsInst() and cdsParam() labels.

4.2 Analog Design Environment (ADE)

No requirements.

4.3 Spectre/SpectreRF simulation

REQ 4.3.1 :
A *spectre* view for each device in the device list.
REQ 4.3.2 :
A *spectre* entry in the CDF simInfo section.
REQ 4.3.3 :
Device models . Each model name should also include the process name as a prefix to avoid name collisions. (e.g gpdk090_nch , gpdk090_respoly,..)
REQ 4.3.4 :
Corner models for corner simulations.
REQ 4.3.5 :
Statistical models for Monte Carlo simulations.
REQ 4.3.6 :
Models for DC mismatch analysis
REQ 4.3.7 :
rdiff models for n/p-diffusion resistors.
REQ 4.3.8 :
Better model for *npn/pnp* device (i.e hicum/Vbic/Mextram504.)

4.4 AMS

REQ 4.4.1 :
A *spectre* view for each device
REQ 4.4.2 :
A *spectre* model for each device.
REQ 4.4.3 :
A *spectre* entry in the CDF simInfo section.

4.5 UltraSim

REQ 4.5.1 :
A *spectre* view for each device

REQ 4.5.2 :
A *spectre* model for each device.
REQ 4.5.3 :
A *spectre* entry in the CDF simInfo section

5 Physical Implementation

5.1 Virtuoso (VLE)

REQ 5.1.1 :
All layer definitions in technology file.
REQ 5.1.2 :
Basic standardVia devices in technology file.
REQ 5.1.3 :
Complete *constraints* section.
REQ 5.1.4 :
Complex vias with asymetric end-of-line rules in technology file.
REQ 5.1.5 :
Display resource file defining colors, line styles and fill patterns.
REQ 5.1.6 :
The user unit per dbu should be set to 2000uu/dbu.

5.2 Virtuoso XL

REQ 5.2.1 :
Complete *constraints* section in techfile.
REQ 5.2.2 :
Multi-part paths for n/p taps in *devices* section of techfile.
REQ 5.2.3 :
ROD based Pcells to showcase advanced VXL features like stretch handles and auto-abutment. All ROD skill code and utility skill code will be packaged into a context file. The context file is loaded through the libInit.il file when opening the GPDK library.

5.3 Toolbox

REQ 5.3.1 :
Complete *constraints* section in techfile.
REQ 5.3.2 :
Updated *techParam* section in techfile.

5.4 VLO (Optimizer)

REQ 5.4.1 :
Complete *constraints* section in techfile.
REQ 5.4.2 :
Updated *devices* section in techfile.

5.5 VLM (Migrator)

REQ 5.5.1 :
External *QTT* file for migration.

5.6 DRD (Wire Editor)

REQ 5.6.1 :
Complete *constraints* section in techfile.
REQ 5.6.2 :
Updated *viaDefs* section in techfile.

5.7 Xstream

REQ 5.7.1 :
GDSII stream layer mapping table

5.8 Modgens (Constraint Editor)

REQ 5.8.1 :
Complete *constraints* section in techfile.
REQ 5.8.2 :
Updated *viaDefs* section in techfile.

5.9 Analog Placer

REQ 5.9.1 :
Complete *constraints* section in techfile.

5.10 Cadence Chip Assembly Router (CCAR)

REQ 5.10.1 :
Pin and connectivity information on Pcells.
REQ 5.10.2 :
Complete *constraints* section in techfile.
REQ 5.10.3 :
Updated *viaDefs* section in techfile.

5.11 Qcells

Requirements: TBD

6 Place and Route

6.1 LEF/DEF

Requirements: TBD

6.2 Finale (Shape Based Router)

Requirements: TBD

7 Physical Verification

7.1 Assura DRC

REQ 7.1.1 :
A sample *drc.rsf* file for running Assura DRC.
REQ 7.1.2 :
A *drc.rule* file containing rules for layer processing and DRC, grouped under the section *drcExtractRules.* This should also include antenna checks,density checks and fill processing.

7.2 Assura LVS

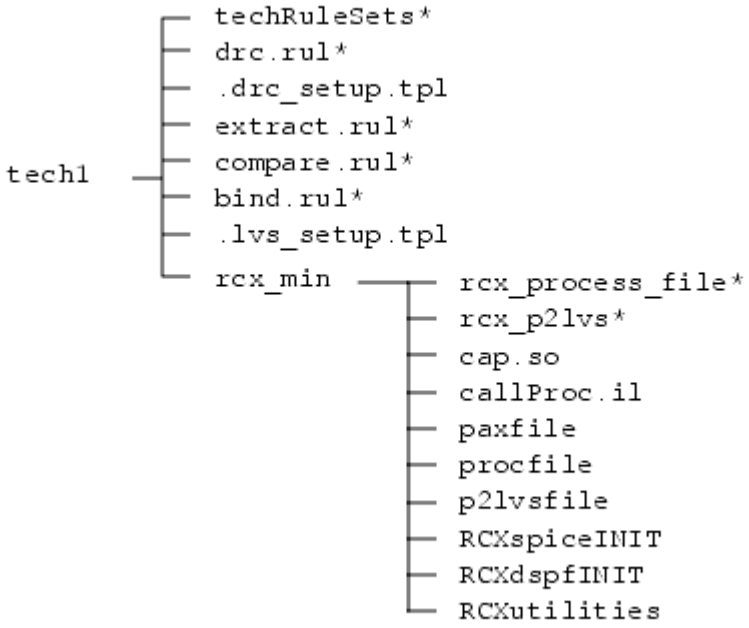
REQ 7.2.1 :
A '*auCdl*' view for every device.
REQ 7.2.2 :
A '*auLvsl*' view for every device
REQ 7.2.3 :
A 'auLvs' entry in the CDF simInfo section.
REQ 7.2.4 :
A 'auCdl' entry in the CDF simInfo section.
REQ 7.2.5 :
A sample LVS.rsf file for running Assura LVS. Provided as a template.
REQ 7.2.6 :
A *techRuleSets* file.
REQ 7.2.7 :
A *extract.rul* file containing rules for layer processing and extracting drawn devices, device parameters, and connectivity (not parasitics), grouped under the section *drcExtractRules.*
REQ 7.2.8 :
A `compare.rul` containing rules for comparing drawn devices and parameters, grouped under the section `avCompareRules`.

7.3 Assura RCX

REQ 7.3.1 :
A `lvsfile`, which is a converted LVS *extract.rul* file that provides LVS device and connectivity information to Assura RCX.
REQ 7.3.2 :
A `p2lvsfile,` which matches the process file to the lvsfile, and also provides technology-based resistance modeling information.
REQ 7.3.3 :
A process description file (*procfile)* for Capgen/Assura RCX.
REQ 7.3.4 :
A Perimeter Area Extraction file (*paxfile*). Thisfile is generated by *capgen*.
REQ 7.3.5 :
Commands used to run the *capgen* simulate and compile steps. (capgen_cmd)

REQ 7.3.6 :
caps2d intermediate file created by *capgen*.
REQ 7.3.7 :
RCXdspfINIT command script for running RCX
REQ 7.3.8 :
RCXspiceINIT command script for running RCX
REQ 7.3.9 :
RCXutilities Korn shell script containing various utilities for processing RCX files.
REQ 7.3.10 :
Compiled capacitance models (*cap.so* file). Generated by *capgen*.

Assura Technology Data Directory



7.4 PVS DRC

REQ 7.4.1 :
A drc.rul file covering all rules defined in the Design Rule manual.

REQ 7.4.2 :
The diva.rul file will be stored under the pvs directory.

7.5 PVS Extract

REQ 7.5.1 :
PVS extract file to extract all devices defined in the device list.
REQ 7.5.2 :
The extract.rul file will be stored in the pvs directory.

7.6 Diva DRC

REQ 7.6.1 :
A divaDRC.rul file covering all rules defined in the Design Rule manual.

REQ 7.6.2 :
The divaDRC.rul file will be stored under the PDK library directory.

7.7 Diva Extract

REQ 7.7.1 :
Diva extract file to extract all devices defined in the device list.
REQ 7.7.2 :
The divaEXT.rul file will be stored in the PDK library directory.
REQ 7.7.3 :
A 'ivpcell' for each device in the device list.

7.8 Diva LVS

REQ 7.8.1 :
A 'auLvs' view for every device in the device list.
REQ 7.8.2 :
A Diva compare file (divaLVS.rul)
REQ 7.8.3 :
The divaLVS.rul will be located under the PDK library directory.

7.9 QRC (Parasitic Extraction)

Requirements: TBD

7.10 SubstrateStorm (Substrate Noise Analysis)

REQ 7.10.1 :
Substrate Technology file defining the different cross-sections in the substrate and the electrical properties (This is obtained from doping profiles for the process). This is the same file as for HF. This file should be named "SCtechnology.gpdk"
REQ 7.10.2 :
Changes to Assura LVS extract and compare rules files to enable SubstrateStorm: This involves identification of the devices, device bulk terminals, substrate regions and contacts and making them appear in the extracted view to be identified by SubstrateStorm for purposes of back-annotation.
REQ 7.10.3 :
Additional layer purpose pairs in the technology library
REQ 7.10.4 :
"SCparameters.cds" file that maps the layers in the extracted view to the substrate technology file
REQ 7.10.5 :
"SCparameters.xtr" file that sets the substrate extraction options.

For more details see the SubstrateStorm Integration spec at
http://partner.cadence.com/gm/document-1.9.97420/sna_integrate_spec.pdf

7.11 Fire & Ice QX

REQ 7.11.1 :

Process information in form of an ASCII-format interconnect technology (ICT) file from which IceCaps generates the technology file for Fire & Ice QX. This technology file contains interconnect models used by Fire & Ice QX to extract the interconnect parasitic capacitance and resistance. For resistance extraction, it contains resistance information on each interconnect layer and via; for capacitance extraction, it contains three-dimensional interconnect models.
The file should be named *gpdk.ict.*
The compiled version of the file *gpdk.tch* should also be part of the GPDK.

7.12 VoltageStorm

REQ 7.12.1 :

Interconnect technology file – gpdk.ict and gpdk.tch – same as those described for Fire and Ice QX .

REQ 7.12.2 :

Tablegen models – In order to use the built-in Spice-like simulators in VS product family, it is required to provide table models for V/I curves for various lengths/widths combination. This is in the form of a dir that is a compiled output of tablegen run. This dir should be provided as part of the GPDK.

REQ 7.12.3 :

XTC command file – this is similar to a LVS deck. XTC is the module within the libgen (library generation process for power grid views). XTC command file contains information about the gds layer map, boolean operations for layer manipulation, device forming statements and connectivity statements

REQ 7.12.4 :

EM Models file - Threshold limits for current density on a per layer basis (for conductors and vias) – this is needed for power electromigration analysis within VST .

7.13 ElectronStorm

REQ 7.13.1 :

Same as VoltageStorm VST. See section 7.12

REQ 7.13.2 :

EM Model file for Signal Electromigration. See document at
http://partner.cadence.com/gm/document-1.9.97422

8 Documentation

REQ 8.1.1 :

The GPDK needs to have a Design Rules Manual (DRM) including layout guidelines and recommendations.

REQ 8.1.2 :

The GPDK should have a Designer Reference Guide.

9 GPDK090 directory structure

The directory structure for the GPDK should be as follows:

Within the <**pdk_install_directory>** directory there are several directories to organize the information associated with the PDK.

assura - Directory containing the Physical Verification Rule Decks for Assura

assura_tech.lib - File containing the Cadence Assura PV initialization path

cds.lib.cdb - File containing the Cadence library definition settings.

This file has the CDB version of the PDK library defined

cds.lib.oa22 - File containing the Cadence library definition settings.

This file has the OA2.2 version of the PDK library defined

dfIItechFiles - Directory containing the ASCII version of the CDB and the OA2.2 DFII techfiles

diva - Directory containing the Physical Verification Rule Decks for Diva

docs - Directory containing the Cadence PDK documentation and the Process design rule manual

fireIce – Directory containing the technology file and layer maps for Fire & Ice

lef – Directory containing the technology LEF file.

libs.cdb – The CDB version of the PDK library

libs.oa22 – The OpenAccess 2.2 version of the PDK library

pvs - Directory containing the Physical Verification Rule Decks for PVS

models - Directory containing the device spectre models

neocell - Directory containing the Neocell technology files

neocircuit - Directory containing the Neocircuit technology file

sna – Directory containing the technology files for SubstrateStorm SNA

soce – Directory containing the Capacitance tables for SOC Encounter

stream - Directory containing the GDSII stream layer map file

vavo - Directory containing the Virtuoso Analog Voltagestorm data file

vcr – Directory containing the Virtuoso Custom Router data file

vlm – Directory containing the Virtuoso Layout Migrate data file

10 GPDK090 Layer Map

The following is a list of the GDSII layers used in the GPDK090:

layer	purpose	streamNumber	dataType
Nwell	drawing	2	0
Oxide	drawing	1	0
Oxide_thk	drawing	24	0
Poly	drawing	3	0
Pimp	drawing	5	0
Nhvt	drawing	18	0
Nimp	drawing	4	0
Phvt	drawing	23	0
Nzvt	drawing	52	0
SiProt	drawing	72	0
Cont	drawing	6	0
Metal1	drawing	7	0
Metal1	label	7	3
Metal1	net	7	4
Metal1	pin	7	1
Via1	drawing	8	0
Metal2	drawing	9	0
Metal2	label	9	3
Metal2	net	9	4
Metal2	pin	9	1
Via2	drawing	10	0
Metal3	drawing	11	0
Metal3	label	11	3
Metal3	net	11	4
Metal3	pin	11	1
Via3	drawing	30	0
Metal4	drawing	31	0
Metal4	label	31	3
Metal4	net	31	4
Metal4	pin	31	1
Via4	drawing	32	0
Metal5	drawing	33	0
Metal5	label	33	3
Metal5	net	33	4
Metal5	pin	33	1
Via5	drawing	34	0
Metal6	drawing	35	0
Metal6	label	35	3
Metal6	net	35	4
Metal6	pin	35	1
Via6	drawing	37	0
Metal7	drawing	38	0
Metal7	label	38	3
Metal7	net	38	4
Metal7	pin	38	1
Via7	drawing	39	0
Metal8	drawing	40	0
Metal8	label	40	3
Metal8	net	40	4
Metal8	pin	40	1
Via8	drawing	41	0

Metal9	drawing	42	0
Metal9	label	42	3
Metal9	net	42	4
Metal9	pin	42	1
CapMetal	drawing	14	0
Nburied	drawing	19	0
Psub	drawing	25	0
Metal1	slot	7	2
Metal2	slot	9	2
Metal3	slot	11	2
Metal4	slot	31	2
Metal5	slot	33	2
Metal6	slot	35	2
Metal7	slot	38	2
Metal8	slot	40	2
Metal9	slot	42	2
Metal1	fill	7	5
Metal2	fill	9	5
Metal3	fill	11	5
Metal4	fill	31	5
Metal5	fill	33	5
Metal6	fill	35	5
Metal7	fill	38	5
Metal8	fill	40	5
Metal9	fill	42	5
Bondpad	drawing	36	0
INDdummy	drawing	16	0
IND2dummy	drawing	17	0
IND3dummy	drawing	70	0
Cap3dum	drawing	84	0
Capdum	drawing	12	0
Resdum	drawing	13	0
BJTdum	drawing	15	0
ResWdum	drawing	71	0
VPNP10dum	drawing	62	0
VPNP2dum	drawing	60	0
VPNP5dum	drawing	61	0
M1Resdum	drawing	75	0
M2Resdum	drawing	76	0
M3Resdum	drawing	77	0
M4Resdum	drawing	78	0
M5Resdum	drawing	79	0
M6Resdum	drawing	80	0
M7Resdum	drawing	81	0
M8Resdum	drawing	82	0
M9Resdum	drawing	83	0
NPNdummy	drawing	20	0
PNPdummy	drawing	21	0
DIOdummy	drawing	22	0
ESDdummy	drawing	74	0
PWdummy	drawing	85	0

11 GPDK090 Device List

The following devices are part of the GPDK090.

Device	Description
npn	Bipolar NPN with variable emitter area
pnp	Bipolar PNP with variable emitter area
vpnp2	1.2 volt Vertical substrate PNP 2x2 fixed emitter
vpnp5	1.2 volt Vertical substrate PNP 5x5 fixed emitter
vpnp10	1.2 volt Vertical substrate PNP 10x10 fixed emitter
mimcap	Metal-Metal Capacitor
ndio	1.2 volt N+/psub diode
pdio	1.2 volt P+/nwell diode
nmos1v	1.2 volt nominal Vt NMOS transistor
nmos1v_hvt	1.2 volt high Vt NMOS transistor
nmos1v_iso	1.2 volt isloated nominal Vt NMOS transistor
nmos1v_nat	1.2 volt native Vt NMOS transistor
nmos2v	2.5 volt nominal Vt NMOS transistor
nmos2v_nat	2.5 volt native Vt NMOS transistor
pmos1v	1.2 volt nominal Vt PMOS transistor
pmos1v_hvt	1.2 volt high Vt PMOS transistor
pmos2v	2.5 volt nominal Vt PMOS transistor
nmoscap1v	1.2v Nmos cap
nmoscap1v3	1.2v Nmos cap with bulk node
nmoscap2v	2.5v Nmos cap
nmoscap2v3	2.5v Nmos cap with bulk node
pmoscap1v	1.2v Pmos cap
pmoscap1v3	1.2v Pmos cap with bulk node
pmoscap2v	2.5v Pmos cap
pmoscap2v3	2.5v Pmos cap with bulk node
resm1–resm9	Metal <k> resistor (k=1-9)
resnsndiff	N+ diffused resistor without salicide
resnsnpoly	N+ Poly resistor without salicide
resnspdiff	P+ diffused resistor without salicide
resnsppoly	P+ Poly resistor without salicide
resnwoxide	N-Well resistor under OD
resnwsti	N-Well resistor under STI
ressndiff	N+ diffused resistor with salicide
ressnpoly	N+ Poly resistor with salicide
resspdiff	P+ diffused resistor with salicide
ressppoly	P+ Poly resistor with salicide

11.1 GPDK090 Device Views

The following PDK views are part of the GPDK090.

Device	schematic#	symbol	spectre	layout*	ivpcell	auCdl	auLvs
npn		x	x	x	x	x	x
pnp		x	x	x	x	x	x
vpnp2		x	x	f	x	x	x
vpnp5		x	x	f	x	x	x
vpnp10		x	x	f	x	x	x
mimcap		x	x	x	x	x	x
ndio		x	x	x	x	x	x
pdio		x	x	x	x	x	x
nmos1v		x	x	x	x	x	x
nmos1v_hvt		x	x	x	x	x	x
nmos1v_iso		x	x	x	x	x	x
nmos1v_nat		x	x	x	x	x	x
nmos2v		x	x	x	x	x	x
nmos2v_nat		x	x	x	x	x	x
pmos1v		x	x	x	x	x	x
pmos1v_hvt		x	x	x	x	x	x
pmos2v		x	x	x	x	x	x
nmoscap1v		x	x	x	x	x	x
nmoscap1v3		x	x	x	x	x	x
nmoscap2v		x	x	x	x	x	x
nmoscap2v3		x	x	x	x	x	x
pmoscap1v		x	x	x	x	x	x
pmoscap1v3		x	x	x	x	x	x
pmoscap2v		x	x	x	x	x	x
pmoscap2v3		x	x	x	x	x	x
resm1–resm9	x	x	x	x	x	x	x
resnsndiff	x	x	x	x	x	x	x
resnsnpoly	x	x	x	x	x	x	x
resnspdiff	x	x	x	x	x	x	x
resnsppoly	x	x	x	x	x	x	x
resnwoxide	x	x	x	x	x	x	x
resnwsti	x	x	x	x	x	x	x
ressndiff	x	x	x	x	x	x	x
ressnpoly	x	x	x	x	x	x	x
resspdiff	x	x	x	x	x	x	x
ressppoly	x	x	x	x	x	x	x

schematic# = schematic pcell to handle series and parallel devices

layout* = cell “x” , fixed layout “f”

12 GPDK090 Device CDF Parameters

An overview of the CDF parameters used in the GPDK090 are as follows:

12.1 Mosfet CDF

Model Name - spectre model name (non-editable)

Multiplier - number of Parallel MOS devices

Length (M) - gate length in meters

Total Width (M) - gate width in meters (sum of all fingers)

Finger Width - width of each gate finger/stripe

Fingers - number of poly gate fingers/stripes used in layout

Threshold – finger width at which to apply device folding of the layout

Apply Threshold – button to apply threshold or not

Gate Connection – allow shorting of multi-fingered devices and addition of contact heads to gate ends

S/D Connection – allow shorting of sources and/or drains on multi-finger devices

S/D Metal Width – width of metal used to short sources/drains

Switch S/D – source is defined as left-most diffusion region and alternating regions to the right. Pins are not automatically permuted and can be switched using this parameter

Bodytie Type – None, Detached, or Integrated (butting source)

- For Detached, user may select Left, Right, Top, and/or Bottom to specify the located of bodyties. Selection of all four creates a guardring
- For Detached, the user may specify Tap Extension (in microns) which sets the distance from the bodytie to the device. Maximum distance is 100 microns
- For Integrated, the user may select Left or Right for a device with an odd number of fingers (1, 3, 5, …). The user may select Left and Right for an even fingered device

Edit Area & Perim – allow Drain/Soure area and periphery be entered manually for simulation

Drain diffusion area, etc. – several simulation parameters are presented. The area and perimeter parameters are calculated and netlisted in accordance with the layouts or can be entered manually if “Edit Area & Perim” is checked

12.2 Resistor CDF

Model Name – Spectre model name (non-editable)

Segments – number of series or parallel segments for a resistor

Segment Connection – cyclic field used for series or parallel segments

Calculated Parameter – radio button that determines whether resistance or Length is the calculated value when instantiating a new resistor device

Resistance – total resistance value equal to the sum of body resistance, contact resistance, end resistance, and grain resistance

Segment Width – resistor segment width in meters

Segment Length – resistor segment length in meters

Effective Width – effective resistor segment width in meters

Effective Length – effective resistor segment length in meters

Left Dummy – boolean value used to place a dummy resistor strip on the left side of the main resistor

Right Dummy – boolean value used to place a dummy resistor strip on the right side of the main resistor

Contact Rows – integer number of contact rows

Contact Columns – integer number of contact columns

Show Tap Params – boolean value allowing the user to set the visibility of the resistor tap properties

Left Tap – boolean value used to place a resistor tap on the left side of a device

Right Tap – boolean value used to place a resistor tap on the right side of a device

Top Tap – boolean value used to place a resistor tap on the top side of a device

Bottom Tap – boolean value used to place a resistor tap on the bottom side of a device

Tap Extension – float values to set where the left, right, top, and bottom taps would be to its original placements. This parameter is related to the stretch handle on the taps. The input format should be “left 1.3 right 1.0 top 0.0 bottom 2.0” without the quotes. If neither pair is not present, a zero is assumed

Sheet Resistivity – sheet rho value for body of resistor (non-editable)

End Resistance – resistance value for any salicided area near the contact heads in a non-salicided resistor (non-editable)

Contact Resistance – resistance value for the contact heads of a particular resistor (non-editable)

Grain Resistance – constant resistance value for any salicided area near the contact heads in a non-salicided resistor (non-editable)

Delta Width – resistor width process variation value in meters (non-editable)

Delta Length – resistor length process variation value in meters (non-editable)

Temperature Coefficient 1 – temperature coefficient #1 for resistor (non-editable)

Temperature Coefficient 2 – temperature coefficient #2 for resistor (non-editable)

12.3 Moscap CDF

Model Name - spectre model name (non-editable)

Multiplier - number of Parallel MOS devices

Calculated Parameter - Calculated parameter cyclic (capacitance, length, width)

Capacitance – total capacitance

Length (M) - gate length in meters

Total Width (M) - gate width in meters (sum of all fingers)

Finger Width - width of each gate finger/stripe

Fingers - number of poly gate fingers/stripes used in layout

Gate Connection – allow shorting of multi-fingered devices and addition of contact heads to gate ends

S/D Connection – allow shorting of sources and/or drains on multi-finger devices

S/D Metal Width – width of metal used to short sources/drains

Switch S/D – source is defined as left-most diffusion region and alternating regions to the right. Pins are not automatically permuted and can be switched using this parameter

Bodytie Type – None, Detached, or Integrated (butting source)

- For Detached, user may select Left, Right, Top, and/or Bottom to specify the located of bodyties. Selection of all four creates a guardring
- For Detached, the user may specify Tap Extension (in microns) which sets the distance from the bodytie to the device. Maximum distance is 100 microns
- For Integrated, the user may select Left or Right for a device with an odd number of fingers (1, 3, 5, …). The user may select Left and Right for an even fingered device

Area capacitance – Capacitance per unit area used in parameter calculations (non-editable)

Fringe capacitance – Fringe Capacitance of perimeter used in parameter calculations (non-editable)

Temp rise from ambient, etc. – several simulation parameters are presented.

12.4 Bipolar CDF

Model name – Model name used in simulation

Device Area – Emitter area in microns squared (non-editable

Emitter width – Emitter width microns

Multiplier – Number of Parallel Bipolar devices

Estimated operating region – Simulation operating region

12.5 Diode CDF

Model name – Model used for simulation name

Calculate Parameter – Choices are 'area' , 'width' or 'length'

Device Area – Calculated junction area in meters squared (non-editable)

Length (M) – Diode length in meters

Width (M) – Diode width in meters

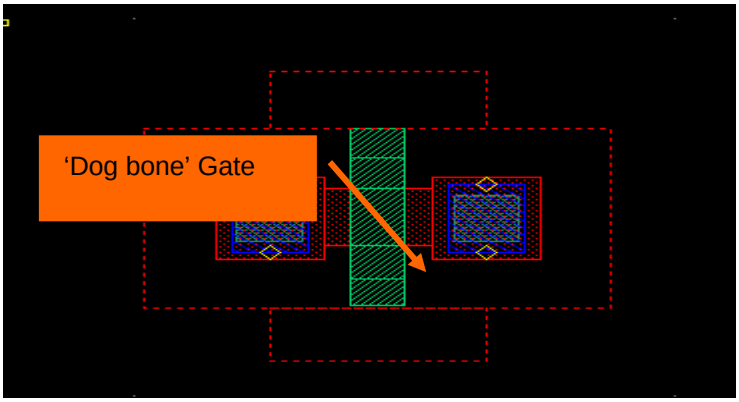
Multiplier – Number of Parallel Diode devices

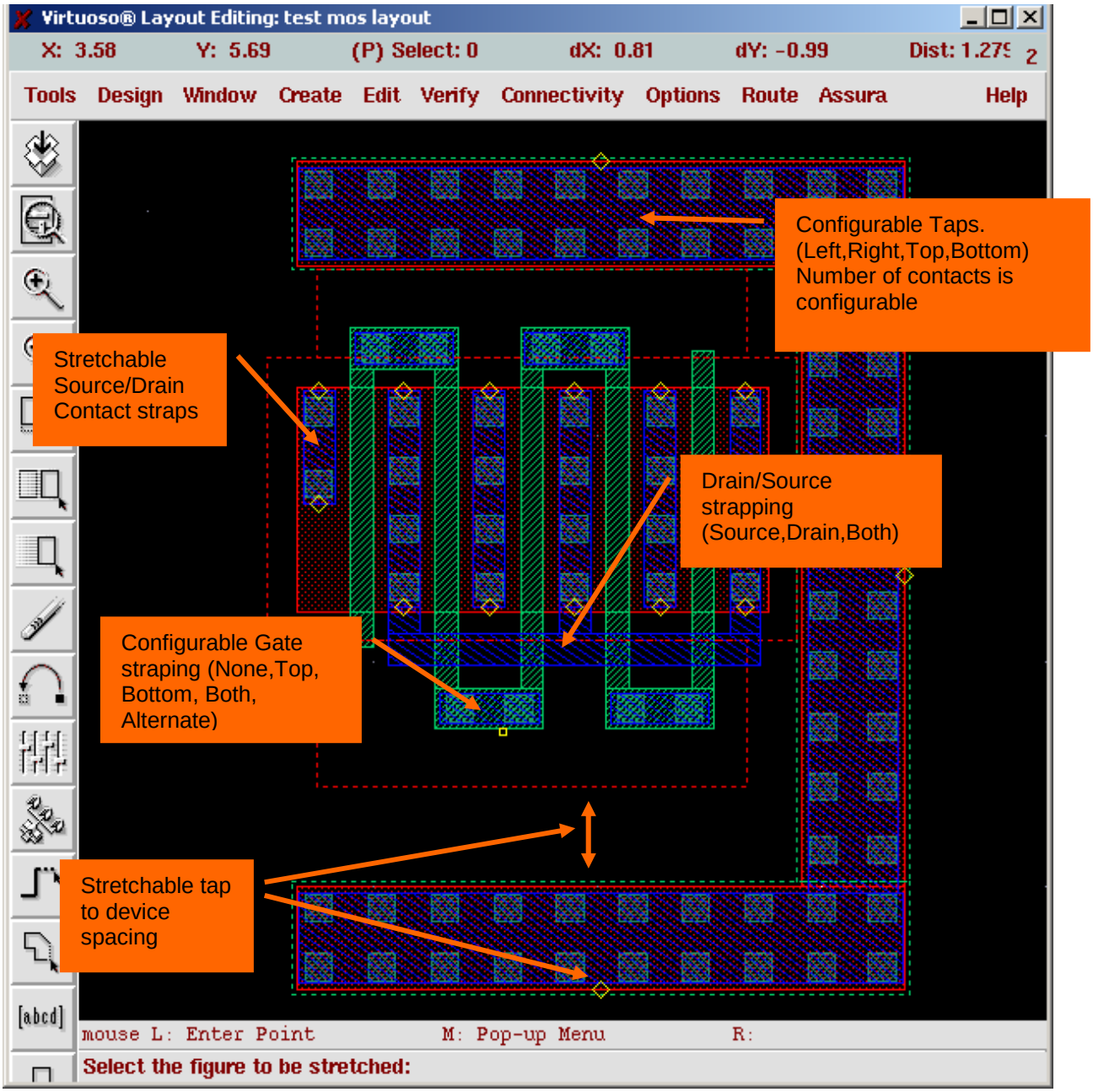
Periphery of junction – Calculated junction periphery in meters (non-editable)

13 GPDK090 Pcell Layouts

13.1 Mos Pcell

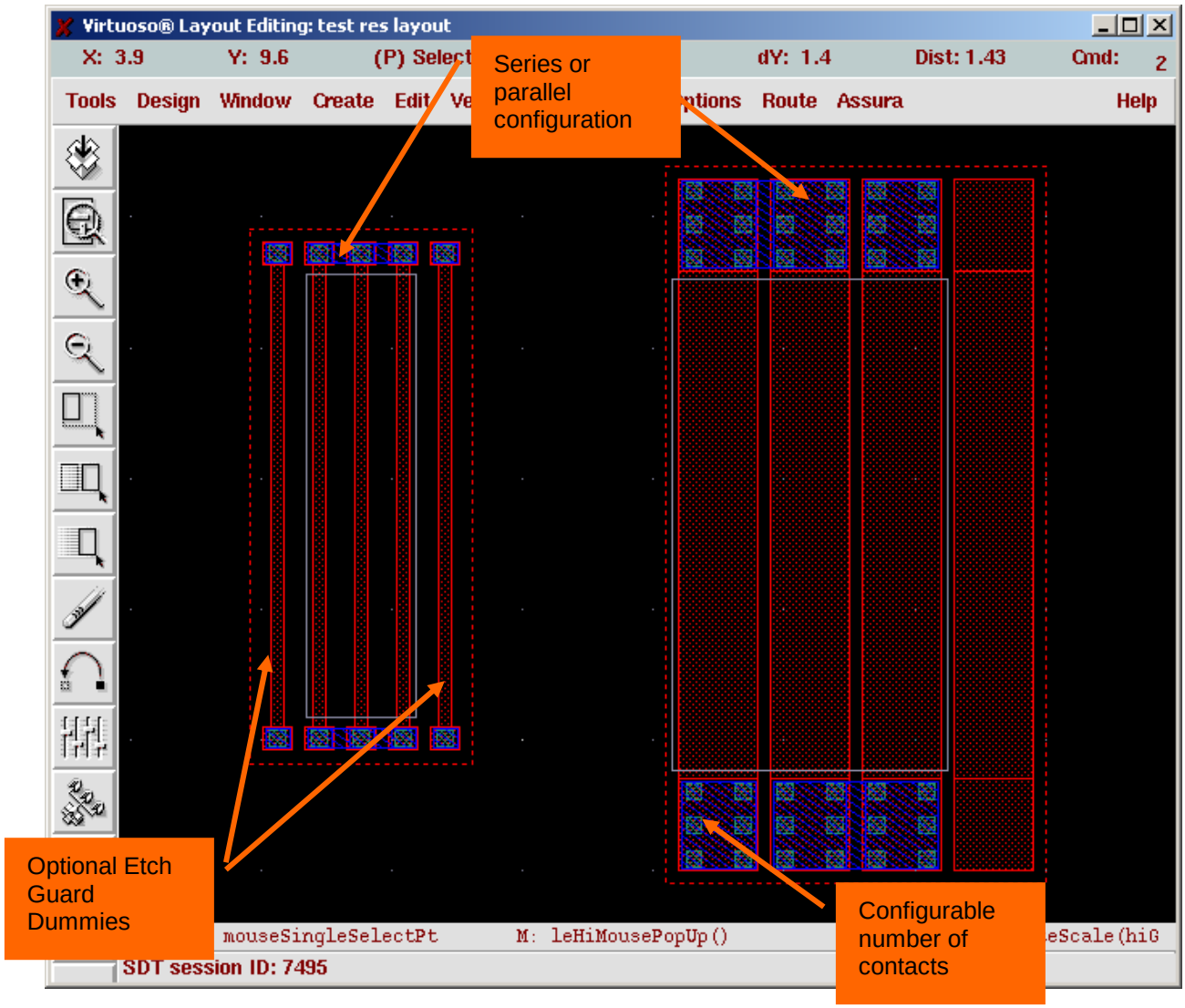
REQ 13.1.1 :
Multi-fingered gates.
REQ 13.1.2 :
Dog bone gate
REQ 13.1.3 :
Configurable source-drain connection for multi fingered devices.(gate,source,both)
REQ 13.1.4 :
Configurable gate straps for multi fingered devices (top, bottom, both, alternate)
REQ 13.1.5 :
Variable source/drain contact coverage with stretch handles on each contact strap.
REQ 13.1.6 :
Optional tap placement for four terminal device. Tab can be configured. (top,bottom,left,right) Spacing between device and tab can be controlled by stretch handle.
REQ 13.1.7 :
Auto abutment enabled.
REQ 13.1.8 :
VXL ready connectivity. Pins access direction needs to allow routing with CCAR.
REQ 13.1.9 :
Permute properties on all pins.


'Dog bone' Gate


Virtuoso® Layout Editing: test mos layout
X: 3.58
Y: 5.69
(P) Select: 0
dX: 0.81
dY: -0.99
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Route
Assura
Help
Configurable Taps. (Left,Right,Top,Bottom) Number of contacts is configurable
Stretchable Source/Drain Contact straps
Drain/Source strapping (Source,Drain,Both)
Configurable Gate straping (None,Top, Bottom, Both, Alternate)
Stretchable tap to device spacing
mouse L: Enter Point
M: Pop-up Menu
R:
Select the figure to be stretched:

13.2 Resistor Pcell

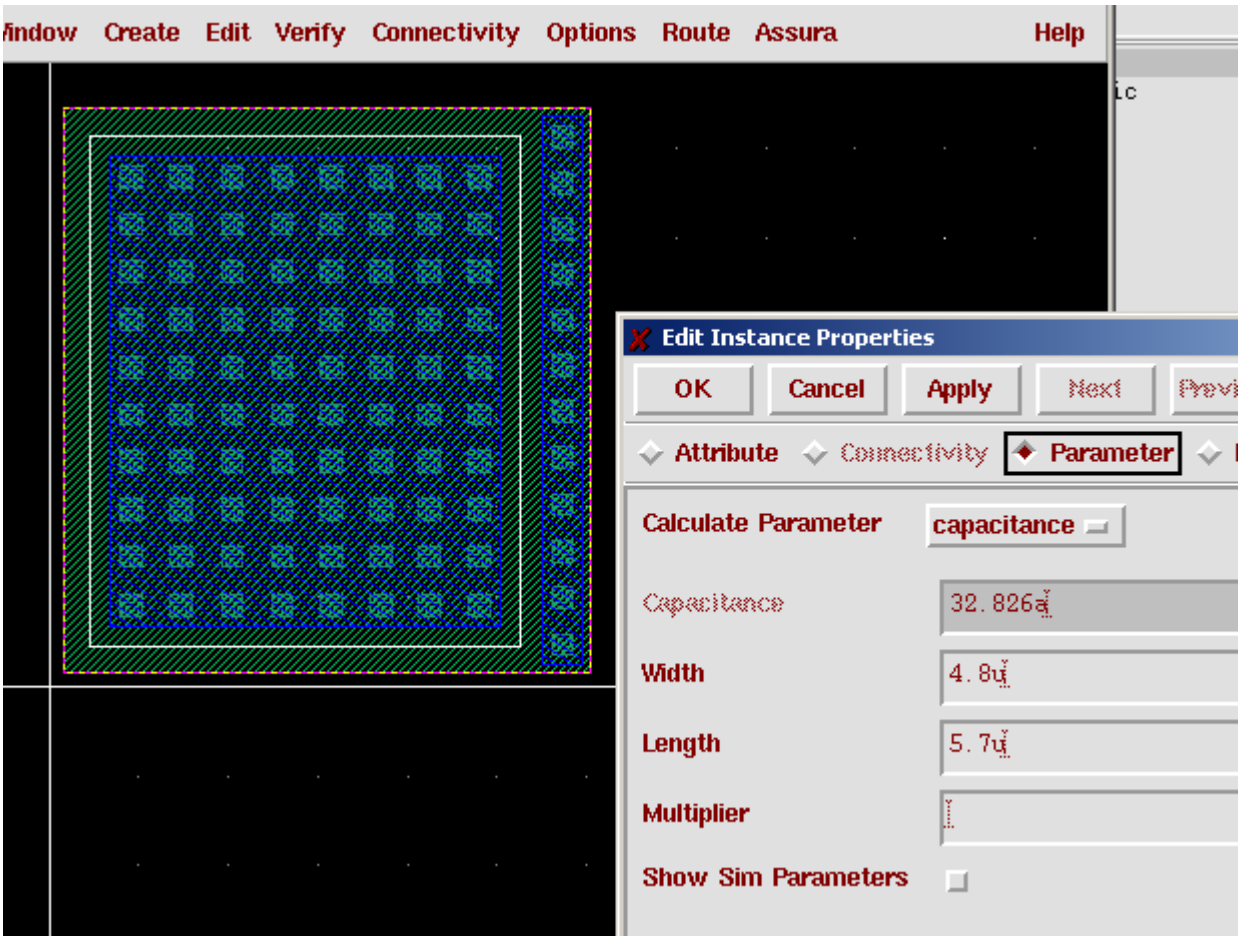
REQ 13.2.1 :
Parallel/Series configuration with metal straps.
REQ 13.2.2 :
Dog bone
REQ 13.2.3 :
VXL ready connectivity
REQ 13.2.4 :
Optional etch guard resistors
REQ 13.2.5 :
Permute properties on all pins



13.3 Capacitor Pcell

REQ 13.3.1 :

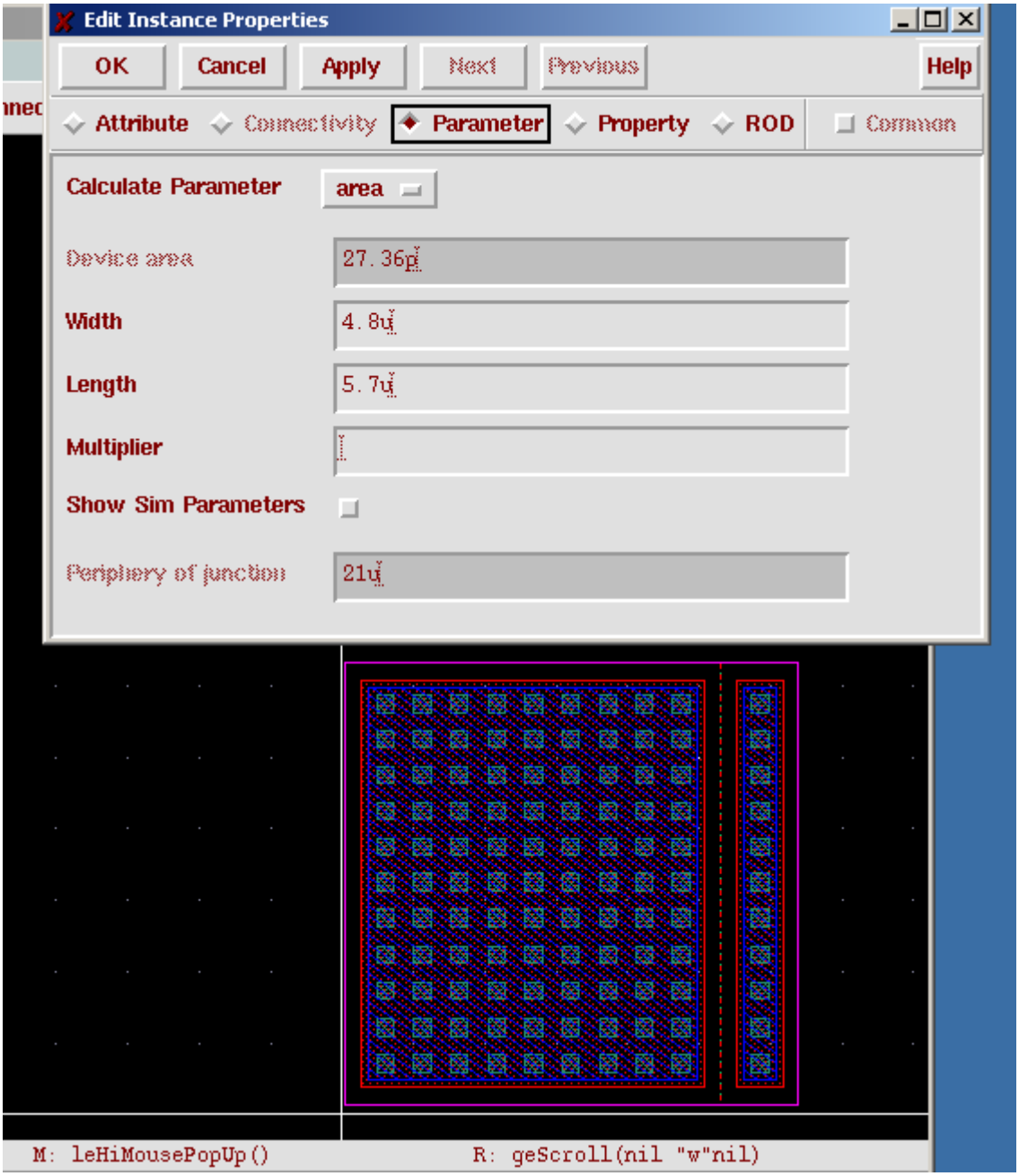
Configurable width, length or capacitance



13.4 Diode Pcell

REQ 13.4.1 :

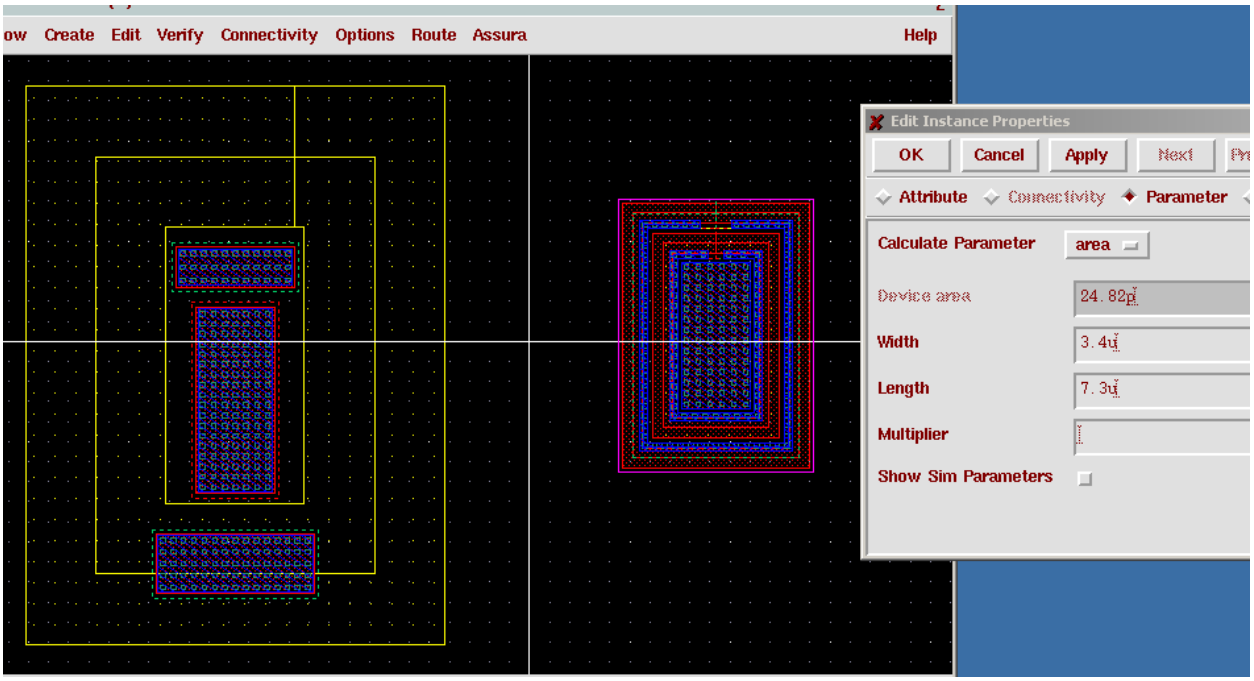
Configurable width, length or area



13.5 Bipolar Pcell

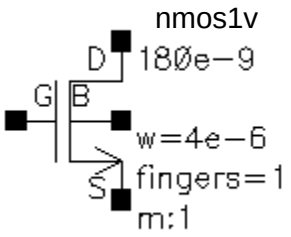
REQ 13.5.1 :

Configurable width, length or area



14 GPDK090 Device Datasheets

14.1 nmos1v datasheet



Spectre Netlist
Spectre Model Name = “gpdk090_nmos1v”

NM1 (D G S B) gpdk090_nmos1v w=4u l=180.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \
pd=5.2u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “nmos1v”

; nmos1v Instance /NM1 = auLvs device M1

d nmos1v D G S B (p D S)

i 1 nmos1v D G S B " m 1.0 l 180e-9 w 4e-6 "

CDL Netlist
CDL Device Name = “nmos1v”

MNM1 D G S B nmos1v W=4u L=180.0n M=1.0

Assura Netlist
Assura auLvs Device Name = “nmos1v”

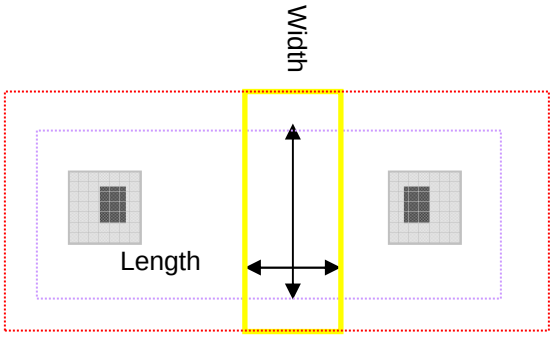
c nmos1v MOS D B G B S B B B ;;

* 4 pins

* 4 nets

S (p D S);

i NM1 nmos1v D G S B ; m 1 l 1.8e-07 w 4e-06 ;



nmos1v – 1.2 volt nominal VT NMOS transistor

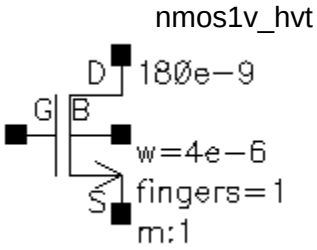
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide AND Nimp CONTAINS Poly
G	Poly
D	Oxide AND Nimp NOT Poly
S	Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

14.2 nmos1v_hvt datasheet

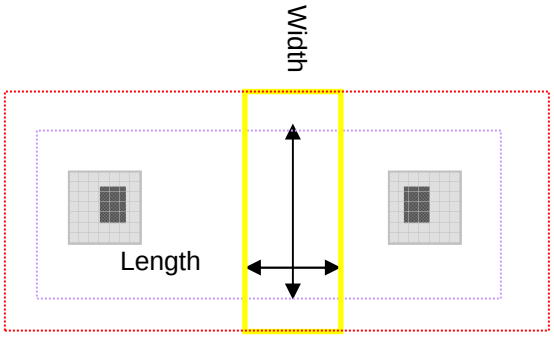


Spectre Netlist
Spectre Model Name = “gpdk090_nmos1v_hvt”
NM1 (D G S B) gpdk090_nmos1v_hvt w=4u l=180.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \ pd=5.2u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “nmos1v_hvt”
; nmos1v_hvt Instance /NM1 = auLvs device M1
d nmos1v_hvt D G S B (p D S)
i 1 nmos1v_hvt D G S B '' m 1.0 l 180e-9 w 4e-6 ''

CDL Netlist
CDL Device Name = “nmos1v_hvt”
MNM1 D G S B nmos1v_hvt W=4u L=180.0n M=1.0

Assura Netlist
Assura auLvs Device Name = “nmos1v_hvt”
c nmos1v_hvt MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i NM1 nmos1v_hvt D G S B ; m 1 l 1.8e-07 w 4e-06 ;



nmos1v_hvt – 1.2 volt high VT NMOS transistor

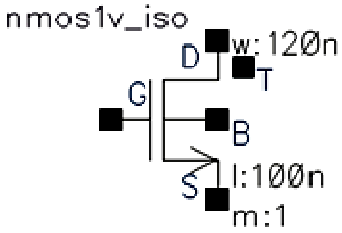
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp & Nhvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide AND Nimp AND Nhvt CONTAINS Poly
G	Poly
D	Oxide AND Nimp AND Nhvt NOT Poly
S	Oxide AND Nimp AND Nhvt NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

14.3 nmos1v_iso datasheet

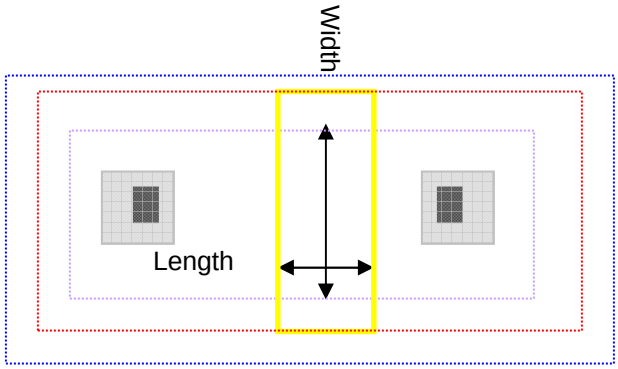


Spectre Netlist
Spectre Model Name = “gpdk090_nmos1v_iso”
NM1 (D G S B T) gpdk090_nmos1v_iso w=4u l=100.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \ pd=5.2u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “nmos1v_iso”
; nmos1v_iso Instance /NM1 = auLvs device M1 d nmos1v_iso D G S B T(p D S) i 1 nmos1v_iso D G S B T " m 1.0 l 100e-9 w 4e-6 "

CDL Netlist
CDL Device Name = “nmos1v_iso”
MNM1 D G S B T nmos1v_iso W=4u L=100.0n M=1.0

Assura Netlist
Assura auLvs Device Name = “nmos1v_iso”
c nmos1v_iso MOS D B G B S B B B T B;; * 5 pins * 5 nets S (p D S); i NM1 nmos1v_iso D G S B T ; m 1 l 1.0e-07 w 4e-06 ;



nmos1v_iso – 1.2 volt nominal VT Isolated NMOS transistor

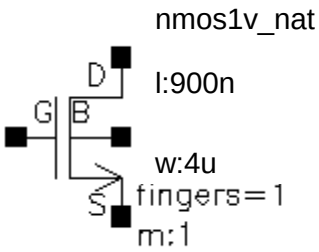
Device Layers	
Layer	**Color and Fill**
Nburied	
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Nburied AND Oxide AND Nimp CONTAINS Poly
G	Poly
D	Nburied AND Oxide AND Nimp NOT Poly
S	Nburied Oxide AND Nimp NOT Poly
B	Isolated Pwell
T	Nburied

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

14.4 nmos1v_nat datasheet



Spectre Netlist
Spectre Model Name = “gpdk090_nmos1v_nat”

NM1 (D G S B) gpdk090_nmos1v_nat w=4u l=900.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \
pd=5.2u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “nmos1v_nat”

; nmos1v_nat Instance /NM1 = auLvs device M1

d nmos1v_nat D G S B (p D S)

i 1 nmos1v_nat D G S B '' m 1.0 l 900e-9 w 4e-6 ''

CDL Netlist
CDL Device Name = “nmos1v_nat”

MNM1 D G S B nmos1v_nat W=4u L=900.0n M=1.0

Assura Netlist
Assura auLvs Device Name = “nmos1v_nat”

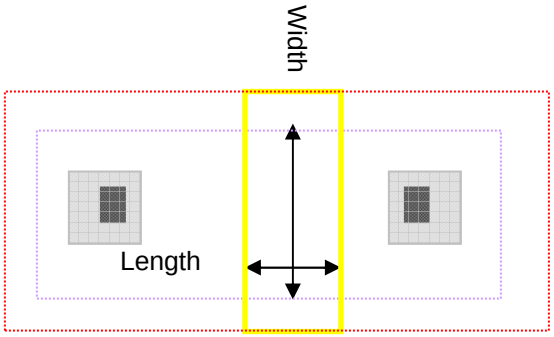
c nmos1v_nat MOS D B G B S B B B ;;

* 4 pins

* 4 nets

S (p D S);

i NM1 nmos1v_nat D G S B ; m 1 l 9.0e-07 w 4e-06 ;



nmos1v_nat – 1.2 volt native VT MOS transistor

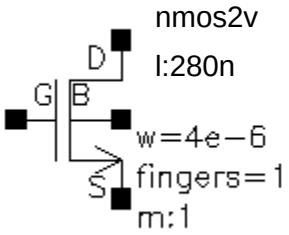
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp & Nzvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide AND Nimp AND Nzvt CONTAINS Poly
G	Poly
D	Oxide AND Nimp AND Nzvt NOT Poly
S	Oxide AND Nimp AND NzvtT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

14.5 nmos2v datasheet

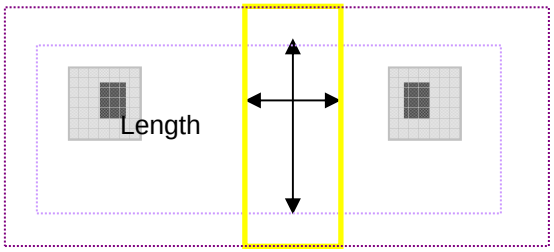


Spectre Netlist
Spectre Model Name = “gpdk090_nmos2v”
NM1 (D G S B) gpdk090_nmos2v w=4u l=280.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \ pd=5.2u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “nmos2v”
; nmos2v Instance /NM1 = auLvs device M1
d nmos2v D G S B (p D S)
i 1 nmos2v D G S B " m 1.0 l 280e-9 w 4e-6 "

CDL Netlist
CDL Device Name = “nmos2v”
MNM1 D G S B nmos2v W=4u L=280.0n M=1.0

Assura Netlist
Assura auLvs Device Name = “nmos2v”
c nmos2v MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i NM1 nmos2v D G S B ; m 1 l 2.8e-07 w 4e-06 ;



nmos2v – 2.5 volt nominal VT NMOS transistor

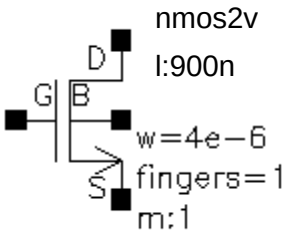
Device Layers	
Layer	**Color and Fill**
Oxide_thk	
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide_thk AND Oxide AND Nimp CONTAINS Poly
G	Poly
D	Oxide_thk AND Oxide AND Nimp NOT Poly
S	Oxide_thk AND Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

14.6 nmos2v_nat datasheet

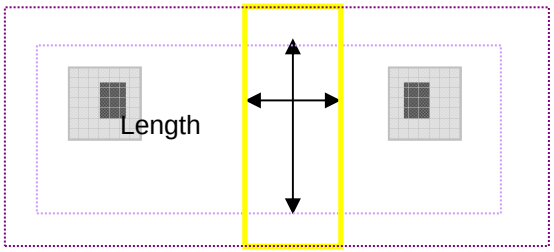


Spectre Netlist
Spectre Model Name = “gpdk090_nmos2v_nat”
NM1 (D G S B) gpdk090_nmos2v_nat w=4u l=900.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \ pd=5.2u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “nmos2v_nat”
; nmos2v_nat Instance /NM1 = auLvs device M1
d nmos2v_nat D G S B (p D S)
i 1 nmos2v_nat D G S B '' m 1.0 l 900e-9 w 4e-6 ''

CDL Netlist
CDL Device Name = “nmos2v_nat”
MNM1 D G S B nmos2v_nat W=4u L=900.0n M=1.0

Assura Netlist
Assura auLvs Device Name = “nmos2v_nat”
c nmos2v_nat MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i NM1 nmos2v_nat D G S B ; m 1 l 9.0e-07 w 4e-06 ;



nmos2v_nat – 2.5 volt Native VT NMOS transistor

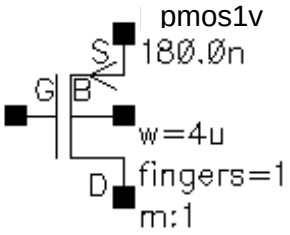
Device Layers	
Layer	**Color and Fill**
Oxide_thk	
Oxide	
Nimp & Nzvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide_thk AND Oxide AND Nimp AND Nzvt CONTAINS Poly
G	Poly
D	Oxide_thk AND Oxide AND Nimp AND Nzvt NOT Poly
S	Oxide_thk AND Oxide AND Nimp AND Nzvt NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

14.7 pmos1v datasheet



Spectre Netlist
Spectre Model Name = “gpdk090_pmos1v”

PM1 (D G S B) gpdk090_pmos1v w=4u l=100.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \
pd=5.2u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “pmos1v”

; pmos1v Instance /PM1 = auLvs device M1

d pmos1v D G S B (p D S)

i 1 pmos1v D G S B " m 1.0 l 100e-9 w 4e-6 "

CDL Netlist
CDL Device Name = “pmos1v”

MPM1 D G S B pmos1v W=4u L=100.0n M=1.0

Assura Netlist
Assura auLvs Device Name = “pmos1v”

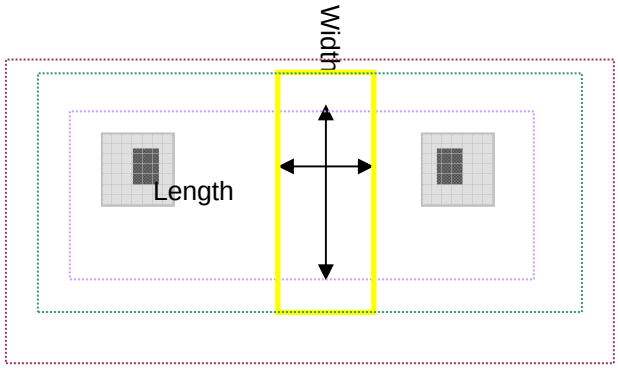
c pmos1v MOS D B G B S B B B ;;

* 4 pins

* 4 nets

S (p D S);

i MP1 pmos1v D G S B ; m 1 l 1.0e-07 w 4e-06 ;



pmos1v – 1.2 volt nominal VT PMOS transistor

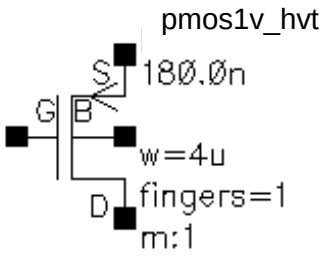
Device Layers	
Layer	**Color and Fill**
Nwell	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Nwell AND Oxide AND Pimp CONTAINS Poly
G	Poly
D	Nwell AND Oxide AND Pimp NOT Poly
S	Nwell AND Oxide AND Pimp NOT Poly
B	Nwell

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

14.8 pmos1v_hvt datasheet

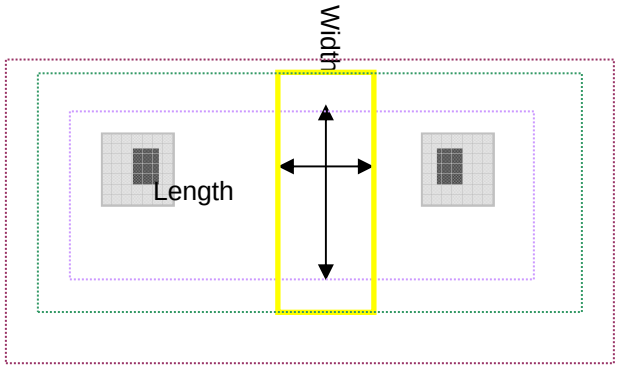


Spectre Netlist
Spectre Model Name = “gpdk090_pmos1v_hvt”
PM1 (D G S B) gpdk090_pmos1v_hvt w=4u l=100.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \ pd=5.2u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “pmos1v_hvt”
; pmos1v_hvt Instance /PM1 = auLvs device M1
d pmos1v_hvt D G S B (p D S)
i 1 pmos1v_hvt D G S B " m 1.0 l 100e-9 w 4e-6 "

CDL Netlist
CDL Device Name = “pmos1v”
MPM1 D G S B pmos1v_hvt W=4u L=100.0n M=1.0

Assura Netlist
Assura auLvs Device Name = “pmos1v”
c pmos1v_hvt MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i MP1 pmos1v_hvt D G S B ; m 1 l 1.0e-07 w 4e-06 ;



pmos1v_hvt – 1.2 volt high VT PMOS transistor

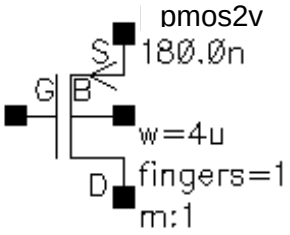
Device Layers	
Layer	**Color and Fill**
Nwell	
Oxide	
Pimp & Phvt	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Nwell AND Oxide AND Pimp AND Phvt CONTAINS Poly
G	Poly
D	Nwell AND Oxide AND Pimp AND Phvt NOT Poly
S	Nwell AND Oxide AND Pimp AND Phvt NOT Poly
B	Nwell

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

14.9 pmos2v datasheet



Spectre Netlist
Spectre Model Name = “gpdk090_pmos2v”

PM1 (D G S B) gpdk090_pmos2v w=4u l=150.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \
pd=5.2u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “pmos2v”

; pmos2v Instance /PM1 = auLvs device M1

d pmos2v D G S B (p D S)

i 1 pmos2v D G S B " m 1.0 l 150e-9 w 4e-6 "

CDL Netlist
CDL Device Name = “pmos2v”

MPM1 D G S B pmos2v W=4u L=150.0n M=1.0

Assura Netlist
Assura auLvs Device Name = “pmos2v”

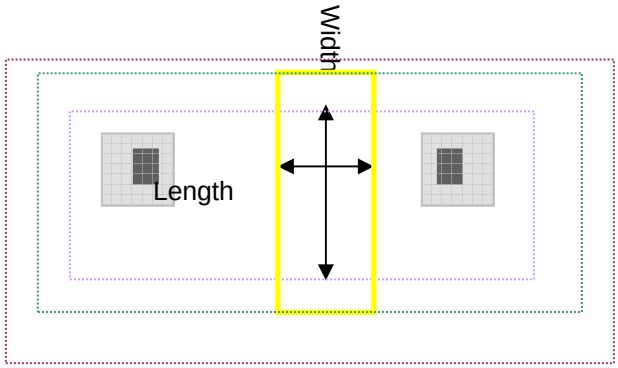
c pmos2v MOS D B G B S B B B ;;

* 4 pins

* 4 nets

S (p D S);

i MP1 pmos2v D G S B ; m 1 l 1.5e-07 w 4e-06 ;



pmos2v – 2.5 volt nominal VT PMOS transistor

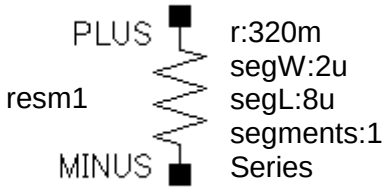
Device Layers	
Layer	**Color and Fill**
Nwell	
Oxide & Oxide_thk	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Nwell AND Oxide AND Oxide_thk AND Pimp CONTAINS Poly
G	Poly
D	Nwell AND Oxide AND Oxide_thk AND Pimp NOT Poly
S	Nwell AND Oxide AND Oxide_thk AND Pimp NOT Poly
B	Nwell

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* S and D are PERMUTABLE

14.10 resm1-resm9 datasheet



Spectre Netlist
Spectre Model Name = "gpdk090_resm1"
R1 (MINUS PLUS) resm1_pcell1 segL=8u segW=2u
Subckt resm1_pcell1 MINUS PLUS
Parameters segL=8u segW=2u
R0 (PLUS MINUS) gpdk090_resm1 l=segL w=segW
Ends resm1_pcell1

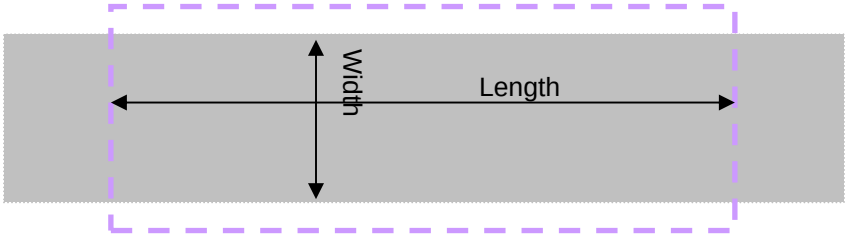
DIVA LVS Netlist
DIVA Device Name = "resm1"
; resm1 Instance /R1 = auLvs device R1
d resm1 PLUS MINUS (p PLUS MINUS)
i 1 resm1 PLUS MINUS " r 320e-3 w 2e-6 l 8e-6"

CDL Netlist
CDL Device Name = "resm1"
RR1 PLUS MINUS $[resm1] r=320m w=2u l=8u

Assura Netlist
Assura auLvs Device Name = " resm1 "
c resm1 RES PLUS B MINUS B ;;
* 2 pins
* 2 nets
S (p PLUS MINUS) ;
i R1 resm1 PLUS MINUS ; r 0.32 w 2e-06 l=8e-06;

* The same format is used for resm2-resm9 as is used with resm1

* Only the metal sheet rho and device name changes



resm1 – N+ diffused resistor without salicide

Device Layers	
Layer	**Color and Fill**
M1Resdum (Marker Layer)	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Metal1 AND M1Resdum
PLUS	Metal1 TOUCHING M1Resdum
MINUS	Metal1 TOUCHING M1Resdum

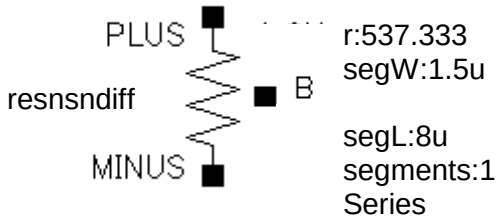
LVS Comparison	
Parameter	**Calculation**
Length	Metal1 AND M1Resdum Length (illustrated above)
Width	Metal1 AND M1Resdum Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

* The same format is used for Resm2-resm9 as is used with resm1

* Only the metal layer and recognition layer changes

14.11 resnsndiff datasheet

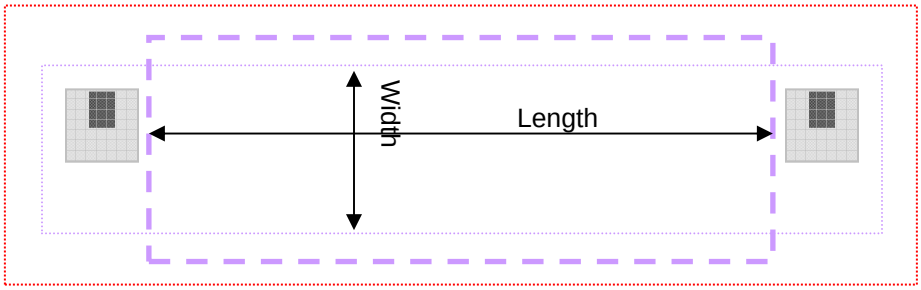


Spectre Netlist
Spectre Model Name = “gpdk090_resm1”
R1 (B MINUS PLUS) resnsndiff_pcell1 segL=8u segW=1.5u
Subckt resnsndiff_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_resnsndiff l=segL w=segW
Ends resnsndiff_pcell1

DIVA LVS Netlist
DIVA Device Name = “resnsndiff”
; resnsndiff Instance /R1 = auLvs device R1
d resnsndiff PLUS MINUS B (p PLUS MINUS)
i 1 resnsndiff PLUS MINUS B " r 537.333 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = “resnsndiff”
RR1 PLUS MINUS B $[resnsndiff] r=537.333 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = “ resnsndiff ”
c resnsndiff RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 resnsndiff PLUS MINUS B ; r 537.333 w 1.5e-06 l=8e-06;



resnsndiff – N+ diffused resistor without salicide

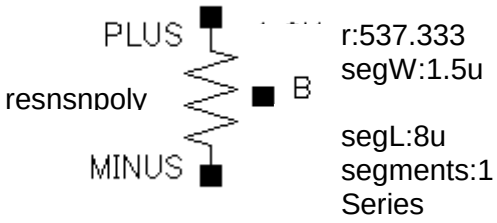
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp	
SiProt & Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide AND Nimp AND SiProt AND Resdum
PLUS	Oxide AND Nimp NOT Resdum
MINUS	Oxide AND Nimp NOT Resdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	SiProt Length (illustrated above)
Width	Oxide Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.12 resnsnpoly datasheet

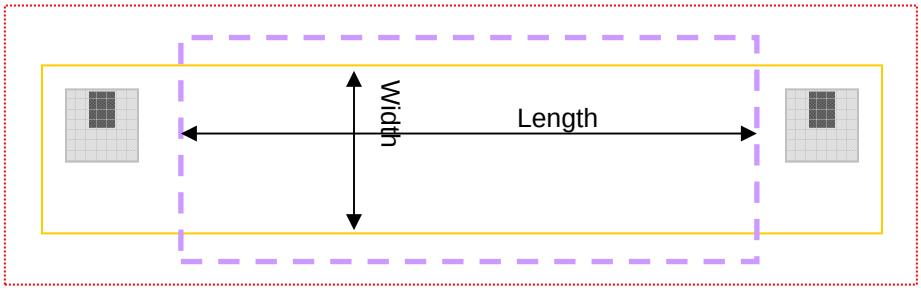


Spectre Netlist
Spectre Model Name = "gpdk090_resnspoly"
R1 (B MINUS PLUS) resnsnpoly_pcell1 segL=8u segW=1.5u
Subckt resnsnpoly_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_resnsnpoly l=segL w=segW
Ends resnsnpoly_pcell1

DIVA LVS Netlist
DIVA Device Name = "resnsnpoly"
; resnsnpoly Instance /R1 = auLvs device R1
d resnsnpoly PLUS MINUS B (p PLUS MINUS)
i 1 resnsnpoly PLUS MINUS B " r 537.333 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = "resnsnpoly"
RR1 PLUS MINUS B $[resnsnpoly] r=537.333 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = " resnsnpoly "
c resnsnpoly RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 resnsnpoly PLUS MINUS B ; r 537.333 w 1.5e-06 l=8e-06;



resnsnpoly – N+ poly resistor without salicide

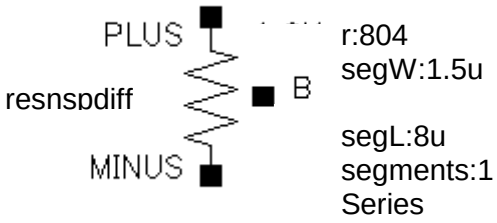
Device Layers	
Layer	**Color and Fill**
Poly	
Nimp	
SiProt & Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Poly AND Nimp AND SiProt AND Resdum
PLUS	Poly AND Nimp NOT Resdum
MINUS	Poly AND Nimp NOT Resdum

LVS Comparison	
Parameter	**Calculation**
Length	SiProt Length (illustrated above)
Width	Poly Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.13 resnspdiff datasheet

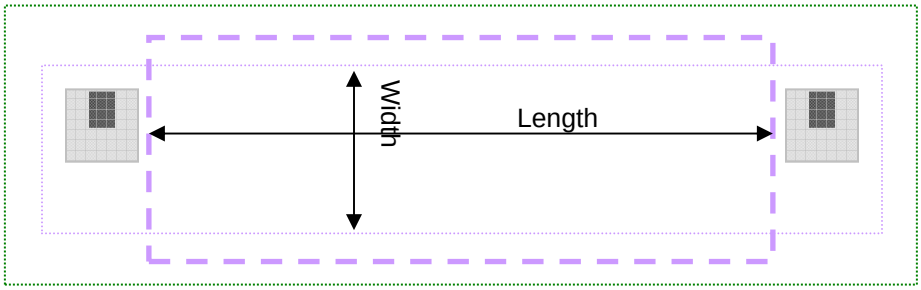


Spectre Netlist
Spectre Model Name = “gpdk090_resm1”
R1 (B MINUS PLUS) resnspdiff_pcell1 segL=8u segW=1.5u
Subckt resnspdiff_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_resnspdiff l=segL w=segW
Ends resnspdiff_pcell1

DIVA LVS Netlist
DIVA Device Name = “resnspdiff”
; resnspdiff Instance /R1 = auLvs device R1
d resnspdiff PLUS MINUS B (p PLUS MINUS)
i 1 resnspdiff PLUS MINUS B " r 804 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = “resnspdiff”
RR1 PLUS MINUS B $[resnspdiff] r=804 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = “ resnspdiff ”
c resnspdiff RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 resnspdiff PLUS MINUS B ; r 804 w 1.5e-06 l=8e-06;



resnspdiff – N+ diffused resistor without salicide

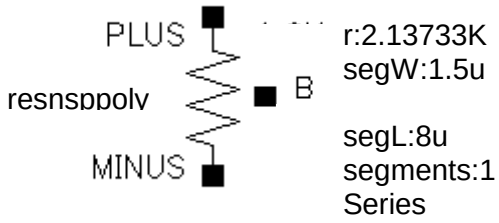
Device Layers	
Layer	**Color and Fill**
Oxide	
Pimp	
SiProt & Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide AND Pimp AND SiProt AND Resdum
PLUS	Oxide AND Pimp NOT Resdum
MINUS	Oxide AND Pimp NOT Resdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	SiProt Length (illustrated above)
Width	Oxide Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.14 resnsppoly datasheet

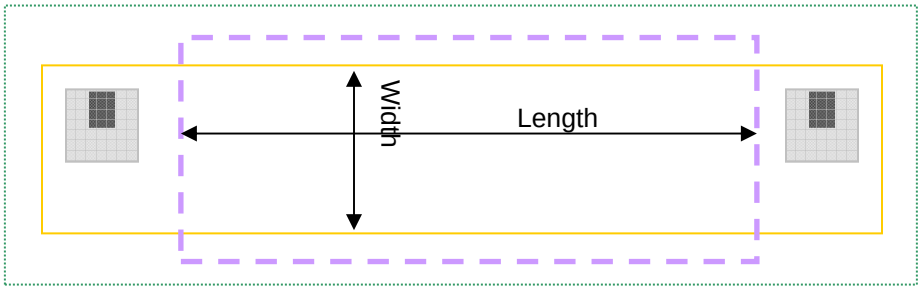


Spectre Netlist
Spectre Model Name = "gpdk090_resnspoly"
R1 (B MINUS PLUS) resnsppoly_pcell1 segL=8u segW=1.5u
Subckt resnsppoly_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_resnsppoly l=segL w=segW
Ends resnsppoly_pcell1

DIVA LVS Netlist
DIVA Device Name = "resnsppoly"
; resnsppoly Instance /R1 = auLvs device R1
d resnsppoly PLUS MINUS B (p PLUS MINUS)
i 1 resnsppoly PLUS MINUS B " r 2137.33 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = "resnsppoly"
RR1 PLUS MINUS B $[resnsppoly] r=2137.33 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = " resnsppoly "
c resnsppoly RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 resnsppoly PLUS MINUS B ; r 2137.33 w 1.5e-06 l=8e-06;



resnsppoly – N+ poly resistor without salicide

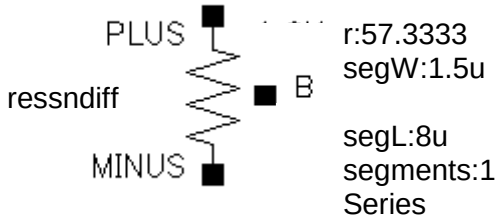
Device Layers	
Layer	**Color and Fill**
Poly	
Pimp	
SiProt & Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Poly AND Pimp AND SiProt AND Resdum
PLUS	Poly AND Pimp NOT Resdum
MINUS	Poly AND Pimp NOT Resdum

LVS Comparison	
Parameter	**Calculation**
Length	SiProt Length (illustrated above)
Width	Poly Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.15 ressndiff datasheet

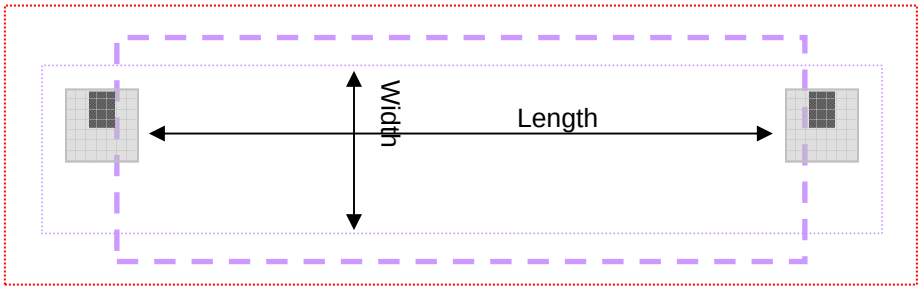


Spectre Netlist
Spectre Model Name = "gpdk090_resm1"
R1 (B MINUS PLUS) ressndiff_pcell1 segL=8u segW=1.5u
Subckt ressndiff_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_ressndiff l=segL w=segW
Ends ressndiff_pcell1

DIVA LVS Netlist
DIVA Device Name = "ressndiff"
; ressndiff Instance /R1 = auLvs device R1
d ressndiff PLUS MINUS B (p PLUS MINUS)
i 1 ressndiff PLUS MINUS B " r 57.3333 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = "ressndiff"
RR1 PLUS MINUS B $[ressndiff] r=57.3333 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = " ressndiff "
c ressndiff RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 ressndiff PLUS MINUS B ; r 57.3333 w 1.5e-06 l=8e-06;



ressndiff – N+ diffused resistor with salicide

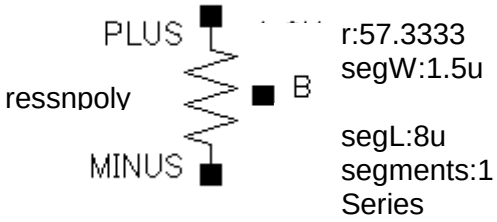
Device Layers	
Layer	**Color and Fill**
Oxide	
Nimp	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide AND Nimp AND Resdum NOT SiProt
PLUS	Oxide AND Nimp NOT Resdum
MINUS	Oxide AND Nimp NOT Resdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Resdum Length (illustrated above)
Width	Oxide Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.16 ressnpoly datasheet

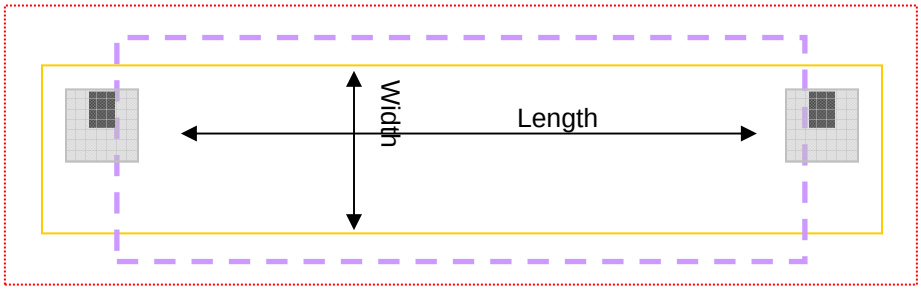


Spectre Netlist
Spectre Model Name = "gpdk090_resnspoly"
R1 (B MINUS PLUS) ressnpoly_pcell1 segL=8u segW=1.5u
Subckt ressnpoly_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_ressnpoly l=segL w=segW
Ends ressnpoly_pcell1

DIVA LVS Netlist
DIVA Device Name = "ressnpoly"
; ressnpoly Instance /R1 = auLvs device R1
d ressnpoly PLUS MINUS B (p PLUS MINUS)
i 1 ressnpoly PLUS MINUS B " r 57.3333 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = "ressnpoly"
RR1 PLUS MINUS B $[ressnpoly] r=57.3333 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = " ressnpoly "
c ressnpoly RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 ressnpoly PLUS MINUS B ; r 57.3333 w 1.5e-06 l=8e-06;



ressnpoly – N+ poly resistor with salicide

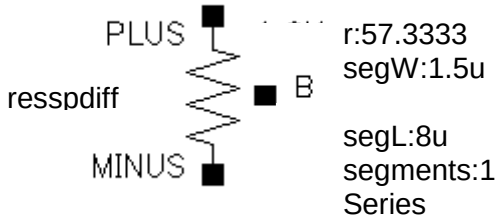
Device Layers	
Layer	**Color and Fill**
Poly	
Nimp	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Poly AND Nimp AND Resdum NOT SiProt
PLUS	Poly AND Nimp NOT Resdum
MINUS	Poly AND Nimp NOT Resdum

LVS Comparison	
Parameter	**Calculation**
Length	Resdum Length (illustrated above)
Width	Poly Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.17 resspdiff datasheet

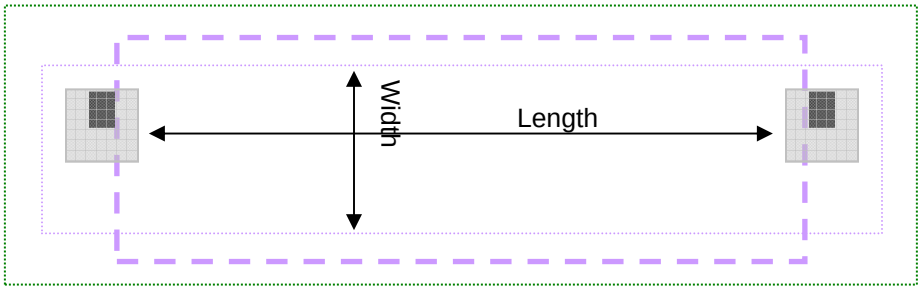


Spectre Netlist
Spectre Model Name = "gpdk090_resm1"
R1 (B MINUS PLUS) resspdiff_pcell1 segL=8u segW=1.5u
Subckt resspdiff_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_resspdiff l=segL w=segW
Ends resspdiff_pcell1

DIVA LVS Netlist
DIVA Device Name = "resspdiff"
; resspdiff Instance /R1 = auLvs device R1
d resspdiff PLUS MINUS B (p PLUS MINUS)
i 1 resspdiff PLUS MINUS B " r 57.3333 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = "resspdiff"
RR1 PLUS MINUS B $[resspdiff] r=57.3333 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = " resspdiff "
c resspdiff RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 resspdiff PLUS MINUS B ; r 57.3333 w 1.5e-06 l=8e-06;



resspdiff – N+ diffused resistor with salicide

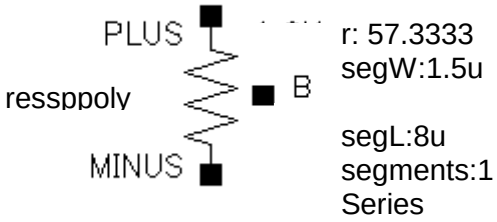
Device Layers	
Layer	**Color and Fill**
Oxide	
Pimp	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide AND Pimp AND Resdum NOT SiProt
PLUS	Oxide AND Pimp NOT Resdum
MINUS	Oxide AND Pimp NOT Resdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Resdum Length (illustrated above)
Width	Oxide Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.18 ressppoly datasheet

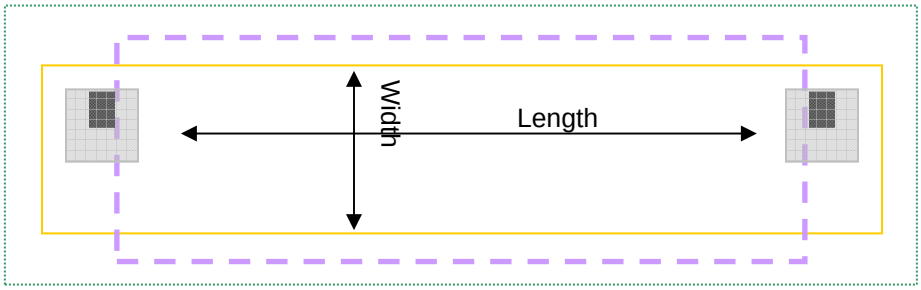


Spectre Netlist
Spectre Model Name = "gpdk090_resspoly"
R1 (B MINUS PLUS) ressppoly_pcell1 segL=8u segW=1.5u
Subckt ressppoly_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_ressppoly l=segL w=segW
Ends ressppoly_pcell1

DIVA LVS Netlist
DIVA Device Name = "ressppoly"
; ressppoly Instance /R1 = auLvs device R1
d ressppoly PLUS MINUS B (p PLUS MINUS)
i 1 ressppoly PLUS MINUS B " r 57.3333 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = "ressppoly"
RR1 PLUS MINUS B $[ressppoly] r=57.3333 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = " ressppoly "
c ressppoly RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 ressppoly PLUS MINUS B ; r 57.3333 w 1.5e-06 l=8e-06;



ressppoly – N+ poly resistor with salicide

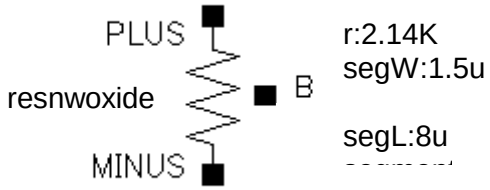
Device Layers	
Layer	**Color and Fill**
Poly	
Pimp	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Poly AND Pimp AND Resdum NOT SiProt
PLUS	Poly AND Pimp NOT Resdum
MINUS	Poly AND Pimp NOT Resdum

LVS Comparison	
Parameter	**Calculation**
Length	Resdum Length (illustrated above)
Width	Poly Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.19 resnwoxide datasheet

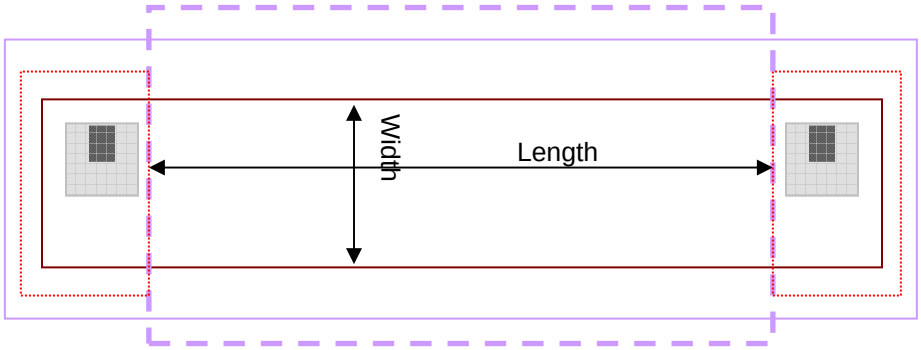


Spectre Netlist
Spectre Model Name = “gpdk090_resm1”
R1 (B MINUS PLUS) resnwoxide_pcell1 segL=8u segW=1.5u
Subckt resnwoxide_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_resnwoxide l=segL w=segW
Ends resnwoxide_pcell1

DIVA LVS Netlist
DIVA Device Name = “resnwoxide”
; resnwoxide Instance /R1 = auLvs device R1
d resnwoxide PLUS MINUS B (p PLUS MINUS)
i 1 resnwoxide PLUS MINUS B " r 2140 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = “resnwoxide”
RR1 PLUS MINUS B $[resnwoxide] r=2140 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = “ resnwoxide ”
c resnwoxide RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 resnwoxide PLUS MINUS B ; r 2140 w 1.5e-06 l=8e-06;



resnwoxide – N+ diffused resistor without salicide

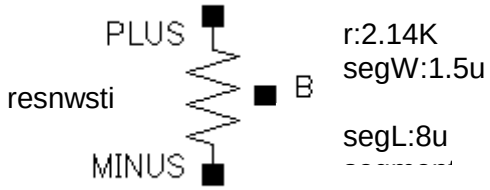
Device Layers	
Layer	**Color and Fill**
Oxide	
Nwell	
Nimp	
ResWdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Oxide AND Nwell AND SiProt AND ResWdum
PLUS	Oxide AND Nwell NOT ResWdum
MINUS	Oxide AND Nwell NOT ResWdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	ResWdum Length (illustrated above)
Width	Nwell Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.20 resnwsti datasheet

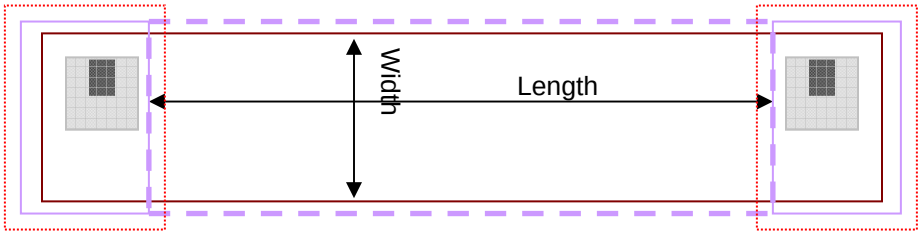


Spectre Netlist
Spectre Model Name = “gpdk090_resm1”
R1 (B MINUS PLUS) resnwsti_pcell1 segL=8u segW=1.5u
Subckt resnwsti_pcell1 B MINUS PLUS
Parameters segL=8u segW=1.5u
R0 (PLUS MINUS B) gpdk090_resnwsti l=segL w=segW
Ends resnwsti_pcell1

DIVA LVS Netlist
DIVA Device Name = “resnwsti”
; resnwsti Instance /R1 = auLvs device R1
d resnwsti PLUS MINUS B (p PLUS MINUS)
i 1 resnwsti PLUS MINUS B " r 2140 w 1.5e-6 l 8e-6"

CDL Netlist
CDL Device Name = “resnwsti”
RR1 PLUS MINUS B $[resnwsti] r=2140 w=1.5u l=8u

Assura Netlist
Assura auLvs Device Name = “ resnwsti ”
c resnwsti RES PLUS B MINUS B B I ;;
* 3 pins
* 3 nets
S (p PLUS MINUS) ;
i R1 resnwsti PLUS MINUS B ; r 2140 w 1.5e-06 l=8e-06;



resnwsti – N+ diffused resistor without salicide

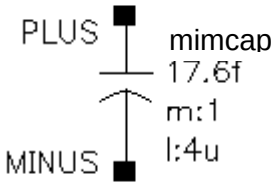
Device Layers	
Layer	**Color and Fill**
Oxide	
Nwell	
Nimp	
ResWdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Nwell AND ResWdum
PLUS	Nwell NOT ResWdum
MINUS	Nwell NOT ResWdum
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	ResWdum Length (illustrated above)
Width	Nwell Width (illustrated above)
Resistance	sheet resistance * Length / Width

* PLUS and MINUS are PERMUTABLE

14.21 mimcap datasheet

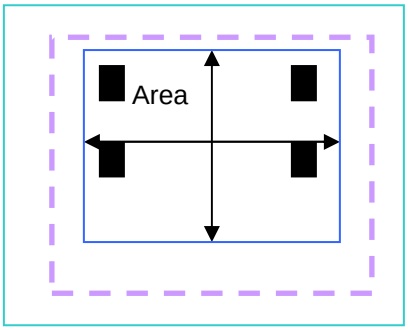


Spectre Netlist
Spectre Model Name = “gpdk090_mimcap”
C1 (PLUS MINUS) gpdk090_mimcap area=16e-12 perim=16e-6 m=1

DIVA LVS Netlist
DIVA Device Name = “mimcap”
; mimcap Instance /C1 = auLvs device C1
d mimcap PLUS MINUS (p PLUS MINUS)
i 1 mimcap PLUS MINUS " area 16e-12 m 1.0 "

CDL Netlist
CDL Device Name = “mimcap”
CC1 PLUS MINUS 16e-12 $[mimcap] m=1

Assura Netlist
Assura auLvs Device Name = “mimcap”
c mimcap CAP PLUS B MINUS B ;;
* 2 pins
* 2 nets
S (p PLUS MINUS)
i C1 mimcap PLUS MINUS ; area 16e-12 m 1 ;



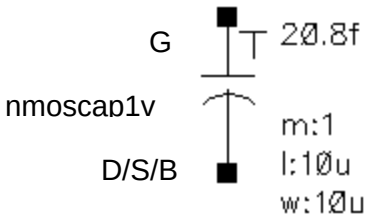
mimcap – Metal / Metal capacitor

Device Layers	
Layer	**Color and Fill**
Metal 2	
CapMetal	
Via2	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	CapMetal AND Metal2
PLUS	CapMetal
MINUS	Metal2 UNDER CapMetal

LVS Comparison	
Parameter	**Calculation**
Area	Area of CapMetal (illustrated above)
Perimeter	Perimeter of CapMetal

14.22 nmoscap1v datasheet

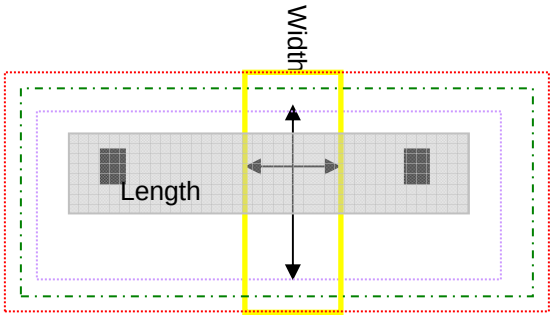


Spectre Netlist
Spectre Model Name = "gpdk090_nmoscap1v"
M1 (D G S B) gpdk090_nmoscap1v w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = "nmoscap1v"
; nmoscap1v Instance /M1 = auLvs device M1
d nmoscap1v D G S B (p D S)
i 1 nmoscap1v D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = "nmoscap1v"
MM1 D G S B nmoscap1v W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = "nmoscap1v"
c nmoscap1v MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i M1 nmoscap1v D G S B ; m 1 l 1e-05 w 1e-05 ;



nmoscap1v – 1.2 volt NMOS capacitor

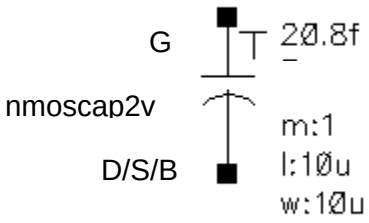
Device Layers	
Layer	**Color and Fill**
Capdum	
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Capdum AND Oxide AND Nimp CONTAINS Poly
TOP	Poly
BOT	Capdum AND Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* Nmos Source, Drain, and Body are Shorted Together

14.23 nmoscap2v datasheet



Spectre Netlist
Spectre Model Name = "gpdk090_nmoscap2v"

M1 (D G S B) gpdk090_nmoscap2v w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = "nmoscap2v"

; nmoscap2v Instance /M1 = auLvs device M1

d nmoscap2v D G S B (p D S)

i 1 nmoscap2v D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = "nmoscap2v"

MM1 D G S B nmoscap2v W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = "nmoscap2v"

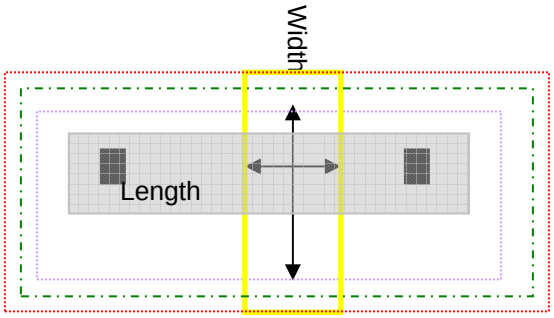
c nmoscap2v MOS D B G B S B B B ;;

* 4 pins

* 4 nets

S (p D S);

i M1 nmoscap2v D G S B ; m 1 l 1e-05 w 1e-05 ;



nmoscap2v – 2.5 volt NMOS capacitor

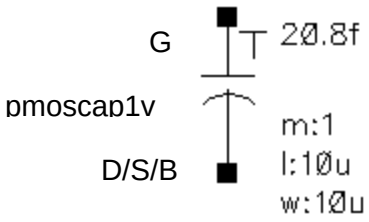
Device Layers	
Layer	**Color and Fill**
Capdum	
Oxide & Oxide_thk	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Capdum AND Oxide AND Oxide_thk AND Nimp CONTAINS Poly
TOP	Poly
BOT	Capdum AND Oxide AND Oxide_thk AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* Nmos Source, Drain, and Body are Shorted Together

14.24 pmoscap1v datasheet

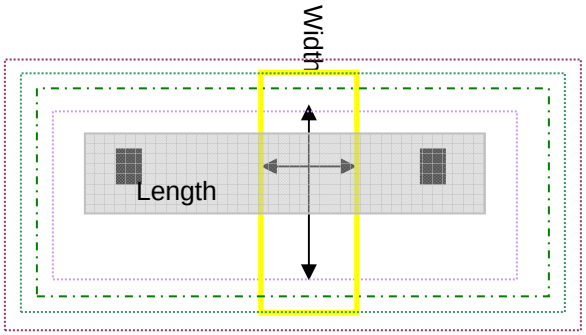


Spectre Netlist
Spectre Model Name = "gpdk090_pmoscap1v"
M1 (D G S B) gpdk090_pmoscap1v w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = "pmoscap1v"
; pmoscap1v Instance /M1 = auLvs device M1
d pmoscap1v D G S B (p D S)
i 1 pmoscap1v D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = "pmoscap1v"
MM1 D G S B pmoscap1v W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = "pmoscap1v"
c pmoscap1v MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i M1 pmoscap1v D G S B ; m 1 l 1e-05 w 1e-05 ;



pmoscap1v – 1.2 volt PMOS capacitor

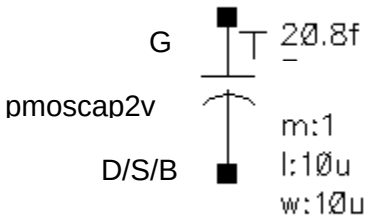
Device Layers	
Layer	**Color and Fill**
Nwell	
Capdum	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Capdum AND Oxide AND Pimp AND Nwell CONTAINS Poly
TOP	Poly
BOT	Capdum AND Oxide AND Pimp AND Nwell NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* Pmos Source, Drain, and Body are Shorted Together

14.25 pmoscap2v datasheet



Spectre Netlist
Spectre Model Name = “gpdk090_pmoscap2v”

M1 (D G S B) gpdk090_pmoscap2v w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = “pmoscap2v”

; pmoscap2v Instance /M1 = auLvs device M1

d pmoscap2v D G S B (p D S)

i 1 pmoscap2v D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = “pmoscap2v”

MM1 D G S B pmoscap2v W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = “pmoscap2v”

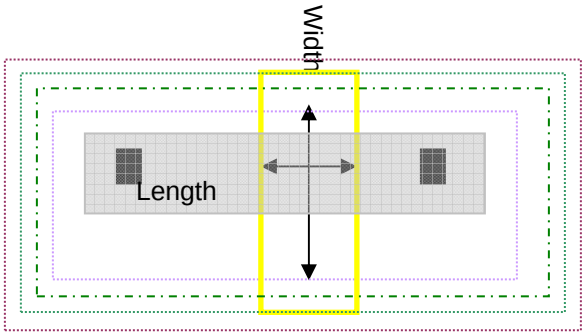
c pmoscap2v MOS D B G B S B B B ;;

* 4 pins

* 4 nets

S (p D S);

i M1 pmoscap2v D G S B ; m 1 l 1e-05 w 1e-05 ;



pmoscap2v – 2.5 volt PMOS capacitor

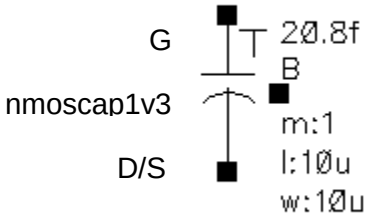
Device Layers	
Layer	**Color and Fill**
Nwell	
Capdum	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Capdum AND Oxide AND Pimp AND Nwell CONTAINS Poly
TOP	Poly
BOT	Capdum AND Oxide AND Pimp AND Nwell NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* Pmos Source, Drain, and Body are Shorted Together

14.26 nmoscap1v3 datasheet

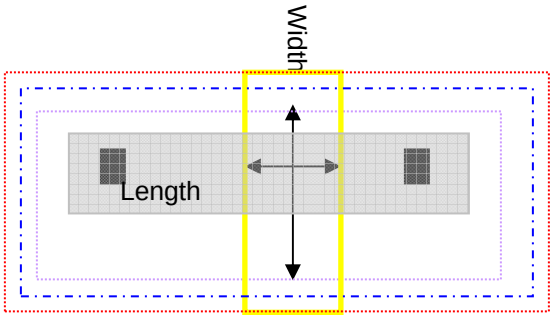


Spectre Netlist
Spectre Model Name = "gpdk090_nmoscap1v"
M1 (D G S B) gpdk090_nmoscap1v w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = "nmoscap1v3"
; nmoscap1v3 Instance /M1 = auLvs device M1
d nmoscap1v3 D G S B (p D S)
i 1 nmoscap1v3 D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = "nmoscap1v3"
MM1 D G S B nmoscap1v3 W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = "nmoscap1v3"
c nmoscap1v3 MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i M1 nmoscap1v3 D G S B ; m 1 l 1e-05 w 1e-05 ;



nmoscap1v3 – 1.2 volt NMOS capacitor

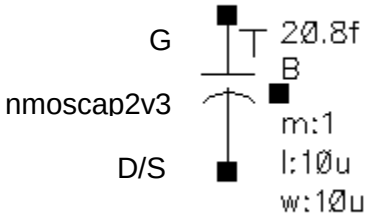
Device Layers	
Layer	**Color and Fill**
Cap3dum	
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Cap3dum AND Oxide AND Nimp CONTAINS Poly
TOP	Poly
BOT	Cap3dum AND Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* Nmos Source, Drain, and Body are Shorted Together

14.27 nmoscap2v3 datasheet



Spectre Netlist
Spectre Model Name = "gpdk090_nmoscap2v"

M1 (D G S B) gpdk090_nmoscap2v w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = "nmoscap2v3"

; nmoscap2v3 Instance /M1 = auLvs device M1

d nmoscap2v3 D G S B (p D S)

i 1 nmoscap2v3 D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = "nmoscap2v3"

MM1 D G S B nmoscap2v3 W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = "nmoscap2v3"

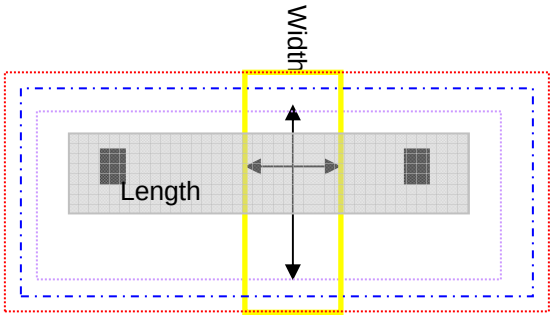
c nmoscap2v3 MOS D B G B S B B B ;;

* 4 pins

* 4 nets

S (p D S);

i M1 nmoscap2v3 D G S B ; m 1 l 1e-05 w 1e-05 ;



nmoscap2v3 – 2.5 volt NMOS capacitor

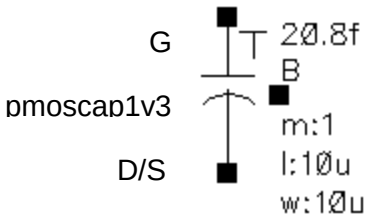
Device Layers	
Layer	**Color and Fill**
Cap3dum	
Oxide & Oxide_thk	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Cap3dum AND Oxide AND Oxide_thk AND Nimp CONTAINS Poly
TOP	Poly
BOT	Cap3dumM AND Oxide AND Oxide_thk AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* Nmos Source, Drain, and Body are Shorted Together

14.28 pmoscap1v3 datasheet

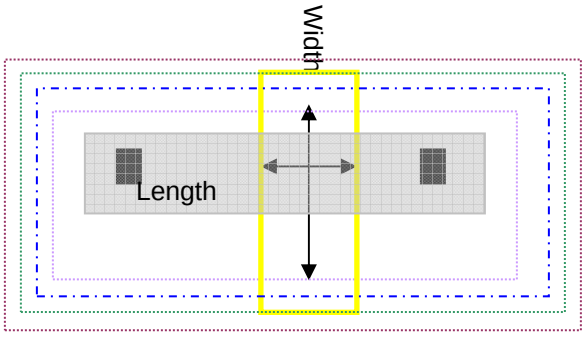


Spectre Netlist
Spectre Model Name = "gpdk090_pmoscap1v"
M1 (D G S B) gpdk090_pmoscap1v w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = "pmoscap1v3"
; pmoscap1v3 Instance /M1 = auLvs device M1
d pmoscap1v3 D G S B (p D S)
i 1 pmoscap1v3 D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = "pmoscap1v3"
MM1 D G S B pmoscap1v3 W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = "pmoscap1v3"
c pmoscap1v3 MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i M1 pmoscap1v3 D G S B ; m 1 l 1e-05 w 1e-05 ;



pmoscap1v3 – 1.2 volt PMOS capacitor

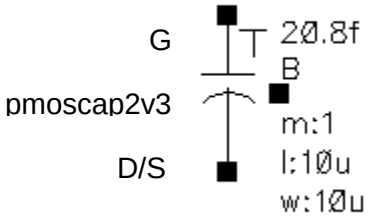
Device Layers	
Layer	**Color and Fill**
Nwell	
Cap3dum	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Cap3dum AND Oxide AND Pimp AND Nwell CONTAINS Poly
TOP	Poly
BOT	Cap3dum AND Oxide AND Pimp AND Nwell NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* Pmos Source, Drain, and Body are Shorted Together

14.29 pmoscap2v3 datasheet

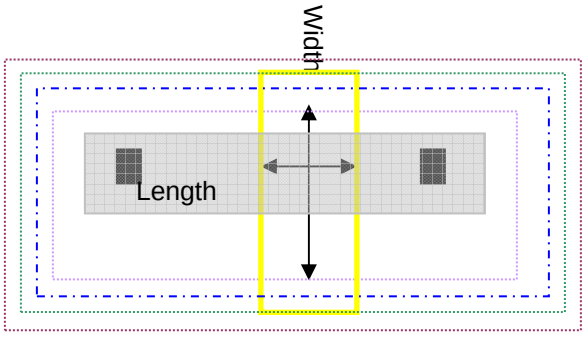


Spectre Netlist
Spectre Model Name = "gpdk090_pmoscap2v"
M1 (D G S B) gpdk090_pmoscap2v w=10u l=10u m=(1)*(1)

DIVA LVS Netlist
DIVA Device Name = "pmoscap2v3"
; pmoscap2v3 Instance /M1 = auLvs device M1
d pmoscap2v3 D G S B (p D S)
i 1 pmoscap2v3 D G S B " m 1.0 l 10e-6 w 10e-6 "

CDL Netlist
CDL Device Name = "pmoscap2v3"
MM1 D G S B pmoscap2v3 W=10u L=10u M=1

Assura Netlist
Assura auLvs Device Name = "pmoscap2v3"
c pmoscap2v3 MOS D B G B S B B B ;;
* 4 pins
* 4 nets
S (p D S);
i M1 pmoscap2v3 D G S B ; m 1 l 1e-05 w 1e-05 ;



pmoscap2v3 – 2.5 volt PMOS capacitor

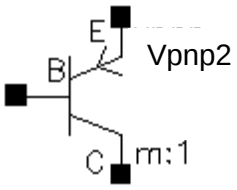
Device Layers	
Layer	**Color and Fill**
Nwell	
Cap3dum	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	Cap3dum AND Oxide AND Pimp AND Nwell CONTAINS Poly
TOP	Poly
BOT	Cap3dum AND Oxide AND Pimp AND Nwell NOT Poly
B	Substrate

LVS Comparison	
Parameter	**Calculation**
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

* Pmos Source, Drain, and Body are Shorted Together

14.30 vpnp2 datasheet

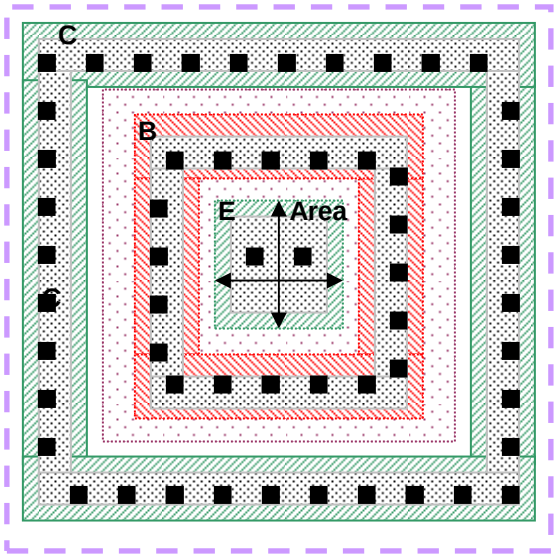


Spectre Netlist
Spectre Model Name = “gpdk090_vpnp2”
Q0 (C B E) gpdk090_vpnp2 area=4 m=1

DIVA LVS Netlist
DIVA Device Name = “vpnp2”
; vpnp2 Instance /Q0 = auLvs device Q0
d vpnp C B E
i 0 vpnp2 C B E " area 4.0 m 1.0 "

CDL Netlist
CDL Device Name = “vpnp2”
QQ0 C B E vpnp2 M=1 area=4.0

Assura Netlist
Assura auLvs Device Name = “vpnp2”
c vpnp2 BJT C B B B E B ;;
* 3 pins
* 3 nets
i Q0 vpnp2 C B E; area 4 m 1 ;



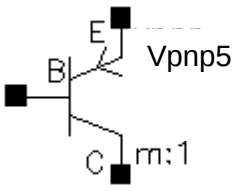
vpnp2 – 1.2 volt vertical substrate PNP with 2x2 fixed emitter

Device Layers	
Layer	**Color and Fill**
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	BJTdummy contains Nimp AND Pimp
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
Area	Area of Emitter (illustrated above)

14.31 vpnp5 datasheet

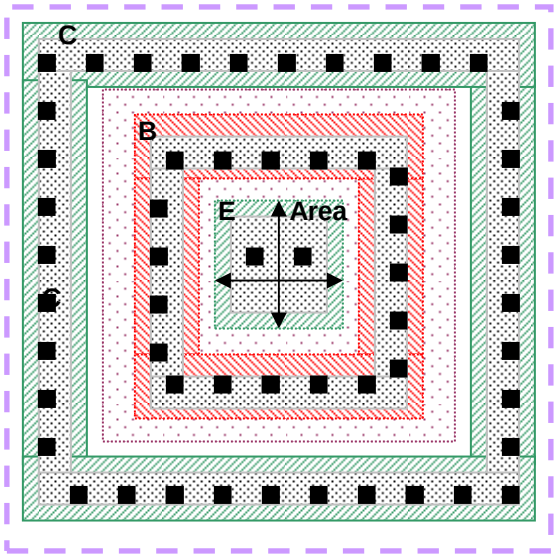


Spectre Netlist
Spectre Model Name = “gpdk090_vpnp5”
Q0 (C B E) gpdk090_vpnp5 area=25 m=1

DIVA LVS Netlist
DIVA Device Name = “vpnp5”
; vpnp5 Instance /Q0 = auLvs device Q0
d vpnp C B E
i 0 vpnp5 C B E " area 25.0 m 1.0 "

CDL Netlist
CDL Device Name = “vpnp5”
QQ0 C B E vpnp5 M=1 area=25.0

Assura Netlist
Assura auLvs Device Name = “vpnp5”
c vpnp BJT C B B B E B ;;
* 3 pins
* 3 nets
i Q0 vpnp5 C B E; area 25 m 1 ;



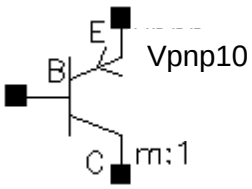
vpnp5 – 1.2 volt vertical substrate PNP with 5x5 fixed emitter

Device Layers	
Layer	**Color and Fill**
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	BJTdummy contains Nimp AND Pimp
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
Area	Area of Emitter (illustrated above)

14.32 vpnp10 datasheet

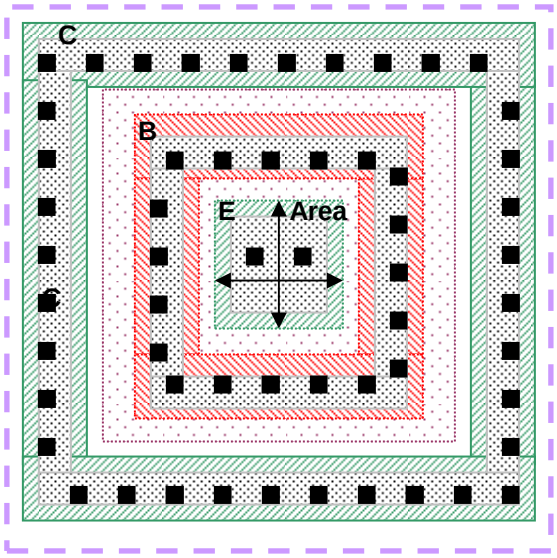


Spectre Netlist
Spectre Model Name = “gpdk090_vpnp10”
Q0 (C B E) gpdk090_vpnp10 area=100 m=1

DIVA LVS Netlist
DIVA Device Name = “vpnp10”
; vpnp10 Instance /Q0 = auLvs device Q0
d vpnp C B E
i 0 vpnp10 C B E " area 100.0 m 1.0 "

CDL Netlist
CDL Device Name = “vpnp10”
QQ0 C B E vpnp10 M=1 area=100.0

Assura Netlist
Assura auLvs Device Name = “vpnp10”
c vpnp BJT C B B B E B ;;
* 3 pins
* 3 nets
i Q0 vpnp10 C B E; area 100 m 1 ;



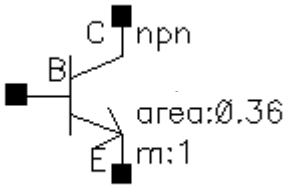
vpnp10 – 1.2 volt vertical substrate PNP with 10x10 fixed emitter

Device Layers	
Layer	**Color and Fill**
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	**Layer Derivation**
Recognition	BJTdummy contains Nimp AND Pimp
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
Area	Area of Emitter (illustrated above)

14.33 npn datasheet

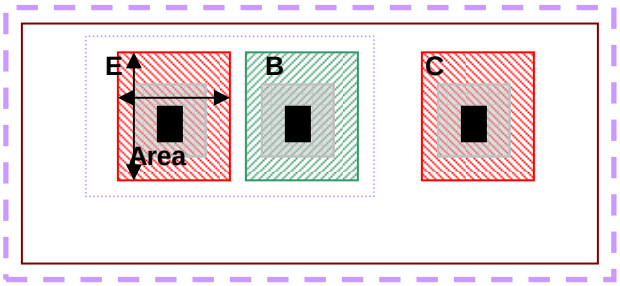


Spectre Netlist
Spectre Model Name = “gpdk090_npn”
Q1 (C B E) gpdk090_npn area=0.36 m=1

DIVA LVS Netlist
DIVA Device Name = “npn”
; npn Instance /Q1 = auLvs device Q1
d npn C B E
i 1 npn C B E " area 360e-3 m 1.0 "

CDL Netlist
CDL Device Name = “npn”
QQ1 C B E npn area=0.36 m=1

Assura Netlist
Assura auLvs Device Name = “npn”
c npn BJT C B B B E B ;;
* 3 pins
* 3 nets
* 0 instances
i Q1 npn C B E ; area 0.36 m 1 ;



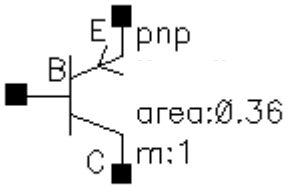
npn – Bipolar NPN with variable emitter area

Device Layers	
Layer	**Color and Fill**
NPNdummy	
Nburied	
Pwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	NPNdummy AND Nimp AND Pwell
E	NPNdummy AND Nburied AND Nimp AND Pwell
B	NPNdummy AND Nburied AND Pimp AND Pwell
C	NPNdummy AND Nburied AND Nimp ANDNOT Pwell

LVS Comparison	
Parameter	**Calculation**
area	Area of Emitter (illustrated above)

14.34 pnp datasheet

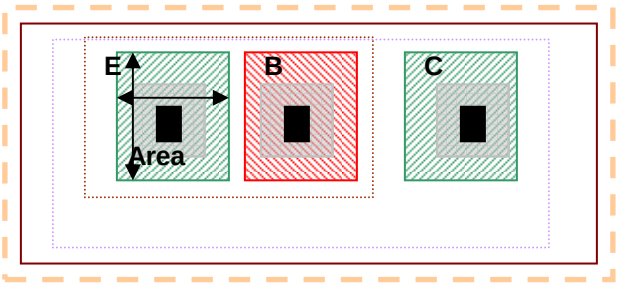


Spectre Netlist
Spectre Model Name = “gpdk090_pnp”
Q1 (C B E) gpdk090_pnp area=0.36 m=1

DIVA LVS Netlist
DIVA Device Name = “pnp”
; pnp Instance /Q1 = auLvs device Q1
d pnp C B E
i 1 pnp C B E " area 360e-3 m 1.0 "

CDL Netlist
CDL Device Name = “pnp”
QQ1 C B E pnp area=0.36

Assura Netlist
Assura auLvs Device Name = “pnp”
c pnp BJT C B B B E B ;;
* 3 pins
* 3 nets
* 0 instances
i Q1 pnp C B E ; area 0.36 m 1 ;



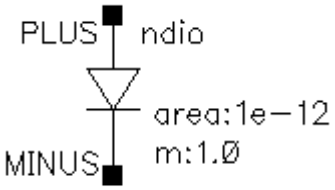
pnp – Bipolar PNP with variable emitter area

Device Layers	
Layer	**Color and Fill**
PNPdummy	
Nburied	
Nwell	
Pwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	PNPdummy AND Pimp AND Pwell
E	PNPdummy AND Nburied AND Pimp AND Nwell
B	PNPdummy AND Nburied AND Nimp AND Nwell
C	PNPdummy AND Nburied AND Pimp ANDNOT Nwell

LVS Comparison	
Parameter	**Calculation**
area	Area of Emitter (illustrated above)

14.35 ndio datasheet

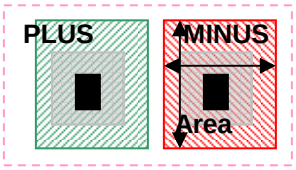


Spectre Netlist
Spectre Model Name = “gpdk090_ndio”
D0 (PLUS MINUS) gpdk090_ndio area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = “ndio”
; ndio Instance /D0 = auLvs device D0
d ndio PLUS MINUS
i 0 ndio PLUS MINUS " area 1e-12 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = “ndio”
DD0 PLUS MINUS ndio 160f 1.6u m=1

Assura Netlist
Assura auLvs Device Name = “ndio”
c ndio DIO PLUS B MINUS B ;;
* 2 pins
* 2 nets
i D0 ndio PLUS MINUS ; area 1e-12 pj 1.6e-6 m 1 ;



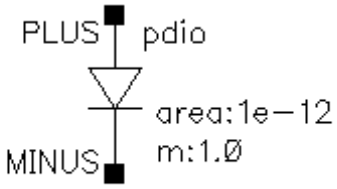
ndio – 1.2 volt N+/Psub diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIOdummy AND Nimp
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	**Calculation**
area	Area of MINUS (illustrated above)

14.36 pdio datasheet

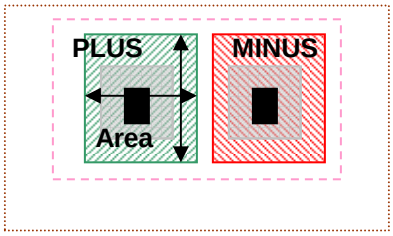


Spectre Netlist
Spectre Model Name = “gpdk090_pdio”
D0 (PLUS MINUS) gpdk090_pdio area=160f pj=1.6u m=1

DIVA LVS Netlist
DIVA Device Name = “pdio”
; pdio Instance /D0 = auLvs device D0
d pdio PLUS MINUS
i 0 pdio PLUS MINUS " area 160e-15 pj 1.6e-6 m 1.0 "

CDL Netlist
CDL Device Name = “pdio”
DD0 PLUS MINUS pdio 160f 1.6u m=1

Assura Netlist
Assura auLvs Device Name = “pdio”
c pdio DIO PLUS B MINUS B ;;
* 2 pins
* 2 nets
i D0 pdio PLUS MINUS ; area 1.6e-13 pj 1.6e-6 m 1 ;



pdio – 1.2 volt P+/Nwell diode

Device Layers	
Layer	**Color and Fill**
DIOdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

Device Derivation	
Device	**Layer Derivation**
Recognition	DIOdummy AND Pimp AND Nwell
PLUS	DIOdummy AND Pimp AND Nwell
MINUS	DIOdummy AND Nimp AND Nwell

LVS Comparison	
Parameter	**Calculation**
area	Area of PLUS (illustrated above)

15 GPDK090 packaging & deployment

REQ 15.1.1 :

The GPDK is packaged and distributed as a compressed tar file. The file will be available at http://pdk.cadence.com .

16 GPDK090 validation and testing

The STEP tool should be used to test the GPDK. The testplan should be outlined in a separate document.

17 GPDK090 Bug and Enhancement Tracking

The PCR system will be used to track bugs/enhancements for the GPDK.

Family	INTERNAL
Product	CDK090
ProdLevel2	GPDK090

18 Software Compatibility Requirements

Supported releases:

- IC 5.1.x (CDBA)
- IC 6.1.x (OA)

19 Platform Requirements

Hardware	Operating System	Requirements
HP (32 bit)	HP-UX	
Sun (64 bit)	Solaris	
PC	Linux	

20 Risks and challenges

The most challenging part of the project will be the creation of ‘realistic’ yet fictious device models.The GPDK will highly depend on the tools that will make up the CIC Platform. Lot of the tools are still in flux, especially OA based tools. This can have a negative impact on the quality and delivery of the GPDK.

21 Acronyms

Acronym	
GPDK	*Generic Process Design Kit*
ADE	*Analog Design Environment*
CIC	*Custom IC*