Appendix A

Fabrication Technology for Miniaturization

INTRODUCTION

Many of the technologies that have enabled advances in miniaturization were first developed for microelectronics and allow both lateral and thickness control in the creation of structures. Although the early techniques and tools were directed at silicon, recent years have seen increased attention to materials other than silicon: compound semiconductors, superconductors, metals, and insulators. Furthermore, they are being applied to more diverse areas: micromechanical structures, biosensors, and chemical sensors.

The same processes that have allowed for decreases in size also allow parallel production of many devices. Thousands or millions of transistors or other devices can refashioned simultaneously on one chip the size of a thumbnail, and many chips preprocessed at the same time on one wafer. The key steps in the process of creating these structures are:

- lithography,
- pattern transfer, and
- characterization.

LITHOGRAPHY

Integrated circuit fabrication techniques all rely on lithography, an ancient technique first used for artistic endeavors. The basic process involves covering an object with a thin layer of material (ancient artisans sometimes used wax) that can be patterned but will resist subsequent processing and protect the material underneath. Industrial lithographers use a hydrocarbon polymer, appropriately called "resist." A pattern is produced in the resist—usually by exposure to visible light or ultraviolet (UV) radiation —exposing selected areas of the material below. The exposed areas can then be modified in some way. Successive applications of this basic process produce a multilevel structure with millions of individual transistors in a square centimeter as described in figure A-1.

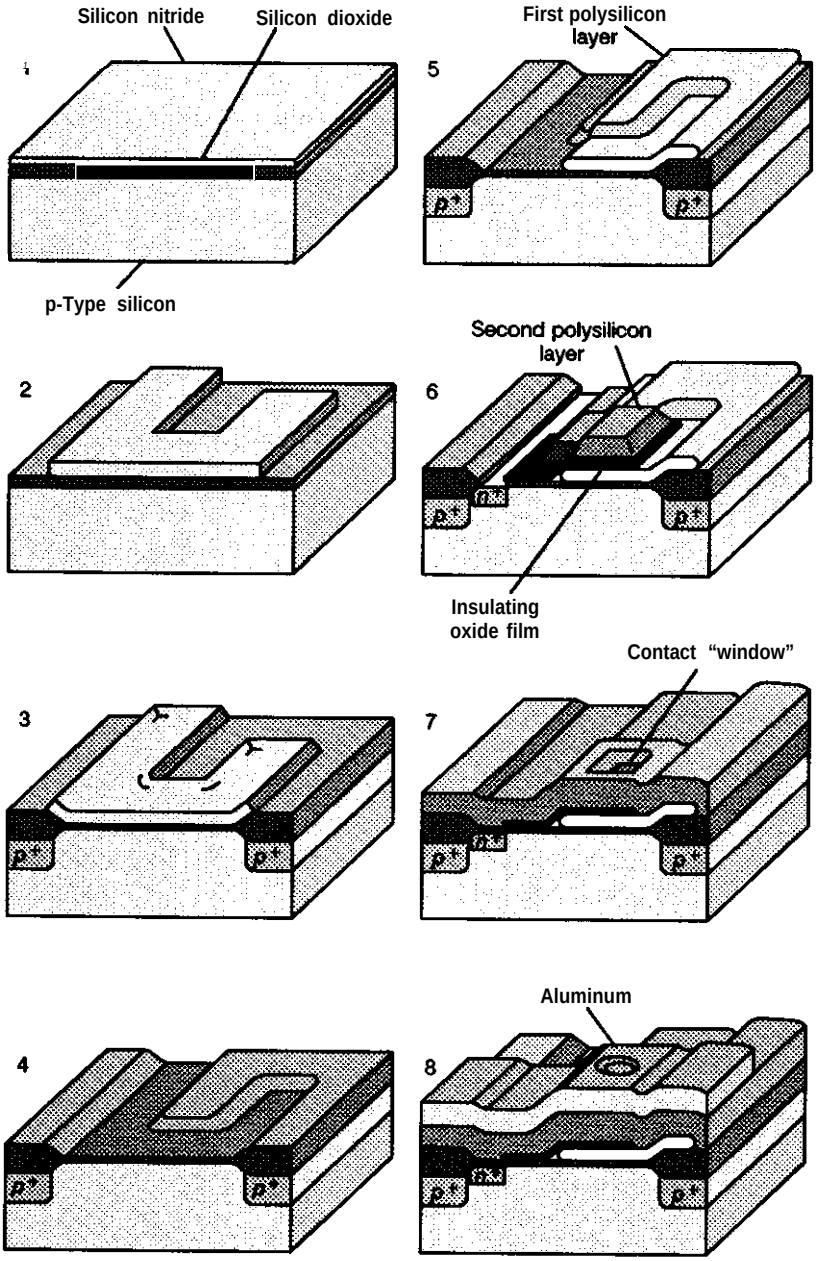
Photolithography is the most widely used form of lithography and is likely to continue to be so for the near future. UV light, usually with a wavelength less than 400 nanometers, is used to create patterns resist layers on flat surfaces. Diffraction of light—the interference of light waves with one another—limits the resolution or minimum reproducible feature size. Diffraction is minimized by reducing the wavelength of the exposing radiation. Mercury vapor lamps are routinely used as a source of 436 nanometer (G-line) and 365 nanometer (I-line) light. Shorter wavelength excimer laser sources are a new source of UV light with operation possible at 248 nanometers and in the future 193 nanometers and other wavelengths. By combining shorter wavelengths with improved mask technology (including phase shifted masks[2]), better optics, and more sophisticated resist chemistries, it is likely that photolithography will be usable to 0.25-microns minimum feature sizes and possibly below 0.2 microns.

The longevity of UV lithography is a subject of debate in the semiconductor industry. Many experts argue the limits of diffraction and depth of focus will prevent use of UV photolithography below 0.2 microns and that x-ray lithography, which uses substantially shorter wavelength radiation, will be the successor to UV lithography. X-ray lithography is a candidate for high volume production of integrated circuits with line widths below 0.5 microns. The most studied and developed form of x-ray use is "proximity printing,"

[1]H.G. Craighead and M. Skvarla, "Micro and Nanofabrication Technology, Applications & Impact," contractor report prepared for the Office of Technology Assessment, April 1990; and Tim Studt, "Thin Films Get Thinner as Research Heats Up,'' R&D Magazine, March *1990,* pp.70-80.

[2]Phase shift masks function by carefully controlling light diffraction, using the constructive and destructive interference to help create the circuit pattern. Phase shift masks hold greatest promise for manufacturing memory and other ICs with regular, repeated patterns.

Figure A-1 -Fabrication Sequence for a Metal-Oxide-Semiconductor (MOS) Circuit



Fabricating this MOS circuit element (a two-level n-channel-negative charge carrier- polysilicon-gate metal-oxide-semiconductor) requires six masking steps. The first few process steps involve the selective oxidation of silicon with the aid of a film of silicon nitride, which acts as the oxidation mask. A thin film of silicon dioxide is grown over the entire wafer, and a layer of silicon nitride is deposited from a chemical (l). The layer is selectively removed in a conventional photolithographic step in accordance with the pattern on the first mask (2). A p-type dopant (e.g., boron) is implanted using the silicon nitride as a mask, followed by an oxidation step, resulting in a thick layer of silicon dioxide in the unmasked-(3). The silicon nitride is then removed in selective etchant that does not attack either the silicon or silicon dioxide (4). Since silicon is consumed in the oxidation process, the thick oxide layer is partly recessed" into the silicon substrate. The first layer of polycrystalline silicon is then deposited and patterned in the second masking step (5). A second insulating film of oxide is grown or deposited, followed by the deposition of the second polysilicon layer, which is in turn patterned in the third masking step (6). A short etch in the hydrofluoric acid at this stage exposes certain regions to an implantation or diffusion of n-type dopant. A thin layer of silicon dioxide is deposited next, and contact "windows" are opened with the fourth mask (7). Finally a layer of aluminum is deposited and patterned in the fifth masking operation (8). The wafer will also receive a protective overcoating of silicon dioxide or silicon nitride (not shown); the fact that openings must be provided in this overcoating at the bonding pads accounts for 6 masking steps. Vertical dimensions are exaggerated for clarity.

SOURCE: William G. Oldham, 'The Fabrication of Microelectronic Circuits," *Microelectronics (San* Francisco, CA: W.H. Freeman & Co., 1977), p. 48. Copyright (c) 1977 by Scientific American, Inc.–George V. Kelvin.

where the mask is placed on the substrate material and its pattern is reproduced by exposure to x-rays, resulting in a substrate pattern the same size as the mask. Practical problems that must be addressed include complexity of mask technologies, difficulty in alignment of multiple layers, economical x-ray sources, and resolution limitations. X-ray lithography operates similarly to UV photolithography, but with much shorter wavelengths–around 5 nanometers. Proximity printing requires a bright source of x-rays. Synchrotron sources are the highest intensity sources of x-rays but they are very expensive. Most experts feel it is unlikely that proximity printing with x-rays will be practical below 0.2 microns, while others hold that the technology will be usable to 0.1 microns.

More recent exploratory work in x-rays involves "reduction projection lithography." X-rays are focused through a mask that is kept away from the substrate. The principal advantages of this approach are cheaper x-ray sources (a synchrotron is not required) and improved resolution. In this country, AT&T Bell Laboratories and other laboratories are investigating this technology. One of the greatest challenges to making projection x-ray lithography useful for manufacturing is the optics used in the process; they are complex, involving the creation of multiple-layer films with precisely controlled thickness.

Another way to get beyond the diffraction limit of radiation-based lithography is to use electrons or atoms to expose the resist. Diffraction does not limit the resolution of electron-beam lithography because the quantum mechanical wavelengths of high energy electrons are exceedingly small. Electrons scatter quickly in solids, limiting practical resolution to dimensions greater than 10 nanometers—significantly greater than current demands of any practical technology. Electron-beam lithography has demonstrated resolution as small as 2 nanometers (0.02 microns) in a few materials. Electron beam technology, however, is limited in usefulness because an electron beam must be scanned across the entire wafer. Electron-beam lithography tools are in use in universities, in laboratories, and in industry for mask-making and small manufacturing production runs.

There are approaches still in research that may yield a more versatile lithography tool. A possible alternative is to use photolithography for large feature definition and reserve the scanned electron beam for the critical dimensions. A varietyof approaches for parallel exposure, rather than serial scanned exposure, of electron-beams have been studied for years. There is currently active research in electron beams reduction projection using masks at AT&T Bell Laboratories, and in multiple source systems and proximity printing at IBM. These approaches would exploit the resolution and alignment possibilities of electron beams with the speed of parallel exposure techniques.

Ion beam lithography is in many ways similar to electron beam lithography with beams of charged atoms (ions) taking the place of electrons. Recent advances in ion sources have increased the utility of scanned focused ion beams. Compared to photons (x-rays and light) or electrons, ions chemically react with the substrate, allowing a greater variety of modifications. Some scattering effects are also reduced compared to electrons and, as with electrons, diffraction limits of ion beams are negligible. The fundamental resolution limits for charged particle lithographies are below 1(M) nanometers. Ion beam lithography suffers the same draw back as electron beam systems; it relies on a serially scanned beam. That limits its applications to products that do not require high throughput—e.g., masks and small batches of electronics. Research efforts are underway to develop parallel projection and multiple source ion beam lithographic equipment that might overcome the limitations of serially scanned ion beam lithography.

Scanned probe modification of surfaces, using recently developed scanning tunneling microscopy (STM) methods, is being done by researchers in many research laboratories. Since STMs can manipulate individual atoms, such approaches have theoretical resolution limits of single atoms. This approach is still in early phases of research and is focusing on basic physics measurements

and better understanding of the behavior of surfaces. The lack of stability of STM tips and slow speed, however, make it far from a practical technology for manufacturing in the foreseeable future.

PATTERN TRANSFER

The various lithography systems produce relief patterns in resists, and a subsequent pattern transfer step is necessary to fabricate the structure. There are a number of options available and each involves some engineering tradeoffs. Once the resist pattern is in place, and selected areas of the underlayer are exposed, there are three possible next steps: 1) add to, 2) remove, or 3) modify the exposed areas.

Adding to the exposed area involves either deposition or growth of a material on the exposed areas. Growth is different from deposition because it involves consumption of the surface (usually combining with some introduced chemical) to create the new substance. The most common example is a silicon surface being consumed in the process of forming silicon dioxide. It involves heating the silicon wafer in the presence of oxygen, causing the growth of silicon dioxide from the exposed silicon. A number of materials are grown in this way, since the consumption of the surface results in excellent adhesion, better electrical and mechanical properties, and improvements in other materials properties. This specific reaction has been exhaustively investigated and perfected and now can be used to grow oxide films whose thickness, and even lateral dimensions, can be measured in atomic layers (a few angstroms).

Deposition creates new layers of material on the exposed area. These techniques usually involve evaporating or sputtering a piece of material-the target-so its atoms or molecules fly off and land on the sample. Deposition techniques include:

- spin-on,
- thermal evaporators,
- sputtering,
- . laser ablation deposition,
- chemical vapor deposition; and
- molecular beam epitaxy such as organometallic chemical vapor deposition.

Spin-on deposition is the simplest deposition technique. It involves spinning the sample while a liquid is poured onto it; the spinning action distributes the liquid evenly. Subsequent heating bakes the liquid into a solid thin film.

Thermal evaporators use a heated filament or an electron beam to vaporize material. The material passes through a vacuum to impinge on the sample, building up a film. Evaporators emit material from a point source, resulting in "shadowing" and sometimes causing problems with very small structures.

Sputter deposition systems erode atoms from a broad target that then travel to the sample. This results in better line width control and uniformity, especially with high aspect ratio (height/width) structures. Refinements of these processes, e.g., in situ cleaning with an ion gun, or using electron cyclotron resonance to confine and densify a plasma, result in better adhesion, higher quality films, and more versatility. Using lasers or particle beams in conjunction with deposition presents the possibility of defining patterns on the sample in a single step.

Laser ablation deposition uses intense laser radiation to erode a target and deposit the material onto a substrate. This technique is particularly useful in dealing with compounds of different elements —e.g., yttrium-barium-copper oxide superconductor films.

Chemical vapor deposition (CVD) deposits thin films by passing reactive gases over the sample. The substrate is heated to accelerate deposition. CVD is used extensively in the semiconductor industry and has played an important role in past transistor miniaturization by making it possible to deposit very thin films of silicon. Most CVD is performed in vacuum, but new techniques allow operation without vacuums. Radio frequency (RF) or photon radiation can be used

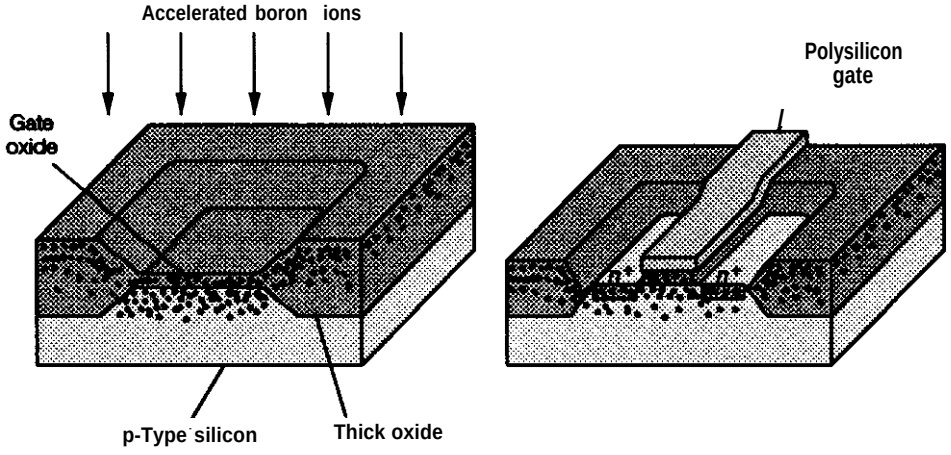
to enhance the process and is known as plasma enhanced CVD (PECVD).

Some deposition techniques are so precise that material can be built up literally atom by atom with the crystal structure of the new material exactly matching that of the underlying layer. In molecular beam epitaxy (MBE), the sample is placed in an ultra high vacuum in the path of streams of atoms from heated cells that contain targets of various types. These atomic streams impinge on the surface, creating layers whose structure is controlled by the crystal structure of the surface, the thermodynamics of the constituents and the sample temperature. Organo-metallic chemical vapor deposition (OMVPE, or sometimes MOCVD) relies on the flow of gases (hydrides like arsine and phospine or organometallics like tri methyl gallium and tri methyl aluminum) past samples placed in the stream. Again, the sample surface and thermodynamics of the processes determine the compounds deposited. Both MBE and OMVPE provide thickness control within one atomic layer (a few angstroms) and are especially useful in creating compound semiconductors and exploiting quantum effects and band-gap engineering. This structural control enables researchers to exploit optical transitions in some materials, producing lasers, detectors, and other optical elements.

Materials modification processes are used mainly to vary the electrical conductivity in the appropriate areas. In the past, dopants (atoms that can either contribute or subtract electrons from silicon atoms) were diffused into the substrate thermally; now they are implanted as high energy ions (see figure A-2). Implantation offers the advantage of being able to place any ion at any depth in the sample, independent of the thermodynamics of diffusion and problems with solid volubility and precipitation. Ion implantation, originally developed for high energy physics, is now an indispensable part of semiconductor manufacturing. Ion beams produce crystal damage in addition to the chemical or electronic effect of the dopants. Since crystal damage reduces electrical conductivity, this effect can be exploited to electrically isolate devices from one another. Ion beams can implant enough material to actually form new materials--e.g., oxides and nitrides-some of which show improved wear and strength characteristics.

Subtractive processes—the removal of material-are also vital to the field. Some of the steps are still done the same way they were centuries

Figure A-2–ion Implantation



Ion implantation is employed to place a precisely controlled amount of dopant (in this ease boron ions) below the gate oxide of a MOS transistor. By choosing a suitable acceleration voltage the ions can be made to just penetrate the gate oxide but not the thicker oxide (left). After the boron ions are implanted polycrystalline silicon is deposited and patterned to form the gate regions of the transistor. A thin layer of the oxide is then removed and the source and drain regions of the transistor are formed by the diffusion of an n-type impurity (right).

SOURCE: William G. Oldham, "The Fabrication of Microelectronic Circuits," *Microelectronics* (San Francisco, CA: W.H. Freeman & Co., 1977), p. 50. Copyright (c) 1977 by Scientific American, Inc. -George V. Kelvin.

ago. The object, with its lithographically defined areas exposed and the remainder protected by the "resist," is dipped into a chemical bath and a reaction or dissolution is allowed to take place. Unfortunately, liquid chemicals usually have no sense of direction and will dissolve at an equal rate on all sides. As device geometries shrink, it becomes important to control directionality. Most modern etching is done in vacuum without contact with liquids.

Ion milling uses the sputtering process to bombard the substrate with accelerated ions. The sputtering process relies on a physical mechanism whereby energy is transferred to a surface by impinging ions. This energy is enough that some atoms break free of the surface. This mechanism erodes all materials, with small differences in rate between any two. Selectivity is poor, and any masking material (resist) will disappear as fast as the underlayer, limiting the (relief) depth.

Reactive ion etching (RIE) can be highly selective because it is a chemical reaction between ions (radicals) formed in a plasma and atoms on the sample surface, and can be highly selective. RIE has excellent lateral control because the electric fields produced by the plasma cause ions to diffuse directionally. Straight parallel trenches a micron or more deep can be etched without affecting a rather fragile resist mask; minimum feature sizes of a few nanometers are possible. RIE is highly selective in its etching: oxygen etches hydrocarbons (resists), fluorine compounds are useful in working with silicon systems, and many materials are susceptible to chlorine etch, especially the compound semiconductors like gallium arsenide. A great deal of work is directed at discovering the etching characteristics of other compounds.

The combination of physical and chemical etching is achieved in a process called chemically assisted ion beam etching (CAIBE). The combined effects of ion sputtering and chemical reaction with reactive ions results in a faster etch rate than that due to either mechanism alone. CAIBE is of particular interest to research groups investigating new materials, since it can be exploited to uncover ways to etch new and exotic materials.

Unlike ancient lithographs, modern semiconductors must undergo many processing steps. The mask must remain intact until the substrate etch is complete, without changing feature size or shape or surface characteristics (morphology). Multiple operations are often required because of the processing limitations of materials. For example, to grow a thin layer of silicon dioxide at 1,000°C, a resist is used to pattern a silicon nitride layer which is then capable of surviving the high temperature during the oxide growth. Multiple layers are often processed in succession to better allow a straightedge to be carried through a thick stack of material.

CHARACTERIZATION

Characterization has become an indispensable tool in the art and science of fabrication. The designer needs information about device performance, the experimenter needs to know composition and concentration, and the process engineer must have immediate confirmation of the electrical, mechanical, optical, or chemical properties of a thin film. In fact characterization, or failure analysis, is in some cases as difficult and extensive as the original experiment. The most common questions addressed by characterization concern the shape and size of the structure. Optical and electron microscopes provide this information over size ranges from hundreds of microns to fractions of a nanometer (near-atomic dimensions).

Instruments also exist to measure a range of materials properties, including the thickness, refractive index, and electrical resistivity. While these techniques involve the measurement of thin film properties over large distances, microcharacterization can determine composition or structure on a size scale comparable to the mean free path of an electron and some techniques have an ultimate resolution on the order of a few atomic diameters.

There are a wide range of techniques usually identified by acronyms, and some of the more useful are listed here:

SCANNED BEAM TECHNIQUES

SEM – Scanning electron microscope: creates image of a surface by measuring the reflection from a beam of electrons.

TEM – Transmission electron microscope: determines crystal structure by measuring transmission of electrons through a thin sample; has high resolution.

AES – Auger electron microscopy: identifies constituents in the surface layer by measuring energy of electrons emitted due to "Auger transitions."

RBS – Rutherford backscattering spectroscopy: identifies constituents by measuring the spectrum of scattered ions off a sample.

SIMS – Secondary ion mass spectroscopy: analyzes composition of material removed by ion bombardment.

XRF – X-ray fluorescence: identifies composition from photon emission due to x-rays.

EDS (EDX)— Energy dispersive x-ray spectroscopy: identifies composition from dispersion of x-rays.

IMMA – Ion microprobe mass analysis: high resolution secondary ion mass spectroscopy (SIMS).

EELS – Electron energy loss spectroscopy: identifies composition by measuring energy loss of electrons during electron interaction.

ED – Electron diffraction: measures crystal structure by diffraction of electrons.

LEED – Low energy electron diffraction: measures surface structure by diffraction of electrons.

RHEED – Reflection high energy electron diffraction: measures surface structure; particularly useful for epitaxial film growth.

SCANNED PROBE TECHNIQUES

STM – Scanning tunneling microscopy: creates image of surface using electron tunneling between the surface and a sharp tip near the surface; very high resolution.

AFM – Atomic force microscopy: creates image of surface using repulsion of electron charge distributions between surface and a tip; near-atomic resolution is possible.

SxM – Other developing scanned probe microcopies: create images of surface characteristics for magnetic force, electrochemical measurement, etc., using the principle of the STM.