Contributions of DOE Weapons Labs and NIST to Semiconductor Technology

September 1993

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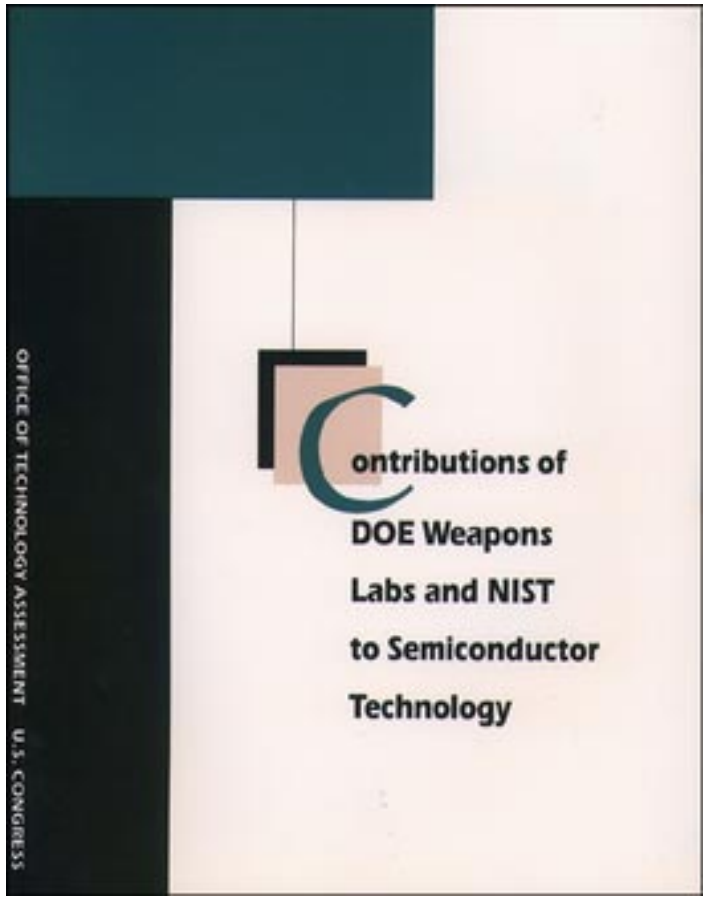

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Foreword

The federal laboratories of the United States are a diverse lot. For those whose primary function was advancing military technologies, the end of the Cold War has meant reexamination of missions, abilities, and resources on a scale grander than anything that has occurred in decades. In particular, the Department of Energy's nuclear weapons laboratories (Lawrence Livermore, Los Alamos, and Sandia National Laboratories) are under close examination. Throughout their existence, the weapons labs' primary missions have involved nuclear weapons. One of the most important is nuclear weapons development, and that function has diminished considerably as a result of the end of the Cold War. While other weapons-related missions remain important, a consensus has emerged that the labs are, in a sense, larger than their remaining missions warrant. But the issue is much larger than simply how much to cut and how to manage the reduction.

National security is still the issue, but defined more broadly than in the past, when it was confined to military security. The concept of national security is now expanding to include industrial competitiveness, and there is lively interest in examining how all the labs in the federal system could contribute to advancing science and precommercial technology. The debate over whether and how to expand the missions of the DOE labs has also raised questions of how to coordinate these new activities with those of labs and agencies that already have responsibility for civilian technology policy—principally the National Institute of Standards and Technology of the Department of Commerce. NIST has emerged in the last few years as one of the federal government's major players in civilian technology advancement through, for example, management of the new and well-regarded Advanced Technology Program.

This Report examines how NIST and DOE weapons laboratories could contribute to advances in semiconductor technology aimed specifically at civilian applications. Semiconductor technology was chosen as an example of a technology focus for a civilian technology initiative, primarily because the industry had already developed a set of comprehensive technology roadmaps and the federal labs had substantial expertise in the area. The Report was requested as a follow-on assessment to OTA's work on the implications for the U.S. civilian economy of the end of the Cold War. That work consists of two Reports: *After the Cold War: Living With Lower Defense Spending,* and *Defense Conversion: Redirecting R&D.* The former considered the effects on defense workers, defense-dependent communities, and defense companies, and suggested policy options to ease transitions for those affected by cutbacks. The latter examined how the R&D institutions whose primary missions were defense-related could contribute to national well-being under a broader concept of national security.

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Contents

Summary and Policy Discussion 1

The federal laboratories possess resources, technologies, and talents that could contribute to the development of semiconductor product and production technologies. Whether they will be able to is uncertain. In particular, the three Department of Energy (DOE) weapons laboratories and the National Institute of Standards and Technology (NIST) are well positioned to contribute to advancing technologies; all four currently participate in R&D partnerships with industry. While the extent of that participation varies greatly among the laboratories, it is clear from OTA's evaluation that there is room for all four labs to expand these partnerships without treading on the toes of other laboratories (private or public), but only if the effort is managed properly.

However, there are several issues that must be resolved if those contributions are to be made in effective, efficient, and synergistic ways. It is quite unlikely that the labs' most effective contributions will happen automatically, notwithstanding the interest among both lab and industry representatives regarding current R&D partnerships. The thorniest issues are:

- developing an effective means of managing the disparate efforts of labs and industry so as to make the greatest possible contribution to commercial technology development, while the labs continue to work on microelectronics in connection with public missions;

[1] For the purposes of this report, these are Livermore, Los Alamos, and Sandia National Laboratories. The Y-12 plant at Oak Ridge National Laboratory is included as a weapons laboratory in DOE accounts, but it is not comparable to the other weapons laboratories in size or scope of work. **Readers not familiar with the semiconductor industry should start this report by reading chapter 3.**

- focusing the labs' efforts on the areas in which their contributions are most needed and their talents most suited; and
- assuring a private-sector presence and commitment sufficient to take the hand-off of publicly funded technologies.

In addition, there is some concern over how to minimize competition or redundancy among laboratories and agencies if lab-based microelectronics R&D is expanded. Other policy issues include funding and development of performance criteria for labs' efforts devoted to civilian semiconductor technology. If these issues are not resolved, much of the promise of ongoing R&D agreements between industry and the labs—particularly the DOE labs—may never be realized, and the enthusiasm of both lab and industry representatives for cooperative work could die.

Ten years ago, this loss would have mattered less; private funding for R&D was more abundant, and labs' technologies were perhaps less relevant to commercial needs. Today, however, cooperative technology development between government and industry is more important than at any other time in the postwar period, especially in industries like microelectronics, where R&D costs are escalating more rapidly than revenues (figure l-l). Many feel that industry's capacity to support escalating costs of technology development is strained; one member of an OTA workshop convened for this assessment asserted that it is becoming difficult for companies to fund the development of the next generation of technology from revenues made on the current generation. The pressure is compounded by rapidly rising plant and equipment costs. Generational changes in semiconductor technology are swift—the Semiconductor Industry Association (S IA) technology roadmaps assume that generational changes will occur every three years, on average, and each new generation entails rapidly escalating expenditures on plant and equipment. Estimates of the cost of wafer fabrication facilities (fabs) stretch to a billion dollars even for the next generation of semiconductors (equivalent to a 64-Megabit DRAM? fab), expected to come on line around 1995.[3] If the costs of new wafer fabs are any predictor of future costs, SIA expects semiconductor revenues to be inadequate to support construction of new fabs beyond 2001.[4] In short, it is becoming increasingly difficult for the industry to find the funds to support both ballooning capital expenditures and rapidly rising R&D costs; cooperative arrangements have been burgeoning as a result.

In the United States, most of the existing cooperative R&D enterprises are private. Semiconductor companies are linked to other companies via an expanding web of technology development and production agreements, many of which span national borders. A few have government support, most notably the industry consortium SEMATECH, which receives half its funding from the Department of Defense (DoD). The impetus for SEMATECH's formation, however, came from the industry itself, as did the Semiconductor Research Corporation (SRC), which was created by the SIA members in 1981. This is a contrast with other semiconductor-producing nations, where government support for commercial semiconductor technology and industrial development has been far more extensive and, in some cases, stretches back more than two decades.[5]

Government support of SEMATECH, originally planned for five years starting in 1987, has

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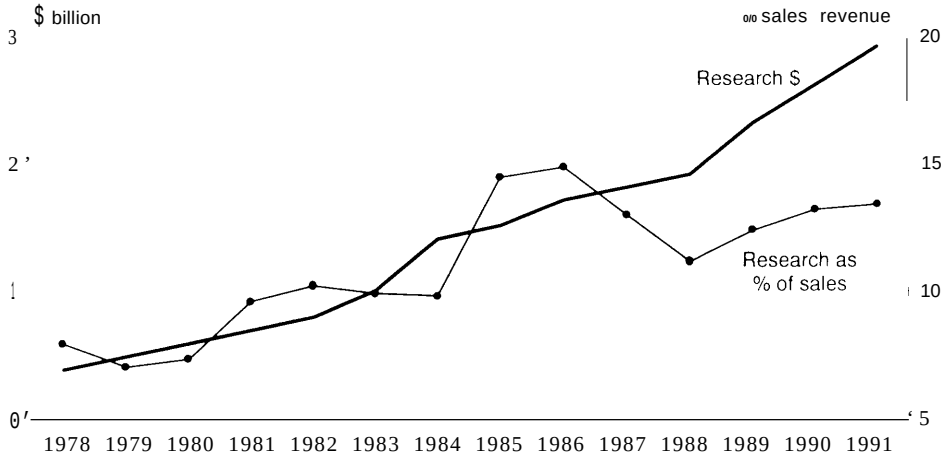
[2] DRAM stands for dynamic random access memory.

[3] Semiconductor Industry Association *Semiconductor Technology: Workshop Conclusions (San* Jose, CA: Semiconductor Industry Association 1993), pp. 6 and 18; and *Electronic Engineering Times*, ''*IEDM* Eyes Economics," Sept. 21, 1992.

[4] Ibid.

[5] U.S. support for semiconductor technology development goes back even farther, to the immediate post-World War II years, when the Department of Defense played a key role in the industry's development and growth. However, support for commercial semiconductor technologies has rarely been considered in the United States, and did not become a reality until the mid-1980s.

Figure I-l—Sales Revenues and R&D Expenditures in the U.S. Semiconductor Industry, 1978-1991



SOURCE: Semiconductor Industry Association, Annual Databook: Global and U.S. Semiconductor Competitive Trends-1978-1991 (San Jose, CA: Semiconductor Industry Association, 1992), p. 41.

been extended at $100 million in FY 1993 (the same as in earlier years), in addition to ARPA's (the Advanced Research Projects Agency of DoD) funding of approximately $300 million worth of R&D on microelectronics.[6] Government has also supported a few projects in other consortia, including SRC and the Microelectronics and Computer Technology Corporation, although most of the resources of these consortia are private.

The major purpose of government support and funding for semiconductor technology development has been for the military, and most of that came from the Department of Defense. While a few DoD labs have pursued microelectronics technology R&D, the largest share of military spending on microelectronics has been in the form of research funding in private companies. Both DOE and the Department of Commerce (DOC) have laboratories, and DOE's in particular are large and well-equipped. Until the end of the Cold War, DOE's work in semiconductor and microelectronics technologies was mostly related to nuclear weapons, and not very much of it was aimed at or available to commercial integrated circuit manufacturers. Now, however, the DOE labs are being encouraged to work with industry in cooperative R&D programs, and as industry and lab researchers become more familiar with each other's resources and abilities, enthusiasm for joint projects has permeated the working levels as well.

A new form of cooperative arrangement is now emerging. In this new arrangement, which often takes the form of a cooperative research and development agreement (CRADA), researchers at government labs and in private industry work together to solve problems of mutual interest, usually without any money changing hands. DOE labs gained authority to execute CRADAs in late 1989, and since then the CRADA has become the primary vehicle for cooperative R&D with industry.[7] NIST, with longer-standing ties to industrial technologies, has had CRADA authority since

6 Not all this money goes to projects that benefit Commercial semiconductor production as ARPA must look after DoD's special needs for semiconductor technology. However, ARPA's mission is also strongly dual-use, and many of ARPA's projects help advance commercial technologies as well.

7 For a more complete discussion of DOE CRADA activities, opportunities, and problems, see U.S. Congress, Office of Technology Assessment, *Defense Conversion: Redirecting R&D,* OTA-ITE-552 (Washington DC: U.S. Goverment Printing Office, May 1993).

1986, in addition to nine decades' experience in working on problems of a commercial nature.[8] NIST's labs are a national repository of metrology[9] technologies, and they have had productive interactions (using many mechanisms, not just CRADAs) with the semiconductor industry stretching back more than three decades.

All four labs have CRADAs with industry in microelectronics. The DOE labs report that the value of DOE finds committed to CRADAs with the U.S. semiconductor industry, as of summer 1993, is over $110 million. The underpinning of these efforts is approximately $100 million worth of existing program efforts in microelectronics at the three DOE laboratories,[10] and $9.5 million in internal funds and $7.8 million in Advanced Technology Program funds at NIST[11] In the course of pursuing its mission, each laboratory has developed some competencies that semiconductor industry representatives believe could contribute to technological advance, in direct support of the SIA technology roadmaps, if properly managed (see ch. 2 for a discussion of core competencies, and box 1-A for a discussion of the SIA roadmaps).

In addition, several interagency and consortia/agency efforts have begun. Sandia and NIST have a memorandum of agreement (MOA) governing the two labs' collaborative efforts in a number of technology areas.[12] SRC, which manages research for a consortium of semiconductor companies, is trying to initiate CRADAs with all three DOE weapons laboratories; Los Alamos is an SRC member.[13] Defense Programs, at DOE headquarters, recently began to explore the feasibility of SRC coordinating the various cooperative research projects at all the DOE weapons labs on soft x-ray projection lithography, a technology that, if it proves viable and cost-effective, could be ready for commercial use by 2007.[14] SEMATECH has had a cooperative research agreement with Sandia for several years, and initiated anew, $100-million, **five-year** agreement in early 1993. At the end of August 1993, the agreement included over 20 projects, such as tool benchmarking and characterization, materials and manufacturing process modeling and development, metrology, and contamination-free manufacturing.

Unfortunately, CRADAs have proven time-consuming and troublesome to initiate at DOE (NEST'S CRADA process is much swifter and more predictable, in part because the legislation governing CRADA authority at NIST makes the process simpler than DOE's CRADA authority). Most DOE CRADAs, particularly those with weapons labs, still take over eight months to start after submission of a work proposal, which itself may take many months for industry researchers to prepare. Some of the reasons for this are the fault of the agency or the labs, though some are not

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[8] Most of NIST's work is and has been commercial, but the NIST labs have had substantially greater military funding in the past. In both World Wars, NIST's work was heavily oriented to military work. See Nelson Robert Kellogg, *Gauging the Nation: Samuel Wesley Stratton and the Invention of the National Bureau of Standards,* Ph.D. Dissertation The Johns Hopkins University, 1992.

9 Metrology is the science of measurement.

10 Avtar s. Oberai, ''The OTA Report on Federal Labs and the Semiconductor Industry,'' Contractor report for the Office of Technology Assessment, June 1993, p. 60.

11 The Advanced Technology Program (ATP) is a program of mostly private research, of which about half is funded by NIST. NIST holds competitions for ATP funding, and selects from among proposals made by private, university, and occasionally government researchers in a variety of fields. ATP projects do not involve NIST research or onsite research at NIST.

12 These areas include development of advanced packaging technology, procedures and standards for characterizing lithography tools, techniques for model verification, and methods to improve integrated circuit performance, yield, and reliability. Source: ''Memorandu of Agreement between the National Institute for Standards and Technology and Sandia National Laboratories," March 16, 1993, mimeo.

13 Sandia has been a member in the past, but is no longer.

14 Personal communication with William C. Holton, Vice President, Research Operations, Semiconductor Research Corporation, July 14, 1993.

Box 1-A–The SIA Roadmaps

Over the past decade and a half, the Semiconductor Industry Association (SIA) has played an increasingly important role in supporting the industry's competitiveness. The very formation of the association was at least partly a response to the rise of Japanese competition; so was SIA's initiation of SRC in t he early 1980s and SEMATECH a few years later. Some of the competitive problems of the 1980s have been solved, and SRC and SEMATECH played important roles in many of the solutions. A new set of technical challenges confronts the industry in the 1990s. SIA's response was to convene a group of experts-mostly from the semiconductor industry and its customers, with several academ ics, government experts, and representatives from national laboratories--in late 1992 to "create a common vision of the course of semiconductor technology over the next 15 years."[1]

The group, through the course of several meetings and much off-line work, was able to create such a vision, specifying the characteristics of cutting-edge semiconductor technology in 2007, shown in table 3-5. Working groups assembled roadmaps of what efforts would be needed in 11 areas to assure that these technological advances could be made. The 11 areas are chip design and test, process integration, lithography, interconnects, materials and bulk processes, environmental safety and health, manufacturing systems, manufacturing facilities, process/device/structure computer-aided design (CAD), packaging, and equipment design and modeling. The roadmap lays out what performance must be achieved in each area, and what inquiries should be conducted, in order to meet broader semiconductor performance specifications.

The efforts that culminated in the roadmap date back several years. In the late 1980s, the National Advisory Committee on Semiconductors (NACS) examined future technological challenges to the semiconductor industry. This effort was followed by the MicroTech 2000 workshop, which focused on the requirements needed to accelerate technology development by one generation, producing a 1-gigabit static random access memory (SRAM) by the year 2000.[2] Construction of the roadmap was an outgrowth of MicroTech 2000.

SIA plans periodic updates of the roadmap as work underway in industry, academia, and government begins to narrow choices between technology options. Technology forecasts are notoriously unreliable past the short term, and updates and revisions will be needed to keep on track with both planned and unexpected developments in the industry.

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1 Semiconductor Industry Association, *Semiconductor Technology: Workshop Conclusions* (San Jose, CA: Semiconductor Industry Association, 1993) pp. iii-iv.

2 *MicroTech 2000 Workshop Report: A Report to the National Advisory Committee on Semiconductors*, August 1991.

(box l-B). While industry's appetite for joint research with the DOE labs has been unexpectedly vigorous in the four years that the labs have had authority to enter CRADAs, the difficulty and trouble it takes to establish one is frustrating to many industry participants.[15] If Congress or DOE initiates a formal program of R&D aimed at areas of the SIA roadmaps, creation of a special means of managing cooperative R&D might be necessary. For instance, the Superconductivity Pilot Center Agreement (SPCA) is a means of arranging for cooperative R&D between companies or universities and the DOE labs that maintain Superconductivity Pilot Centers, and they appear

15 See U.S, Congress, Office of Technology Assessment, op. cit., chapters 1, 2, and 4, for a discussion of the CRADA process at DOE.

Box 1-B–The DOE CRADA[1]

The cooperative research and development agreement (CRADA) became an accepted way for government, industry, and academic researchers to engage in shared research in the 1980s. Most government laboratories got the authority to initiate CRADAs in 1986, with the passage of the Federal Technology Transfer Act (FTTA). FTTA authorized government-owned, government-operated (GOGO) labs to sign CRADAs with any outside organization, including businesses, nonprofits, and state and local government organizations. Federal Order 12591 of April 1987 authorized the directors of GOGO labs to negotiate the division of funds, services, property, and people with outside organizations in CRADAs, subject to the requirement that labs could contribute in-kind services, but not funds. Under FTTA, NIST labs could initiate CRADAs, and the Federal Order gave lab directors at NIST broad authority to approve agreements. NIST already had many ways of dealing with industry, and maintains many mechanisms still, but the CRADA became an important instrument over the next few years.

DOE's labs are nearly all government-owned, contractor-operated (GOCO) labs, and FTTA did not give them CRADA authority. That authority was granted in 1989, with the passage of the National Competitiveness Technology Transfer Act (NCTTA), and the powers of laboratory directors to enter into CRADAs were substantially different under NCTTA than under FTTA. NCTTA requires GOCO laboratories to gain approval from their departments of both the CRADA (which is a legal document) and a statement of work before initiating a CRADA; GOGOs do not face this requirement. Partly as a result of this requirement, and partly due to unfam iliarity with the process, DOE's CRADA process has proved frustratingly slow to many in industry. Most of the attention has focused on CRADAs with the weapons laboratories, partly because of their large size and resultant visibility, and partly because the lion's share of CRADA money comes through Defense Programs (DP) in DOE, which manages the weapons labs. As of mid-1 993, it still took eight months or more to initiate a CRADA with a DOE weapons laboratory, beginning with the submission of a proposal. About half the time typically has been taken for review and ranking of proposals, a process that involves teams from the labs ranking proposals and forwarding prioritized lists to DP for headquarters selection. The other half has been used to negotiate the CRADA

1The information in this box is drawn from U.S. Congress, Office of Technology Assessment, *Defense Conversion: Redirecting R&D*, op. cit., pp. 98-120.

to be working more smoothly than the CRADA process.[16]

Government/private cooperative work to strengthen semiconductor product and process technologies has been helpful in the past and is even more promising today, but several measures could help assure that the program results are timely, useful, and efficient. Industry and lab researchers are interested in cooperative work, and both see that they have much to gain through working together. This enthusiasm is most readily measured by the volume of CRADA activity. But that is not a good measure of the overall success of cooperative R&D, which will depend on finding the right management structure, selecting and using appropriate evaluation criteria, taking steps to improve business plans and industrial strength as well as R&D in weak parts of the industry, selecting appropriate roles and projects for government labs, and providing for adequate funding of the federal part of the effort.

16 For a more complete discussion of SPCAS, see U.S. Congress, Office of Technology Assessment, op. cit., pp. 101-102.

itself. The labs take the lead in the negotiations, subject to guidance and review by DOE field offices and, in some cases, headquarters.

It has become common for critics of the DOE CRADA process to compare it with NIST's swifter, simpler one. This comparison is bot h misleading and unfair, partly due to the differences in authorit y of GOGO and GOCO labs. There are several other reasons for the difference. One is simply that DOE labs' authority to enter into CRADAs coincided with the National Technology Initiative (NTI), a special federal program of the Bush administration to stimulate cooperative technology development between government labs and industry, which generated an unexpectedly large industry interest in CRADAs at a time when DOE and its labs were trying to learn how to manage their new authority. Another factor is magnitude: t he three weapons laboratories are the largest federal laboratories in the country, with a combined budget of $3.4 billion in 1993. NIST's lab budget, in contrast, was $599 million in FY 1993 (including the Advanced Technology Program). As of mid-1993, the average DOE CRADA involved more than $800,000 in funding; the average NIST CRADA, $200,000. By the end of FY 1993, the value of DOE's CRADAs probably will come to around $400 m ill ion, and t he agency has asked for $198 m illion in operating funds for DP technology transfer (most of which is expected to go toward CRADAs), a sizable program by any accounting. Considering t hat the DOE CRADA program is barely four years old, it is not surprising t hat the agency and labs have had t heir hands full trying to devise adequate oversight and management mechanisms, and that those mechanisms are not yet streamlined.

However, understanding the reasons for the time involved in initiating an agreement with a DOE lab and being willing to put up with them are hardly the same. Industry CRADA partners quickly grew frustrated with what they perceived as a slow, unpredictable process that required a great deal of effort up front and little confidence that any request for joint work would be funded. Bills in both houses of Congress in mid-1993 aim at streamlining and shortening CRADA approval and negotiation, and the agency and labs continue to try to do so on their own. However, it may still be some time before the process can be brought down to DP's target of four months (if indeed it is done at all), from proposal submission tot he beginning of work, even if this Congress does pass a national laboratories bill. As long as t he process remains as lengthy and, from the standpoint of bidders, unpredictable as it is, companies may become increasingly disenchanted with working with the DOE labs at all, even with tighter R&D budgets.

BACKGROUND OF THIS REPORT

OTA was asked by Senator Hollings, in his capacity as chairman of the Senate Commerce Committee and subcommittee chairman of the Senate Committee on Appropriations, to examine how national laboratories could contribute to commercial competitiveness. The primary focus of the request was on two sets of institutions: laboratories that would be closed or downsized as a result of declining defense budgets, and laboratories that already are responsible for supporting commercial competitiveness. At the time, OTA **was** working on its assessment *Defense Conversion: Redirecting R&D,*[17] which focused mainly on potential cutbacks and new roles for the Department of Energy's nuclear weapons laboratories. Both houses of Congress were considering new roles for the DOE labs, and there was some concern that expanding their missions could create redundancies with other laboratories, particularly those of NIST.

[17] Ibid.

OTA agreed to examine these issues in a selected technology area following the release of *Defense Conversion.* OTA selected semiconductor technology and hired a contractor, Dr. A.S. Oberai, to assemble a team of industry, laboratory, and academic experts to assess the work and potential contributions of the three weapons labs (Livermore, Los Alamos, and Sandia National Laboratories) and NIST. This panel toured and talked with researchers in all four labs[18] and prepared draft sections of a report summarizing their findings.[19] OTA used that report, along with its own evaluations and investigations, to prepare this document.

POLICY ISSUES

Congress had two main concerns in requesting this work. One was that all federal laboratories position themselves to make more effective contributions to civilian technology development and competitiveness. Another was that unnecessary overlaps between the work of the DOE weapons labs, which are pursuing civilian technology development more enthusiastically than in the past, and NIST, which also is managing rapidly expanding missions, be identified and eliminated. In evaluating these questions, OTA identified several other policy issues that underlie the original two.

Management Structure

In a CRADA that involves both a company and a lab doing research and no money changing hands,[20] the private company manages its portion of the research, and the public lab manages its share. This is the case with most CRADAs underway at the DOE weapons laboratories and NIST. In the case of DOE, the agency shares with the lab managers (who are not civil servants) responsibility for overseeing the work of the weapons laboratories. This kind of management is appropriate for individual projects, but, for a larger, multi-institutional program aimed at a set of objectives as broad and challenging as the SIA roadmap, probably is not adequate to assure the most effective contributions on the part of any participant. Even within the private sector, broad-scale R&D efforts involving many companies—such as the work of SEMATECH or SRC—have management structures that supersede those of individual companies. R&D programs that include both government and private researchers in joint projects are rare (more typical is federal funding of R&D performed by private sector or university researchers), and there are few examples of an effective management structure for such an effort. If Congress wishes to allocate additional resources at the labs[21] specifically to pursue civilian semiconductor technology development, it could be well worth the effort to devise a new management structure.

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18 Properly speaking, NIST is not one laboratory, but eight. Most of the work relevant to microelectronics and semiconductor technology is carried on in NIST's labs in Gaithersburg, Maryland, and the panel convened in Gaithersburg to hear about and discuss all NIST's microelectronics work. For the purposes of this report, NIST is refereed to as one lab.

19 Oberai, op. cit. The draft and final reports of the panel were assembled and written by Dr. Oberai, using sections that were, in some cases, written by panel members. Neither Dr. Oberai nor OTA represents this contractor report as a complete consensus; there were many disagreements among panel members, and while most were worked out, a few remain.

20 Neither DOE nor NIST can pay for outside research through a CRADA. Some CRADAs involve industry, or another outside entity, writing a check for R&D done in a lab, but most DOE CRADAs and many of NIST's involve no exchange of money, The outside partner contributes in-kind R&D, and so does the lab.

21 This would include not only the DOE weapons labs and NIST, but possibly other government labs as well. This study could not include evaluations of all the public or government-owntxi, contractor-operated (GOCO) labs that might contribute to the SIA roadmap, but there are other promising candidates. In 1992, the Army Research Lab's Electronics and Power Sources Directorate signed 21 CRADAs with totat funding of nearly $4.4 million; some of this work maybe pertinent or adaptable to a government-wide effort to support civilian microelectronics technology development. So, too, is some of the work of MIT's Lincoln Laboratories, which has projects underway in advanced semiconductor technologies, mostly funded by the Air Force.

There is a range of opinion and options on what such a management structure should look like. At one end of the spectrum is the industry advisory panel approach, a model with which many in government are comfortable if not wholly satisfied. Advisory panels are common throughout the federal government, and they have the advantage of being a relatively quick way of getting feedback and advice on the conduct of federal programs from affected groups. However, few in the private sector care for this model, and some in government are growing more disenchanted with it. According to critics, advisory panel membership is unduly constrained by conflict of interest and financial disclosure regulations that often prevent those most interested from serving as advisors over a reasonable span of time. Another source of dissatisfaction, particularly as it applies in this case, is that advisory panels are just that: advisory. Agencies are free to disregard advice they don't agree with or would have a hard time carrying out, and while that may be appropriate in many instances, it is an unpromising approach for managing an extensive, government- and industry-wide effort to advance civilian technologies in the national laboratories.

Nonetheless, advisory panels have some attractions. More federal programs now aim at furthering private-sector goals, at least implicitly; without input and feedback from company representatives, it is hard for agencies to execute such responsibilities effectively. Where advisory bodies work well, agencies take seriously the counsel of the panels and yet are not unduly constrained by the wishes of the members, many of whom understand the public missions of the agencies imperfectly, just as federal managers often have a poor understanding of the exigencies of life in the private sector.

A somewhat different approach is being developed in the fall of 1993. Many in both the legislative and executive branches are interested in supporting semiconductor technology development that are broader than SEMATECH or other past programs, and better coordinated than previous federal-private technology development. The defense authorization bill under consideration in the Senate in summer of 1993 contains provisions for the expansion of the Semiconductor Technology Council, intended to foster precompetitive cooperation in technology development *among* government, industry, and academia, redirect existing federal semiconductor R&D, and evaluate opportunities for new R&D efforts. The Council's functions include:

- advising SEMATECH and the Secretary of Defense on appropriate technology goals for SEMATECH;
- exploring opportunities for improved coordination among industry, government, and academia;
- opening a dialogue on new technology challenges;
- identifying gaps or redundancies in existing public and private R&D programs;
- assessing the progress of existing R&D in terms of the goals of the technology roadmap, and helping to update and implement the roadmap; and
- making recommendations regarding the content and scope of federal semiconductor technology development.

Public officials[22] and representatives of industry and academia[23] would serve on the Council.

22 These would include the Under Secretary of Defense for Acquisition (co-chairman), the Under Secretary of Energy responsible for science and technology matters (a position that could be created in a couple of different ways in separate legislation), the Under Secretary of Commerce for Technology, the Director of the Office of Science and Technology Policy, the Assistant to the President for Economic Policy, and the Director of the National Science Foundation.

23 There would be four members prominent in the semiconductor device industry, one of whom would serve, with the Under Secretary of Defense for Acquisition as co-chairman; two members prominent in semiconductor equipment and materials industries; one member from the semiconductor user sector, and one member representing an academic institution.

While its role is nominally advisory, the seriousness with which both Congress and the administration are taking the effort to create it would likely give the group more power than a government advisory panel ordinarily has.

That power could evaporate, however, in an administration with a different outlook and goals. While there have been few precedents, the experience of the National Advisory Committee on Semiconductors (NACS) is instructive. Congress established NACS in 1988[24] "to devise and promulgate a national semiconductor strategy. ' Its powers were confined to evaluation and recommendation of actions on the part of Congress and the President, and like the proposed Semiconductor Technology Council, it had no other control over expenditures or policies. Like the Council, NACS drew membership from industry and government. NACS' policy recommendations were considerably broader than those envisioned for the Council. NACS addressed financial, educational, and trade policies as well as technology development, and it made recommendations regarding intellectual property protection and antitrust law and enforcement. NACS, in the succeeding four years, published several reports, many with strong recommendations for action, which were mostly ignored. In some cases, not acting on the recommendations turned out to have been prudent, or at least fortuitous;[26] in others, it might be that the industry would now be better off had NACS' options been enacted. The lesson is that advisory bodies with no other managerial power rely on goodwill and policy compatibility for their effectiveness, and these change.

Another management option would therefore be to construct some kind of public/private managerial body with greater power to affect the plans, programs, and fiscal commitments of any cooperative efforts to advance semiconductor technology aimed specifically at following the SIA roadmaps. SEMATECH was set up largely at the urging of the semiconductor industry, and while its funding was half public (through ARPA), the managerial control of the program has been largely in the hands of private-sector managers, though ARPA's influence has always been strong. ARPA has an order in place, in the form of a grant, that references and authorizes SEMATECH'S annual plan of work. ARPA has some input to the annual plan, both through SEMATECH'S six Focus Technical Advisory Boards (FTABs), which oversee various technology areas, and through a heavy schedule of meetings between SEMATECH and ARPA managers. At the working level, there is little tension between ARPA managers and SEMATECH representatives, but, according to one ARPA representative, there can be tension at the FTAB level, where ARPA sometimes views industry managers as having an excessively short-term outlook, while industry FTAB representatives have the converse view of ARPA managers.

Nevertheless, the process works, though not perfectly; compromises are forged and generally adhered to; moreover, SEMATECH itself has proven effective in helping the U.S. semiconductor industry regain some lost market share and improve the quality and competitiveness in several equipment sectors. Over its frost five years, SEMATECH grew to have closer relationships with ARPA managers, and ARPA representatives frequently attended meetings of SEMATECH's various technical advisory boards (figure 1-2). ARPA is not represented on these boards, but SEMATECH and ARPA planners meet extensively to develop technical plans for SEMA-

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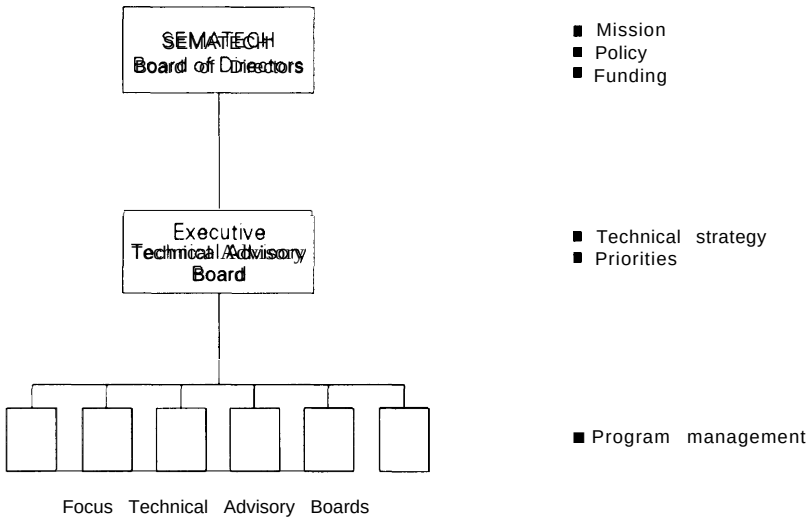
U Its organic act was the National Advisory Committee on Semiconductor Research and Development Act of 1988 (Public Law 100-410.

25 National Advisory Committee on Semiconductors, *A Strategic Industry At Risk: A Report to the President and Congress From the National Advisory Committee on Semiconductors* (Washington DC: November 1989), p. vii.

26 For example, NACS recommended aggressively pursuing synchrotrons x-ray lithography technology in 1989. In the succeeding few years, other forms of advanced lithography have shown as much or more promise.

Figure 1-2—Management and Coordination Structure for SEMATECH



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p. 67.

TECH's operation. ARPA's opinions are respected at SEMATECH, though its wishes are not always implemented. A prime concern of ARPA, for instance, has been what the agency views as SEMATECH's myopic concentration on near-term technologies; through years of interaction, ARPA and SEMATECH were able to agree that, beginning in 1994, SEMATECH would devote 20 percent of its funding[27] to longer-term strategic projects with new thrusts (design, test, packaging, and materials).

Using SEMATECH's management structure as a blueprint for management of a public/private research effort aimed at the SIA roadmap probably is both infeasible and impractical. The point of such a research effort is, after all, to develop techniques and technologies that, if they prove feasible, cost-effective, and robust, could be inserted in 5 to 10 years. SEMATECH's concerns are more immediate, and while nearly everyone agrees that SEMATECH is the best vehicle for disseminating technologies that are ready for commercialization, it may not be the best manager for longer-term projects. Moreover, it is very rare for private-sector managers to have as much control over as much public money as SEMATECH'S management has had, though the exception has been accepted in SEMATECH's case. For example, one factor that sets SEMATECH apart from a lab-based public/private program is that unlike DOE and NIST, ARPA funds but does not conduct research internally. Whatever the management structure of a civilian semiconductor technology development program, it is unlikely that a wholly or mostly private structure like SEMATECH's would prove acceptable to managers of federal laboratories, or to their agencies. Finally, R&D in the four labs is designed to fulfill both public and private missions. NIST is chartered to do projects aimed frankly at civilian industrial concerns, but even so, there are public missions that NIST must satisfy as well. The DOE weapons labs, in contrast, have until recently aimed almost all their microelectronics work at satisfying defense needs, and while some of it is clearly adaptable to

27 According to a representative of SEMATECH, this means 20 percent of the consortium's total budget, or $40 million.

civilian concerns, some is not. The end of the Cold War does not mean the end of the DOE labs' responsibilities for defense, and the agency and labs must continue to work on defense electronics. It is unrealistic to expect that DOE, or any other agency whose work could be used in both military and civilian applications, would be willing to turn over significant management of dual-use work to a private-sector team.

The same is true of MST. While NIST has a much longer history of serving civilian needs, some of NIST's work is fundamental science, intended to support the U.S. metrology infrastructure on a time scale beyond industry's immediate needs. NIST managers, along with others in the scientific community, feel strongly the need to protect the agency's freedom to engage in work deemed technically valuable, even if it has no near-term commercial application.

Nevertheless, some private-sector involvement consisting of more than just advice for efforts that *are* primarily aimed at meeting commercial needs is desirable in this case. Many options are possible, but would mostly be a departure from current practice. If Congress does allocate part of the effort of federal laboratories to cooperative work on the roadmaps as a public mission, some attention to devising such a management structure would be worthwhile. One option is, of course, to channel *some* responsibility for labs' work pertaining only to the roadmaps through SEMATECH. For example, it might be possible to invest SEMATECH with handling the handoffs of technology from labs (or lab/industry cooperative R&D) to industry when proofs of concept have been established, and the primary need is commercialization. If SEMATECH is to have broader managerial responsibilities, strengthening the influence and power of the federal agencies[28] in the program with SEMATECH might be desirable (though many in SEMATECH would oppose this). Another would be to put the management of such an effort under the guidance of the STC, or make one of the Council's duties the construction of an appropriate management structure. An intermediate option would be to devise new mechanisms whereby public or company managers could have stronger influence over program planning and funding for the cooperative efforts. Perhaps a public/private/lab management council could be created with a set of duties much like those of the Council, but greater power to influence funding or direction of research programs by voting, after carefully evaluating projects. That, in turn, depends on having a reasonable set of evaluation criteria established in advance, along with appropriate monitoring.

Focusing the Efforts of the Laboratories

OTA's panel of experts concurred that there is knowledge and technology in all four labs that could be (and often is) exploited or adapted by the civilian semiconductor industry. What is harder to agree on is how large an effort this should be, or how much of the potential trove of technology to attempt to develop specifically for the needs of the industry. To some extent, the question will answer itself, considering that any company has access to the labs' technologies through several avenues, including contract research, CRADAs, interactions among researchers, site visits, and publications. But that kind of access will not have the same results as a program targeting a few problems that the labs have the best shot at solving. Moreover, the possibilities of redundant projects arising at several labs are greater without an overall strategic focus.

Already, SIA has identified NIST as the primary developer of metrology technologies, and although many other labs can play supporting

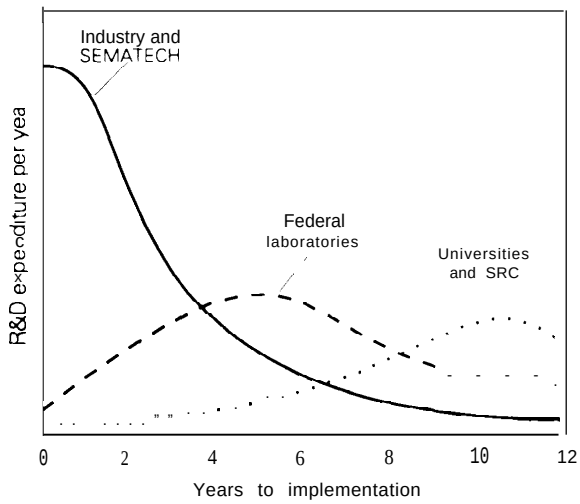
28 This would include all agencies with labs involved in an initiative specifically designed to advance civilian semiconductor technology. For the purpose of this report, those agencies include the Department of Commerce (or at least NIST) and DOE.

roles,[29] the choice of NIST as lead metrology lab is undisputed. However, there is little consensus now on which of the other laboratories should assume lead roles in other technologies, or even what those technologies should be. There is broad agreement that federal laboratories have a niche in research that is longer-term than industrial R&D and probably not as future-oriented as most academic R&D (figure 1-3), but within this broad framework we have yet to select the handful of initiatives that show the most promise of yielding commercializable results. There is a developing consensus that advanced lithography is an appropriate technology for DOE and other labs to pursue, though no lead lab has been named; a critical mass of opinion is also forming around equipment and manufacturing process modeling, environmentally conscious manufacturing, and cleanup. Again, however, while all the DOE weapons labs are pursuing programs in these areas, no lead responsibilities have been assigned.

If Congress is interested in authorizing a program of shared R&D aimed at furthering civilian semiconductor technology, one option is to select only a few key starting technologies from the plethora of possibilities and devote serious effort to designing appropriate responsibilities and management for them. A modest start might be frustrating to some, but it will be easier to build on a smaller, successful approach and the lessons learned than to make a grand entrance into a new business and risk many failures, always a possibility in a new program and a development almost sure to kill promising approaches as well as false starts.

Another important step is designating lead and supporting responsibilities among laboratories. Many of the talents and resources, particularly in the DOE labs, are complementary, and could be made to work in a synergistic way if managed properly. DOE headquarters is aware of this, and is trying to formulate appropriate managerial strategies. For example, in August 1993, DP officials were negotiating with SRC to coordinate the labs' work in advanced lithography. DOE is also interested in designating lead labs in technology areas that have garnered a great deal of outside interest. Such efforts are a good beginning, and encouraging them probably is wise. In the absence of higher authorities making some tough decisions about how the labs should coordinate and divide work on civilian technologies, there is a substantial risk that opportunities to capture synergies, or to focus the attention of the labs on the problems they are best able to solve, could be missed. There is competition among the labs, mostly among DOE weapons labs (and sometimes other multiprogram DOE

Figure 1-3-Federal Laboratories' Role in the Technology Development Cycle



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Lahs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p. 63.

[29] Sandia and NIST are already working together on semiconductor issues under a 1993 Memorandum of Agreement (MOA). Under the MOA, NIST has agreed to develop supporting metrology and associated technology for advanced semiconductor manufacturing tools, assure purity and assess the composition of materials, and assure manufacturing process reliability, Sandia will develop technologies to eliminate contamination, work on developing lithography tools, assist with modeling the next generation of semiconductor products, and provide access to the Center for Microelectronics Technologies (CMT) to serve as a testbed.

labs), but labs affiliated with other agencies are in some cases vying for "their" share of precious budget dollars. Some competition is healthy, but, especially in today's tight fiscal environment, the dangers of unchecked competition probably outweigh the merits.

Evaluation Criteria

Increasing competition for R&D funding, federal and private, has bolstered the case for development of good performance criteria. R&D is notoriously difficult to evaluate properly. Input measures--e.g. dollars or FTEs[30]--are often the most readily available measures, but they fail to capture the quality or usefulness of the R&D. Output measures, often including data or estimates of the commercial impact of technologies, or return-on-investment calculations, are unalterably judgmental, and are therefore subject to manipulation or bias. Frankly judgmental approaches, such as Delphi techniques, compensate partly by relying on many evaluators, and presumably some of these cancel out; however, research and development communities are still subject to penchants and fashions, despite the reverence of scientists for objectivity. None of this means that thorough, rigorous evaluation of R&D can be avoided; it means that evaluation criteria must be developed carefully, applied rationally, and amended as necessary.

The OTA review panel devised two sets of criteria-one for DOE labs, one for NIST--to use in evaluating whatever R&D programs were undertaken (box l-C). The panel envisioned a phased approach to the DOE labs' studies aimed at the roadmap. Phase 1 projects include concept or exploratory work, usually averaging $1 million to $3 million in size, and aimed at producing technologies whose commercialization could begin 6 or more years in the future. The panel envisioned these as designed to be synergistic with university-based research efforts managed by SRC, to the extent feasible. Examples might include laser doping, nanometer stage investigation, and low-damage etch processes.

Phase 2 projects would examine technical and commercial feasibility. These projects would average $3 million to $10 million, and aim at producing technologies for commercialization three to six years out. Phase 2 projects would be expected to have industry participation (both in conducting and funding the studies), perhaps through SEMATECH. The result of a typical Phase 2 project would be a preproduction prototype technology, such as a lithography tool, a contamination-free manufacturing system, or TCAD (technology computer-aided design) software. The third phase, insertion and implementation, would involve industry much more than labs, both in terms of time and expenditure (see figure 1-4). Phase 3 projects would develop applications of generic skills or capacities to solve identified problems on an as-needed basis. Some of the key evaluation criteria, which the panel called 'return on investment, " address how many projects progress from Phase 1 through 3.

These two sets of criteria were apparently acceptable to OTA's panel, and might serve as interim measures. In OTA's view, however, the two sets of evaluation criteria are mismatched enough that further effort to develop a more consistent set might be warranted. As the lists stand now, DOE's criteria are mainly output- or process-oriented, while NIST's resemble goal or mission statements more than evaluation criteria, with little obvious avenue for feedback other than that provided by MST's ongoing advisory committees. The lack of more explicit measures of performance could be a concern, especially under an expanded, interagency program of cooperative R&D. Conversely, the criteria as written for NIST give it a very tough assignment, one that might not be manageable within the agency's budget in a time of tight fiscal discipline.

30 Full-time equivalents, a measure of Staff time.

Box l-C—Evaluation Criteria for National Laboratories

Criteria for DOE Laboratories

- **Industry is involved with the labs and vice-versa. Measures could include:**
  - **—Number of companies providing resources to the lab programs.**
  - **-Companies contribute dues (>$10,000) to acknowledge access to the labs' consulting capability.**
  - **—Reasonable attendance (>70%) at quarterly update meetings.**
  - **—More than three companies provide significant resources per program.**
  - **-Co-principal investigators from the industry.**
  - **—Significant fraction (>30%) of the work done at industry sites.**
- **. Positive return on investment. Measures could include:**
  - **—>20% of Phase 1 programs move to Phase 2.**
  - **—>25% of Phase 2 programs are commercialized.**
  - **—Principal investigators are measured on executing and transfer of technology.**
- **. Mechanisms are established to ensure that programs can be killed if industry doesn't want the technology.**
  - **-Multi-year programs are projected in one-year stages for easy reset.**
  - **—Industrial partners are signed up within three years.**

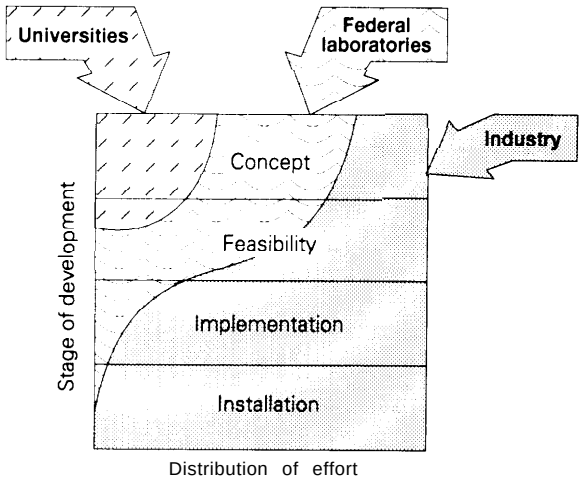
Criteria for NIST

- **Measurement techniques are provided for all key steps of future semiconductor processing (examples: gate oxide thickness, photolithography critical dimensions and overlay, contamination levels, device profiles).**
- **Standards and services are provided so that industry can calibrate their measurements with NIST.**
- **. Data are supplied for characterization and validation of the various process, device, and package technology needed to implement the national roadmaps.**
- **. Where appropriate, NIST provides services to allow the laboratories and industry to do measurements that would allow participants to compare their performance to that of other participants.**
- **Program plans reflect the needs and timing of the national roadmap and are kept up to date.**

While many of the specific measures suggested for the DOE labs may not be appropriate for NIST, the generalized criteria-significant contact among lab and industry researchers in projects, positive return on investment (not necessarily measured financially), and mechanisms to insure program termination if the technology turns out to be useless to industry--are appropriate as a starting point in developing a more consistent list.[31] It would also be useful to

[31] Many lab representatives are, however, concerned about the last criterion (measures to terminate programs when industry is 'ot interested in the technology). Most argue that this provision must be strongly tempered by the labs having flexibility to pursue public missions (including advancement of basic sciences, national defense, energy conservation, and the like) even when industry does not foresee commercial applications. Also, NIST reviewers point out that many of the criteria suggested for DOE labs are already used at NIST, de facto if not formally, There is, according to NIST, already extensive contact between lab and industry scientists and engineers; many NIST projects have been evaluated in terms of return on investment; and mechanisms are in place to assure termination of unuseful programs.

Figure 1-4—Roles of Universities, Federal Laboratories, and Industry in Development of New Technologies



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p. 59.

consider adding standards for project selection, as well as process and output measures. The task of developing appropriate criteria for anew program of public/private R&D, unusual as such undertakings are, could be daunting, and could require special effort. Several organizations could be directed to look into the matter broadly (e.g., developing criteria for all publicly funded R&D aimed at commercial applications) or narrowly (developing criteria for any special program dedicated to advancing commercial semiconductor technologies). Possibilities include the National Academy of Sciences, creation of a special commission or blue-ribbon panel for the purpose, or (narrowly construed) the Council.

Assuring Effective Hand-offs

The success of the whole public-private cooperative R&D effort depends on there being strength on both sides of the relationship. Researchers from labs, industry, and universities must have frequent and close contact, and all parties must work to accommodate everyone's concerns and objectives in program planning and execution. This is less likely to happen if one of the partners is weak.

The American semiconductor industry and the materials and equipment industries that support it have had a turbulent decade. Still considered globally dominant in the late 1970s, the industry lost share rapidly in the 1980s in most market segments, mostly to Japanese manufacturers. Since the late 1980s, the industry has revived to some extent, mostly due to private-sector efforts but also due to a couple of government programs, including ARPA's funding half of SEMATECH and (though some would dispute this) the Semiconductor Trade Agreement with Japan (see ch. 3). The improvement can be measured in such terms as the U.S. global share of merchant semiconductor production,[32] which turned up in 1990. Similar upturns occurred in several equipment sectors as well. All analysts caution that some of the upturn in market shares of U.S .-based producers is attributable to the fact that the Japanese market, which Japan-based producers heavily dominate, has undergone a deeper and more protracted recession than the United States in the 1990s. However, there is also a broad consensus that the industry's revival is also due to more sustainable bases, like better technology and greater control and understanding of manufacturing processes.

Several areas remain weak, however. One of the key weaknesses is in lithography equipment.[33] Lithography, according to SIA, is ''both the dominant cost factor in wafer processing and the driving technology for increasing chip functionality and, hence, is the primary pacing tech-

32 Semiconductor sales are commonly measured in terms of merchant and captive sales. Merchant producers are those who sell semiconductors or devices to users, often systems makers; captive production is intrafirm production in vertically integrated companies.

33 Lithography is the process by which a pattern is formed in a photosensitive coating that covers a substrate. (SIA, 1993, op. cit.) In semiconductor production it is used to pattern the lines connecting various devices on a chip.

nology for industry progress."[34] Yet the U.S. lithography equipment industry has grown weaker over the past decade, going from a 90 percent global market share in 1981 to 10 percent in 1991.35 Concern for maintaining a domestic industry mounted recently as one of the three U.S. companies in the business, GCA, was offered for sale by its parent firm (General Signal) and, when no buyer made an acceptable offer, dissolved. SEMATECH had, for several years, invested millions of dollars in GCA, and SEMATECH experts worked with the company to improve its equipment. Many agree that these efforts met with technical success; GCA's machine, by 1992, was technically comparable to or slightly better than its competition. However, the company still failed.[36] While many in the industry attribute at least some of the failure to management problems at GCA or its parent company, General Signal, it is also true that lithography equipment is a very hard business to stay in, even for a well-managed company. It demands millions of dollars' worth of R&D every year, has a limited market, and is subject to exceptionally fast technological obsolescence. The two Japanese companies that dominate the business, Nikon and Canon, are large,[37] horizontally diversified, and vertically integrated, which means that they can cross-subsidize investment-hungry segments like lithography with the profits from less-demanding segments. Added to that is the fact that, for several decades, capital costs have been lower and investors more patient in Japan than in the United States. Considering too the technical excellence of the Japanese companies, it is easy to see why the lithography equipment business has been so tough for American companies.

There are two left: SVGL (Silicon Valley Group Lithography) and Ultratech Stepper.[38] Ultratech has carved out a market niche in the l-micron range, which is not state-of-the-art in line width resolution but satisfies the requirements for most of the 25-30 lithography steps currently required in most semiconductor production. The only American company that still is a player on the cutting edge of line-width technology in lithography is SVGL. SVGL resulted from the Silicon Valley Group's purchase of the lithography business of Perkin Elmer, once a prominent manufacturer of lithography equipment. SVGL's new technology, Micrascan, is reportedly very good, and may hold promise for the next generation of semiconductor technology.[39] But SVGL is a small company competing against larger, better-established businesses with deserved reputations for technical excellence and outstanding service. If Micrascan technology does not sell adequately in the next couple of years, SVGL could go the way of Perkin-Elmer and GCA, leaving the world with three stepper companies (Nikon, Canon, and the European company ASM), barring new entrants. SVGL has also received funding and assistance from SEMATECH and its members, and the effort, along with SVGL's own expertise, has apparently yielded good interim technical results. But SVGL is in the midst of licensing MicraScan technology to Canon, reportedly in return for licensing fees and some

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34 SIA, op. cit., p. 8.

35 Semiconductor Industry Association, *Semiconductor Technology: Workshop Working Group Reports* (San Jose, CA:1993) p. 36.

36 In 1993, there was some interest in Congress and the Executive branch in mounting a rescue effort for GCA. By this writing, in fall 1993, the company remains defunct, and the passage of time will only increase the difficulty of revival.

37 One company official compared Canon and Nikon to their American competition by saying, "The R&D budget of Nikon is bigger than the annual sales of [the American companies]."

38 There are also several companies exploring advanced lithography, but SVGL and Ultratech are the only producers of optical lithography equipment in the United States.

39 The current generation of leading-edge lithography technology makes line-widths as small as (). 35 microns; the next generation, expected to come on line in the late 1990s, is expected to be 0.25 microns.

help from Canon with manufacturing technology.[40] With the disparity in the size, market power, and experience of the two fins, many knowledgeable observers are concerned that SVGL may not survive more than a few years.

In many equipment industries-for example, many segments of the textile equipment industry—loss of domestic suppliers has not proven much of a competitive handicap for American firms. In others, the loss of competence and market share in equipment has cost downstream manufacturers dearly. Semiconductor equipment is probably one of the latter. Semiconductor technologies change rapidly, and close relationships with equipment manufacturers are important considering that a few months' lead in installing, debugging, and producing using new equipment can mean a significant edge in market share. Many American equipment suppliers once maintained close relationship with semiconductor and systems producers, relying on customer feedback to help design new equipment and develop new technologies, but as competitive pressures took a toll, many of these ties were frayed. SEMATECH, and its close partnership with the equipment suppliers association (SEMI), helped to restore the productive ties of equipment and chip manufacturers, even in lithography equipment. But unlike in other segments, the efforts in lithography missed the mark. Many reasons for that miss have been advanced; some say that GCA's machines were too late, becoming available later than promised and after major semiconductor manufacturers had made purchasing commitments for the current generation of technology. Some regard GCA's business plans as weak and the fact that CGA's new machines failed to find enough buyers is attributable to a lack of confidence in the company's longevity (if true, of course, this amounted to a self-fulfilling prophecy). Canon and Nikon, in contrast, are regarded as reliable, competent companies. Whatever the reason, GCA's failure and SVGL's modest position in the market mean that the American stepper industry is still weak, even after a great deal of public and private effort has been devoted to strengthen it.

There is, as usual, a wide range of opinion on what to do. Some would do nothing, assuming that foreign suppliers will go on being as competent and reliable as they have been. But to others, the issue of relying heavily (perhaps exclusively, depending on ASM's performance in the next few years) on two suppliers, and Japanese suppliers in particular, is worrisome. While European semiconductor manufacture has struggled for years to gain a larger toehold on global markets, Japanese competition in semiconductors has improved at an impressive pace. Japanese merchant semiconductor manufacturers held a larger share of the global market than American merchant producers until 1992, and the gap has been narrow in the last couple of years. Canon and Nikon are often reported to have closer relationships with their Japanese customers than with most of their American customers, for obvious historic, geographic, and cultural reasons. Some openly doubt that American firms get equipment as early, or can command the responsiveness to technical adjustments, that their Japanese customers get from Nikon and Canon. Mostly because of the uniquely interconnected networks of businesses that characterize much of Japan's economy, some worry that dependence on Japanese suppliers in particular, and especially in so important a sector as lithography equipment, could be a significant competitive disadvantage.

Public policy has seldom dealt with such issues particularly well. No government department can wield the kind of influence over ongoing business plans and decisions that Japan's Ministry of

[40] The licensing agreement between Canon and SVGL is under review at SEMATECH, and not publicly available as this report is being written. The terms of the agreement as written above arc what many knowledgeable observers believe to be contained in the agreement. According to one source, not only Micrascan technology but the 193-nanometer process, which has even freer resolution and was originally developed at Lincoln Laboratories, is also part of the agreement.

International Trade and Industry (MITI) could when the **Japanese** semiconductor industry and its attendant equipment sectors were weak. Even if it were possible, differences in situation and environment between the United States now and Japan in the 1960s and 1970s probably make the actual public policy decisions of Japan a poor guide. If, as much of the industry's own analysis indicates, lithography equipment is a key sector in which to maintain strength, it would be prudent to consider all the steps necessary to build that strength. Technology policy is almost never enough, by itself. Though it is not the purpose of this report to examine all the policy choices with respect to key, but weak, sectors, this consideration should be prominent in decisions regarding how the labs can contribute to lithography, and other sectors like it. In short, Congress might wish to consider creating a commission of experts drawn from academia, industry, and government, to analyze key factors that account for the decline of the stepper manufacturing sector in the United States, and to list attendant policy recommendations. This option becomes even more important if the United States continues to support development of advanced lithography technologies, as it has done for many years,

Several agencies have lithography R&D efforts underway. ARPA has supported advanced lithography to the tune of $75 million in earmarked funds in FY 1993, plus SEMATECH's expenditures on lithography; DOE weapons labs have R&D efforts underway to support their own missions, and NIST has programs designed to permit the domestic semiconductor industry to use lithographic equipment effectively. While most of the work done in the past was in optical lithography, SIA expects some radical shifts in lithography over the next decade or so; examining new approaches to lithography will certainly require tens of millions of dollars (and maybe more) annually for several years, Some of the needed R&D in advanced lithography will be carried on by industry,[41] but exploration of new concepts in lithography (advanced optical, projection and proximity x-ray, e-beam, ion projection, and massively parallel direct write) will not be supported by the private sector at a level sufficient to have any assurance of strength in lithography by the turn of the century.

There is keen interest, both in the labs and in the private sector, in continuing government funding of advanced lithography research. Many approaches are being explored; most are far from even being in the development phase. Research is needed to bring one or more to the proof-of-concept stage, or to the point where industry is willing or able to invest more heavily in technology development and commercialization (under the assumption that we are unwilling to risk dependence on foreign stepper suppliers). To support exploratory work in lithography alone, at a level sufficient to give a reasonable chance of having alternatives available as semiconductor line-widths narrow below 0.2 microns, will require tens of millions of dollars of public funding over the next several years, in addition to what is already being spent on lithography. An examination of the scope, purpose, and performance of lithography research being done by government agencies would also be in order; the investment of new money might be smaller if some existing work could be adapted (without compromising public missions) to better meet the needs of commercial stepper technology development. Explicit coordination mechanisms for a multiagency program might also be in order, including DOE, DoD, and NIST at a minimum. Finally, it is worth remembering that even if adequate funding and coordination are established to advance lithography technology, these may not be enough to assure that American companies are represented in the stepper business, or that American consumers of steppers can reap the benefits of public

[41] For example, four companies—Jamar, Ultratech Stepper, Intel, and AT& T/Sandia-have CRADAs with Livermore working on soft x-ray lithography.

funding of advanced lithography research. Exploration of additional policy approaches to rebuilding a domestic industry might be warranted, especially if public resources devoted to lithography research are significantly expanded.

Funding[42]

None of the four labs being considered in this report has adequate funding, under current circumstances, to handle the new responsibilities possible in a public/private program to advance commercial semiconductor technology. In order to devote resources sufficient to make much of a difference, all of the four would have to either have new money or redirect ongoing research. Some redirection may be possible, especially at the DOE labs, where missions are changing as a result of the end of the Cold War and cuts in military programs. Even there, however, the dividend available from cutbacks in nuclear weapons programs is commonly overestimated (barring a revision and reorganization of the labs' defense responsibilities more extensive than anything yet done or underway). A close examination of whether redirecting existing research in the four labs, or even government-wide, could serve commercial needs adequately without compromising public missions could be valuable, but there is a strong possibility that the answer will be no.

All four labs have many interests and projects competing for available resources. NIST has had some appropriated funding for semiconductor metrology R&D, but the combination of increasing demand for metrology support across a range of emerging technologies and federal budgetary constraints have made it impossible to fully fund the lab's requested budget during the last two administrations. DOE's CRADA program, while it is not the only or the best answer to cooperative R&D, serves as a useful example of funding bottlenecks. DOE's CRADA program has grown very rapidly for a new program, from $1 million in 1990 to probably more than $200 million in FY 1993.[43] The rapid expansion, along with the program's high visibility,[44] made the new activities difficult to manage. DOE's DP, which controls the largest share of CRADA funds, has also devised a proposal screening and selection process that, though aimed at worthy objectives like minimizing redundancy and reinforcement of the core competencies of various labs, has proved cumbersome and opaque. Equally frustrating to many companies interested in CRADAs is the amount of time it takes to negotiate an agreement after the approval is granted. Throughout 1992 and 1993, it has taken about four months for DP to approve proposals, and another four months to negotiate a CRADA (a process in which the lab takes lead responsibility, guided by DOE field offices). One reason for the lengthy selection process is that DOE has been peppered with proposals, so that even with the relatively generous funds available, the agency probably funds many fewer than one in ten proposals. At the beginning of 1993, about half the money available for CRADAs in DP ($71 million) was already committed to ongoing projects, and proposals approved in early November (which had been submitted in the previous fiscal year, in the June 1992 call for proposals) accounted for approximately $40 million more. That left only

42 For an expanded discussion of funding issues associated with cooperative R&D at the DOE labs, see U.S. Congress, Office of Technology Assessment, *Defense Conversion: Redirecting R&D,* op. cit., pp. 110111.

43 Defense Programs at DOE, which has more money for CRADAs than any other division, has a $141 million appropriation set aside for cooperative R&D at the weapons laboratories. One other division, Energy Research, also has a setaside for CRADAs; other divisions fund cooperative R&D from program funds.

44 The program's visibility was the result of many things. One was the National Technology Initiative, a I@ agency program launched in 1992 to acquaint potential cooperators (universities and industry) with the opportunities for technology transfer and joint R&D at federal laboratories. Another was the fact that DOE's weapons laboratories are, by substantial margins, the nation's largest, and up until recently, least known. Their nuclear weapons missions makes anything they do controversial.

about $30 million for proposals submitted in late 1993 and approved in spring of 1994. There was very little or no set-aside money for CRADAs left in DP after spring. In fact, there has been very little flexibility for DP to fund CRADAs with set-aside money throughout FY 1993, considering that the last call for proposals (which used up all but the dregs of the $141 million) was in late 1992. Several semiconductor manufacturers and semiconductor equipment manufacturers were already working with the weapons labs, or had negotiations underway, but interest in shared research was also burgeoning in spring of 1993, just when funding was drying up. Even at NIST, where CRADA executions are straightforward and swift, trying to initiate significant amounts of new work in one industry area might prove problematic, given the amount of cooperative work NIST researchers already maintain (NIST reports that it has one CRADA for every four full-time researchers).

The above illustration is not meant to imply that CRADAs are the only, or even the best, avenue for the labs to contribute to technology development. The time and trouble that it has taken to begin a DOE CRADA has soured many industry representatives on the whole process, and many would prefer to use other mechanisms if a new semiconductor technology initiative were begun. However, unless additional money is made available (through appropriation or internally, with agency program funds) for cooperative R&D and earmarked for semiconductor work, funding will remain an obstacle.

Overlap

Currently, there is little concern about redundancy among the four laboratories' work in microelectronics. In some cases, the labs' core competencies are described in similar terms, but on closer evaluation the specifics of the work are sufficiently different that overlap problems have not arisen. Some of this is due to differences in lab missions--NIST's primary function is to provide metrology, and its major target audience is civilian industry, while the DOE weapons labs' missions have concentrated on a variety of other sciences and engineering, primarily for military applications and secondarily to meet the nation's energy goals. Livermore and Los Alamos were originally designed to compete and to complement each other's work in physics and nuclear science, but even there, the differences in what they have done and can do best to advance semiconductor roadmaps are more striking than the similarities.

If the labs' semiconductor work were significantly expanded, redundancy could become more of a problem, however. The most expeditious way to avoid redundancy would be to create, along with expanded authority to pursue civilian microelectronics R&D, the kind of management structure described above. Frequent communication among labs, companies, and universities cooperating in such an effort can be an effective way of assuring that needless overlap (some overlap is good) is avoided.

Laboratory Capabilities; 2

The Department of Energy's weapons labs (Sandia National Laboratories, Lawrence Livermore National Laboratory, and Los Alamos National Laboratory) and the Department of Commerce's National Institute of Standards and Technology (NIST) offer potential for improving the competitiveness of U.S. semiconductor manufacturers and their suppliers. All four labs have developed strong competencies in areas the Semiconductor Industry Association (SIA) has identified as critical to the future success of the U.S. semiconductor industry, such as lithography, modeling and simulation, environmental safety and health, and equipment design. In 1993, the four labs devoted resources valued at approximately $115 million to cooperative research and development agreements (CRADAs) with the commercial semiconductor industry.

At present, the labs' work with industry is fragmented, consisting of numerous small projects that build upon the capabilities of individual researchers or research groups. However, each of the labs appears to have strong capabilities in particular subjects that could become focal points of their efforts to support the commercial semiconductor industry. NIST is clearly the leader in most areas of metrology; Sandia has particular capabilities in equipment modeling and design, as well as in contamination-free manufacturing; Los Alamos is strong in both the modeling of semiconductor devices, manufacturing processes, and complete factories, and in environmental safety and health; Lawrence Livermore has particular expertise in soft x-ray lithography and materials processing. Already, the labs are beginning to pursue leadership roles in some areas and coordinate their research with the other labs, industry, and universities.

Integrating the labs more closely with industry will not be easy, though. DOE labs are new to commercial missions and do

not operate with the same cost considerations or time horizons as commercial companies. Such cultural differences are likely to cause frustration in joint R&D programs between industry and the labs. Industry has already found negotiating CRADAs with DOE labs slow and laborious. In addition, the labs have only limited experience with the most advanced commercial practices for manufacturing integrated circuits (ICs). While Sandia has manufactured ICs for defense applications and NIST has provided support in metrology (the science of measurement) to the commercial IC industry for several decades, the labs as a whole have not been operating on the leading edge of commercial IC production. Los Alamos and Lawrence Livermore boast strong capabilities in simulation and modeling, but do not have extensive experience applying these strengths to commercial semiconductor processes and factories. It may therefore take some time before their contributions to commercial industry become evident in the marketplace.

LABORATORY/INDUSTRY COLLABORATION

Both the DOE weapons labs and NIST offer significant, and complementary, capabilities to aid the U.S. commercial semiconductor industry, While these are not the only federal laboratories with capabilities of interest to the semiconductor industry, they are, for several reasons, the labs most likely to contribute to commercial missions in the near term. First, with the decline in nuclear weapons work, the DOE labs may be given new missions to assist commercial industry through technology transfer and cooperative research and development,[1] They are already being encouraged to work more closely with industry through CRADAs. Second, NIST has a long history of working with industry to develop and disseminate new standards and measurement methods. In the last decade, NIST has been given new responsibilities to support manufacturing extension programs and commercial technology development.

DOE Labs

The Department of Energy Defense Program Laboratories (or weapons labs) were created to develop nuclear weapons technology. In fulfilling this mission, the weapons labs developed diverse science and engineering capabilities for producing, testing, and ensuring the safety of the nation's nuclear deterrent. These capabilities, which include specific competencies in physics, chemistry, materials science, engineering, and computer science (box 2-A), now form the basis of the DOE labs' ability to help improve U.S. industrial competitiveness in the semiconductor industry.

The weapons labs have experience in nearly all stages of technology development, with the notable exception of full-scale commercial production. The labs invented a complete design and manufacturing process, beginning with detailed nuclear and atomic physics and extending through systems integration, for both the nuclear and non-nuclear components of the weapons systems. Each of the labs played a specific role in the process. Los Alamos and Lawrence Livermore were chartered to understand the physics of nuclear devices and to develop materials technology in support of the weapons program. Sandia National Labs was directed to develop the science and engineering skills required for the non-nuclear portion of nuclear weapons systems, including custom and radiation-hardened ICs and other electronics.

The weapons labs may be best-suited to address research problems that are in the middle of the development cycle-between basic research and product development—and that com-

[1]Two bills currently under consideration in Congress, H.R. 1432 and S.473, direct the DOE labs to work more closely with industry. The House bill restricts DOE to missions in nuclear weapons, defense, energy, and environmental remediation, but encourages greater technology transfer and cooperative R&D. Tbe Senate bill includes a broader mission statement that explicitly charters the labs to conduct programs of industrial R&D.

Box 2-A—Core Competencies of DOE Weapons Laboratories

Lawrence Livermore

Applied physics, chemistry, and materials science
- Plasma, solid-state, and atomic physics and chemistry
- Synthesis and processing of metal and alloys, ceramics, and organics
- Surface science and processing, adhesion and bonding, microstructural science
- Chemical kinetics and synthesis
- Superconductivity, materials and mechanisms
- Nuclear chemistry
- Materials characterization via synchrotrons radiation, accelerator mass spectrometry, electron and scanning microscopy, positron spectroscopy, etc.

Measurements and diagnostics
- Plasma and high-temperature diagnostics
- Surface diagnostics
- Sensors and detectors
- Data capture, analysis, fusion, and control
- Process monitoring and control
- X-ray micro- and macro-tomography

Computational science and engineering
- Modeling of solids, fluids, atomic structure at micro and macro scales, under normal and extreme conditions
- Constitutive models for complex materials processing
- Quantum chemistry, lubrication and bio-molecules on surfaces
- EM circuit and electro-optic device design
- Electricity and magnetism in 3-dimensional Maxwell's equations solvers with complex boundary conditions
- Scientific visualization
- Imaging and signal processing

Microelectronics and photonlcs
- High-density, high-performance chip packaging (multichip modules)
- High-speed electrical and optical data transmission
- Materials and systems reliability
- Band-gap engineering and verification
- Gas immersion laser doping (GILD)
- Display technologies
- High-speed electromagnetic and optical circuit modeling, test, and diagnostics

Lasers, optics, electro-optics
- Soft x-ray lithography systems: x-ray sources, optics, and materials
- High-power/high-radiance solid-state lasers
- High-power semiconductor laser arrays
- Optoelectronics design and development
- High-power optical fiber transport
- Laser processing of materials

Manufacturing
- Precision engineering
- Metrology
- Advanced design and process engineering
- Computed tomography and ultrasound
- Non-destructive evacuation

Engineered materials and processes
- Modellng, production, and metrology of multi-layer and epitaxial materials
- Advanced low- and high-dielectric materials
- Atomic, ionic, particle, and photon beam materials processing and modeling
- Plasma processing-modeling and validation of processing methods
- Aerogels, zerogels, and solgels
- Microstructure: microchannel coolers, actuators, sensors, and micro instruments
- Molecular dynamic modeling of machined and deposited microstructure

Atmospheric and geosciences
- Seismology and imaging
- Geochemistry
- Global climate and transport modeling
- Transport measurements, atmospheric chemistry

Defense sciences
- Nuclear system design
- Scientific computing of massive problems with disparate time and distance scales
- Energetic materials and conventional munitions
- Nuclear measurements and design validation under extreme conditions

Blosclence/Biotechnology
- Genomics
- Physical biology
- Analytical cytology
- Synthetic and natural biomaterials sciences
- Micro-instruments and sensors

Environmental science and technology
- U.S. and California compliance and remediation expertise
- Measurements and sensors
- Remediation technologies
- Process developments
- Bio, chemical, and radiation dosimetry

(continued on next page)

Box 2-A–Core Competencies of DOE Weapons Laboratories-Continued

Sandia

Microelectronics and photonlcs
- IC design, fabrication, and test
- Advanced lithography
- Reliability physics and engineering
- Advanced packaging
- Compound semiconductor and strained-layer semiconductor technology
- Optoelectronics and photonics
- Lasers, laser arrays, and associated technology
- Compound Semiconductor Research Laboratory

Engineered materials and processes
- Synthesis and processing of metals, ceramics, and organics
- Characterization and analytical technique development
- Theory, simulation and modeling of materials and processes
- Melting, casting, and joining
- Chemical vapor deposition and plasma deposition
- ion beam processing and analysis

Pulsed power
- intense particle beam physics
- High-speed switching
- Intense x-ray physics
- Radiation effects simulation
- Plasma and electromagnetic theory and application

Physical simulation and engineering sciences
- Combustion sciences
- Geological sciences
- Experimental mechanics
- Solid and structural mechanics
- Radiation transport and above-ground radiation testing
- Diagnostics and instrumentation
- Fluid and thermal sciences
- Nondestructive evaluation
- Environmental testing and engineering
- Research reactor engineering and experimentation

Computational simulation and high-performance computing
- Massively parallel computing
- High-performance scientific computing
- Quantum chemistry and electronic structure
- Computational hydrodynamics, mechanics, and dynamics
- Digital communications and networking
- information surety
- Development and application of intelligent machines
- Signal processing

plement the R&D capabilities of industry and universities. The labs have the capabilities and the facilities necessary to conduct applied research programs and to develop prototypes of new systems for demonstration/validation purposes. This is a mission that industry has slowly retreated nom, universities have not yet ventured into, and government rarely supports,

Each of the labs has managed and executed large-scale programs requiring large facilities, high levels of funding, and multidisciplinary scientific expertise. Together, the labs managed an operational budget of $3.4 billion and employed almost 25,000 people in 1993. Their technical staffs employ more than 11,500 workers, over one-third of whom hold Ph.D. in fields such as physics, chemistry, engineering, mathematics, and computer science (figure 2-l).

Furthermore, the weapons labs are gaining experience in working with industry. Since 1989, all DOE labs have begun programs of cooperative R&D with industry. Though implementation of CRADAs has been slow and frustrating, the three weapons labs had signed 179 CRADAs as of May 1993, totaling over $235 million of in-kind laboratory contributions.[2] Many of these agree-

[2] U.S. Congress, Office of Technology Assessment, *Defense Conversion: Redirecting R&D,* OTA-ITE-552 (Washington, DC: U.S. Government Printing Office, May 1993), pp. 104-105.

Box 2-A—Core Competencies of DOE Weapons Laboratories-Continued

Los Alamos

Nuclear technologies
- Nuclear weapons design
- Reactor design and safety analysis
- Nuclear medicine
- Nuclear measurements

High-performance computing and modeling
- Global environment (climate change, etc.)
- Computational test bed for industry
- Massively parallel processing
- High data rate communication
- Traffic modeling
- Visualization

Dynamic experimentation and diagnostics
- Arms control/verification
- Global environment
- Neutron scattering
- Measurement of explosive phenomena
- Light detection and ranging for atmospheric measurements

Theory and complex systems
- Human genome
- Traffic simulation
- Neural networks
- Non-linear phenomena

Advanced materials and processing
- Plutonium processing
- Manufacturing process analysis
- Materials modeling (material by design)
- Polymers
- Ceramics
- Metallics
- Composites

Beam technologies
- Accelerator transmission of waste
- Laser diagnostics
- Materials characterization
- Photonics
- Photolithography (x-ray sources)
- Neutron beam chemistry and physics

Systems engineering and rapid prototyping
- Transportation systems
- Environmental and energy systems analysis
- Lasers manufacturing
- Accelerator systems

SOURCE: Lawrence Livermore National Laboratory, Livermore, CA; Los Alamos National Laboratory, Los Alamos, NM; Sandia National Laboratories, Albuquerque, NM.

ments cover R&D in fields related to semiconductor technology.

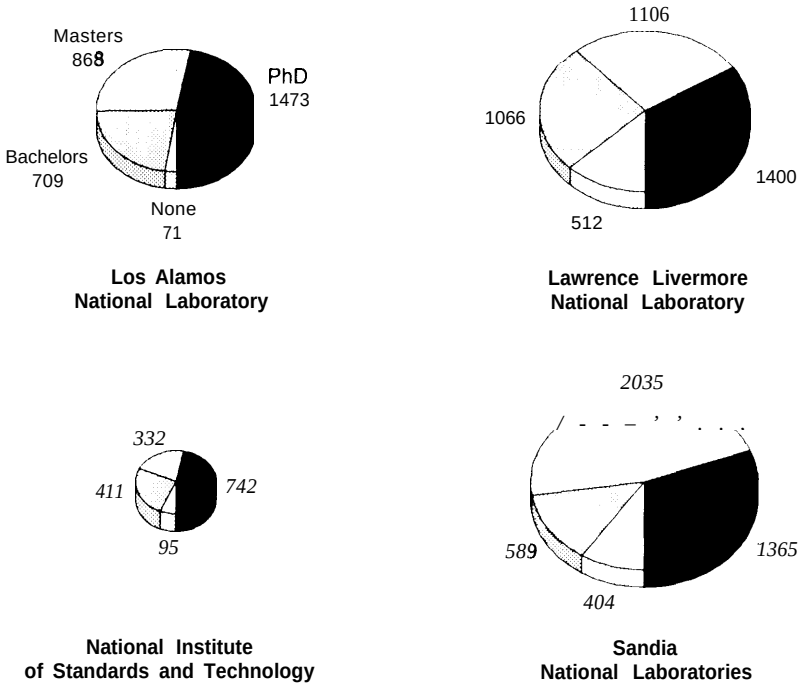
With declining defense budgets, the labs may be able to dedicate more of their resources to nondefense problems. Already, the portion of their budgets directed to defense has fallen. In 1993, defense activities at Los Alamos comprised 71 percent of its total operating budget, compared with 78 percent in 1987; at Lawrence Livermore, defense activities dropped to 67 percent, down from 76 percent in 1988; and at Sandia, defense activities have declined from 87 percent to 78 percent since 1989. Despite these changes, the labs' combined operating budgets remained constant (in real dollars) during this period,[3]

NIST

Originally founded in 1901 as the National Bureau of Standards, NIST is the national custodian of the fundamental units of measurement. Measurements developed at NIST rest on the most secure metrological foundation possible in the United States and, in many cases, anywhere in the world. NIST is legally designated to function as the lead national laboratory for providing the measurements, calibration, and quality assurance

[3] Ibid, p. 83.

Figure 2-l—Professional Staff of DOE Weapons Labs and NIST by Degree



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p. 27.

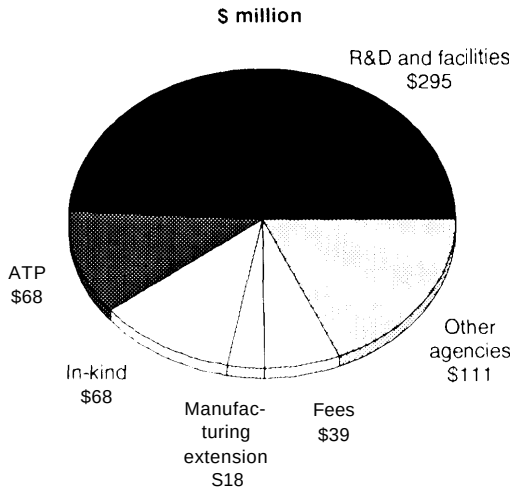
techniques that underpin U.S. commerce. Among other activities, NIST represents the United States in international affairs having to do with weights and measures, provides technical advice and consultation to other parts of the government, and cooperates with the private sector in the development of voluntary standards. NIST has developed or improved a large fraction of the measurement methods used daily by the semiconductor industV .

NIST's mission was expanded in the Omnibus Trade and Competitiveness Act of 1988 to give it a greater role in stimulating U.S. industrial competitiveness. NIST now operates a growing number of manufacturing extension centers (nine as of 1993) that bring best-practice manufacturing methods to small and medium-sized business. MST also manages the Advanced Technology Program, which provides cost-shared R&D grants to companies and other institutions developing critical commercial technologies. These extramural programs have grown from $6 million in 1988 to $86 million in 1993.

NIST is smaller than the DOE weapons labs, with a total staff of about 3,200, approximately 1,600 of whom are on the technical staff and 800 of whom hold Ph.D. degrees. NIST had a total budget of $599 million in 1993 (figure 2-2). Congress appropriated two-thirds of this total: $295 million to support MST's intramural research program and construction of new facilities, and $86 million to support ATP and the manufacturing extension centers. The remainder of NIST's budget came from outside sources: other federal agencies that support research at MST; in-kind contributions of staff and equipment from companies conducting joint research with NIST; and fees from companies using agency facilities or purchasing standard reference materials.

NIST's operating budget is likely to grow significantly in the next four years. The Clinton administration plans to shift federal R&D priori-

Figure 2-2—NIST Funding By Source, 1993



SOURCE: National Institute of Standards and Technology, "General Information About NIST," briefing to OTA, March 15, 1993.

ties away from defense and toward commercial problems. NIST has been targeted as a key player in a larger civilian effort; its budget may grow by a factor of four, to $1.7 billion, by 1997, ATP would receive the largest proportional increase, growing from $68 million in 1993 to $730 million by 1997.

Unlike the DOE weapons labs, which have only recently been chartered to collaborate with and support commercial industry, NIST has long had an industrial mission. In its work with the semiconductor industry, NIST not only supports performance specifications and operation of advanced manufacturing tools, but also provides the standards and metrology required to assure the purity and composition of materials used in manufacturing.

NIST's intramural research occupies a unique niche in the nation's infrastructure. Most companies do only enough measurement work to solve specific problems. Academic attention to measurement problems is limited. Many measurement problems cannot be broken down into small enough pieces for a student to solve in the course of a graduate program. Furthermore, in the United States, there is little perceived professional glamour in most metrological issues, so professors usually pursue other topics.

NIST has earned a worldwide reputation for impartiality and technical excellence. Its competencies in metrology span a number of disciplines (table 2-l). The efficiency of solving a measurement problem once at NIST and then disseminating the results throughout the whole industry, rather than each company performing the job independently for itself, provides outstanding leverage for NIST's metrological development. Examples studied in the semiconductor field have been estimated to have benefit-to-cost ratios ranging from 5:1 to over 100: 1.[4]

NIST produces measurement systems and prototype instruments as a byproduct of its work and initiates few projects to develop measurement hardware. Metrological programs are not like system development projects in which the end products are often the only useful results. Most NIST projects are conducted in cooperation with outside companies or laboratories, and the continuing interaction between the staffs of NIST and its collaborators transfers useful technology steadily as the work progresses. Information--not hardware-is the usual product. Project objective, organization, and size, staff operating techniques, and the types of deliverables are qualitatively different from those at DOE labs.

SEMICONDUCTOR PROGRAMS AT THE FOUR LABS

The DOE weapons labs and NIST currently support several programs that address the needs

[4]U.S. Department of Commerce, National Bureau of Standards, National Engineering Laboratory, ' 'Benefits and Costs of Improved Measurements: The Case of Integrated-Circuit Photomask Linewidths, " NBSIR 82-2458, March 1982; U.S. Department of Commerce, National Bureau of Standards, Planning Office, "Productivity Impacts of NBS R&D: A Case Study of the NBS Semiconductor Technology Program, " June 1981; Judson C. French, National Bureau of Standards, Electron Devices Section, ''Improvement in the Precision of Measurement of Electrical Resistivity of Single Crystal Silicon: A Benefit-Cost Analysis, " report no. 807, Sept. 20, 1967,

Table 2-1—NISTsS Core Competencies

Measurement services	**Physics**
Calibrations	Atomic and molecular physics
Reference data and materials	Chemical physics
	Molecular dynamics and theory
Electronics and electrical engineering	Photon, far UV, and electron physics
Electronic instrumentation	Radiation metrology and dosimetry
Superconducting materials	Radiometric physics
Electric power systems	Time and frequency standards
Magnetics	X-ray spectroscopy
Microwave components and systems	
Optical communication	**Computer science**
Semiconductor devices	Computer security
Semiconductor materials	Image recognition
Semiconductor packaging	Networking architecture and protocols
Semiconductor processes	Software standards and validation
Superconducting electronics	Speech recognition
Manufacturing engineering	**Computing and applied mathematics**
Factory automation	Mathematical software
Mechanical sensors	Numerical optimization
Microelectronics dimensions	Statistical engineering
Precision engineering	
Robotics	**Building and fire research**
	Building fire physics
Chemical science and technology	Building systems
Analytical methods	Earthquake engineering
Biotechnology	Fire safety engineering
Chemical kinetics and transport	Fire hazard analysis
Fluid flow	Structural evaluation
Nuclear chemistry	Thermal machinery
Process sensing	
Thermodynamics	

SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry," contractor report prepared for the Office of Technology Assessment, June 1993, p. 45.

of the U.S. semiconductor industry.[5] All three DOE labs have strengths in high-performance computing-originally developed to design and predict the effects of nuclear weapons—that can also be applied to device modeling, process chamber modeling, and factory modeling in the semiconductor industry. Lawrence Livermore's work in lasers and x-ray optics can help develop next-generation lithography equipment. Sandia, responsible for technologies such as microelectronics-driven guidance and control systems, operates a state-of-the-art research line that can produce submicron linewidths on 6-inch wafers. These labs can undertake large projects to develop semiconductor technologies and manufacturing equipment, and have expressed a desire to do so.

NIST offers strong capabilities in metrology, including measurements needed to produce more advanced semiconductors. NIST has maintained a program of work in semiconductor manufacturing since the late 1950s. The lab has several efforts underway to support the semiconductor

[5] This section of the report discusses major semiconductor programs at the labs. For a more complete discussion of lab projects applicable to semiconductor technology, see Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry," contractor report prepared for the Office of Technology Assessment, June 1993.

industry-for example, new techniques for measuring surface characteristics of silicon wafers and the thickness of thin films deposited on them, and development of standard reference materials for industry to use in calibrating its systems. While NIST has been named as the lead lab in metrology issues applicable to the Semiconductor Industry Association (SIA) technology roadmaps, it does not have—nor is it likely to be appropriated-the resources to address all requirements. NIST will therefore need to coordinate with industry and other government agencies capable of conducting complementary research, as it has recently done with Sandia.

If properly coordinated, research efforts at NIST and the DOE labs could complement both industry and university R&D efforts. In recent years, industry has displayed an increasing reluctance to invest in new enabling technologies because the R&D is too expensive, too risky, has lengthy payback periods, and requires strengths in many separate disciplines. This is the area in which the labs offer the strongest capabilities. These labs may be most effective as part of long-term, industry-led efforts that require large, multidisciplinary resources and facilities.

Sandia National Laboratories

Sandia National Laboratories operates the largest semiconductor program of the three DOE weapons labs. In 1993, Sandia's expenditures for microelectronics-related programs totaled $106 million, much of which supported collaborative work with commercial industry. Sandia's mission has required the lab to design and manufacture microelectronics and photonics components that withstand harsh operating environments, such as high temperatures and high levels of radiation, and to incorporate them into operational systems. Sandia has also conducted extensive test and evaluation exercises to qualify these components for use in nuclear weapons and to ensure their reliability in an adverse environment over the life of the systems.

As a result, Sandia has considerable experience in the fabrication of semiconductors and ICs. Sandia was one of the early leaders in CMOS (complementary metal oxide semiconductor) technology, the current standard for commercial devices, and helped develop the laminar-flow clean room, which is now used in most commercial manufacturing facilities. In the process, Sandia developed partnerships with defense semiconductor manufacturers, who often produced ICs designed by Sandia and returned them to the lab for final testing and acceptance.

Most of Sandia's work, however, has been directed toward the design and manufacture of ICs for defense purposes--ICs not commercially available. Most of Sandia's products are therefore either radiation-hardened circuits, high-temperature circuits, or custom ICs that industry could not efficiently produce in small volumes. These ICs are often about two generations behind commercial chips in critical parameters such as minimum linewidth, level of integration, and maximum operating speed; Sandia's most sophisticated ICs are typically those it takes from industry and radiation hardens. In addition, because it supplies primarily defense needs, Sandia's manufacturing processes have not been required to achieve the high levels of production routine among competitive commercial semiconductor manufacturers.

Nevertheless, Sandia is unique among the DOE weapons labs in that it supports several facilities for R&D and production of semiconductor devices. The largest of these is the Microelectronics Development Laboratory (MDL). The 74,000-square-foot lab includes 37,500 square feet of clean-room space with 12,500 square feet of state-of-the-art, Class 1 clean space in 22 separate clean rooms that can support individual projects. This design provides maximum flexibility for new processing equipment and device technologies. The capabilities of the MDL were expanded in 1993 by a major donation of equipment and technology from IBM. MDL now houses a state-of-the-art submicron silicon R&D line. MDL's complete

Box 2-B--Sandia's Facilities for Microelectronics

In performing its defense mission, Sandia has established several facilities for microelectronics R&D and production that may be of interest to commercial industry. These facilities address a broad spectrum of issues, from near-term to long-term, and provide, at a single facilit y, the capacit y to design, build, and test ICs and other components. This capability is unique within U.S. government facilities. These facilities are described briefly below.

Microelectronics Design Laboratory

To produce custom designs for its customers, Sandia has developed an integrated approach to the design of microelectronic components and systems. As part of these activities, Sandia writes custom support software, which has become the basis for multiple commercial design packages. Sandia's capabilities reside in a network of over 60 design stations and servers that can support either classified or unclassified projects. The software environment supports the complete design cycle, from photomask layout to systems simulation. Sandia's software environment combines circuit-level simulators, logic-level simulations, as well as both analog and digital system-level simulators, with complete verification from chip to multi-chip module to printed circuit board. The software package also combines layout of photomask with schematic vs. layout checking as well as design-rule checking.

Microelectronics Quality and Reliability Center

Sandia has the facilities and equipment to evaluate and verify the electrical and mechanical properties of microelectronic materials. This capability is applied at the parts level through Sandia's Microelectronics Quality and Reliability Center (MQRC). Sandia's reliability physics and engineering efforts draw upon materials science programs that develop a basic understanding of such failure mechanisms as electromigration or stress voiding, defects in insulators and metalizations, and defects in semiconductors.

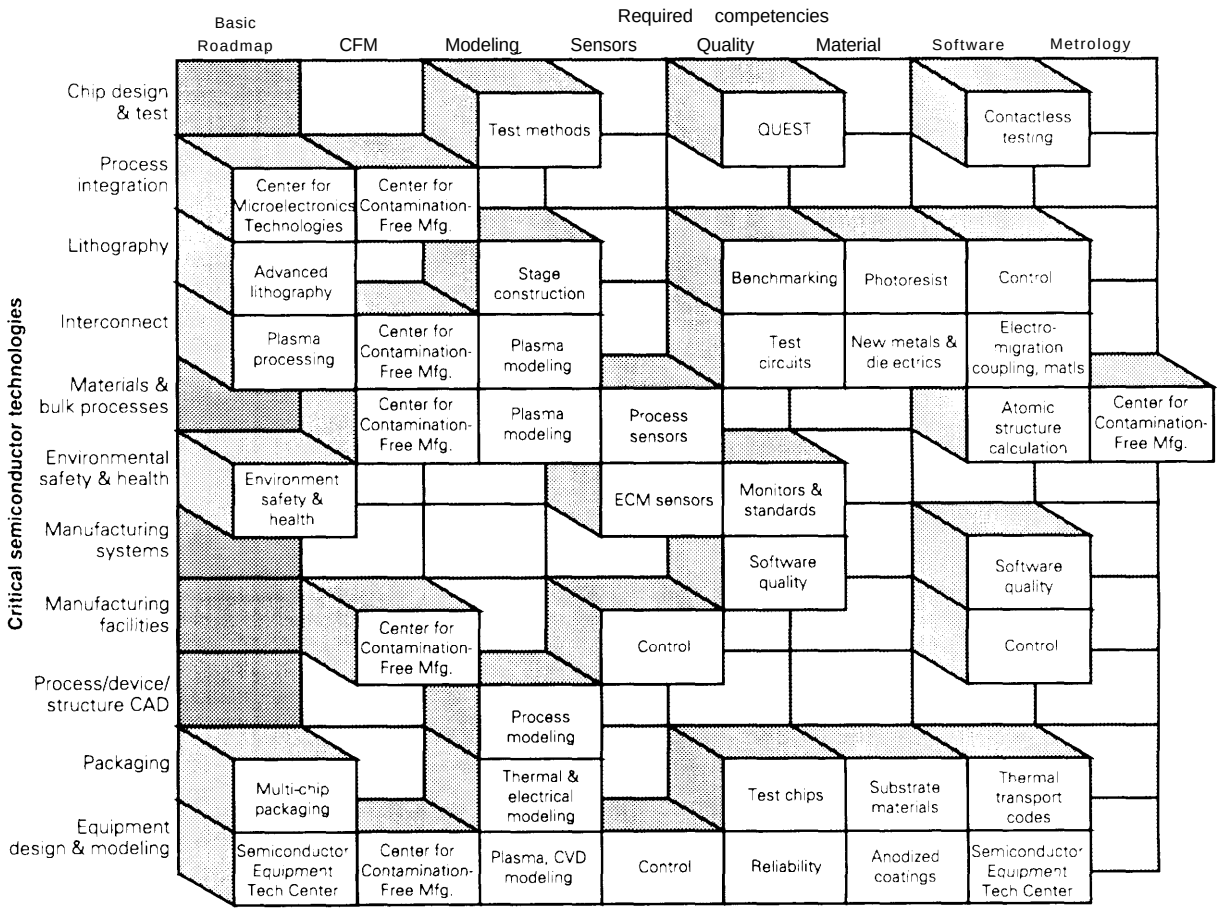
Compound Semiconductor Research Laboratory (CSRL)

The CSRL encompasses the full range of activities--theoretlcal and experimental solid-state physics, materials science, crystal growth, device and circuit design and fabrication-to develop the next generation of compound semiconductor electronic and optoelectronic devices. Facilities include MolecularBeam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) crystal growth capabilities, ion implantation, and electron-beam lithography in a 6,000-square-foot, class-100 clean room with state-of-the-art processing equipment.

Process Design Laboratory (PDL)

This facility for advanced prototype manufacturing is housed in a 100,000-sq.ft. facility and handles hybrid microcircuits, thin film, printed circuits, ceramics, plastics, and rapid prototyping facilities. The PDL coordinates its activities with an integrated manufacturing technology laboratory at Sandia's Livermore, California facility. The charter of the manufacturing center is to examine reliability and quality of manufacturing processes. Particular emphasis is given to automation and robotic hardware. This facility also acts as a proving ground and design center for custom sensors. Additional emphasis is placed on novel approaches to joining and sealing dissimilar materials that have particular relevance to advanced packaging. Collaborations with the Iaccoca Institute at Lehigh University on American competitiveness allow the PDL to support empirical investigations of manufacturing issues such as control and optimization of material flow and workspace organization.

Figure 2-3—Sandia's Ongoing Programs in Semiconductor Technology



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p. 30.

equipment set supports the total semiconductor development cycle. Other Sandia facilities support work in materials quality and reliability, compound semiconductor materials and devices, and process design (see box 2-B),

Commercial Semiconductor Programs

Many of Sandia's ongoing programs are relevant to the commercial semiconductor industry (figure 2-3). Over the past few years, Sandia has initiated a number of new programs specifically targeted at commercial manufacturing. CRADAs are an important part of this process. As of August 1993, Sandia had signed 19 CRADAs related to semiconductor manufacturing (table 2-2), a figure that represents about one-third of all CRADAs underway at Sandia. DOE's total contribution to these projects over their lifetime is estimated at $220 million; the annual contribution is approximately $63 million.

The largest of Sandia's CRADAs is a five-year agreement with SEMATECH. Sandia has been working with SEMATECH for about four years in equipment design and modeling and in technology development. Initially, Sandia's cooperation with SEMATECH operated under a work-for-others contract in which all the work was conducted by Sandia personnel at the lab and was

Table 2-2—Major Sandia CRADAs in Microelectronics

Project title	DOE funding ($K)
Soft X-ray Lithography Tools	**9,286**
Microelectronics Packaging Benchmark	**250**
Advanced Diffusion Barrier Technology	**1,950**
Reduced Lead Loss in Electronics Manufacturing	**570**
Materials Processing at High Temperature/Voltage	**2,308**
Microelectronics Quality/Reliability	**3,130**
Copper-chemical Vapor Deposition for ICs	**1,110**
Printed Wiring Board Interconnects	**5,230**
Application of IRIS to Semiconductor Plasma Processing	**420**
Synthetic Diamond for Multichip Modules	**1,250**
Fabrication of Microreactors in Silicon	**295**
Gold-sulfite Electroplating	**447**
SEMATECH Program (integrated)	**22,500**
Stable Housing **for X-ray Lithography**	**1,150**
Advanced Materials for High-performance Digital	**5,100**
Advanced Intermetal Dielectric Technology	**2,100**
Ferroelectric Read/Write Optical Disk	**1,600**
High-throughput Rotating Disk Reactors	**1,950**
Advanced Manufacturing Techniques for Monolithic Multichip Modules	**2,300**
Total	**$62,946**

SOURCE: Charles Fowler, Manager, Technology Transfer, U.S. Department of Energy, personal communication, Aug. 10, 1993.

paid for by SEMATECH. Sandia then signed a one-year CRADA with SEMATECH, which was followed in mid-1993 by the larger, multi-year CRADA. This five-year, $113-million CRADA contains some 19 individual projects. Sandia's annual contribution to the CRADA will average $22.5 million.

The bulk of Sandia's microelectronics work with industry can be divided into three primary areas: semiconductor equipment design/improvement, contamination-free manufacturing, and pilot line services, most of which are coordinated through the Center for Microelectronics Technology (CMT). Many of these programs are geared toward design and development of semiconductor manufacturing equipment, a task that is suited to the lab's technical workforce, over 60 percent of whom are engineers. Sandia has long had the responsibility for integrating new manufacturing technologies into DOE's weapons production facilities and may be able to apply such skills to commercial manufacturing processes as well.

Pilot Line Services-The focus of Sandia's industry-related work is the CMT, which DOE established to serve as a facility for industry-relevant research and development, including maturation of research concepts into manufacturable technologies. This facility is also designed to develop and test next-generation equipment and associated processes. CMT is supported by a large range of semiconductor and microelectronics capabilities and projects, and is associated with Sandia's MDL. Through CMT, university and industry researchers can gain access to the pilot line housed in MDL. This pilot line duplicates the equipment and processing capabilities found on an actual IC manufacturing line. Engineers can use the line to test and optimize new processes before launching into full-scale production on their own lines

Sandia hopes that the CMT pilot line will reduce the time and money semiconductor manufacturers must invest in R&D for new generations of process technology. These burdens have forced

even large semiconductor manufacturers to form strategic alliances with competitors in order to share R&D costs.[6] The pilot line donated by IBM includes equipment worth over $20 million and an estimated $60 million of process technology. The line offers state-of-the art processing capabilities, such as a GCA I-line stepper capable of 0.35-micron minimum feature sizes. Sandia plans to integrate its electron-beam and soft x-ray lithography modules into the line and upgrade all of the equipment to 8-inch wafers, giving them a research line capable of O. l-micron linewidths on select features. This equipment coupled with Sandia's current 6-inch wafer, 0.5-micron fabrication facility (or fab) will provide a research line service not found anywhere else within the government research community.

Equipment Design and Modeling—in August 1989 Sandia established the Semiconductor Equipment Technology Center (SETEC) to help design and improve semiconductor manufacturing equipment. SEMATECH was originally the sole sponsor of the program, providing $12 million over 30 months for ''direct support to U.S. companies engaged in the design and manufacture of IC manufacturing equipment and materials. Since 1991, SEMATECH and DOE have jointly sponsored SETEC through a CRADA, each contributing an average of $6 million per year.

SETEC projects are directed toward development of equipment models to enhance the performance of future-generation equipment, developing design-for-reliability methodologies, and equipment benchmarking. Semiconductor equipment costs are increasing at an extremely fast rate. Today's new semiconductor factory will cost over a billion dollars-three-quarters of which is due to the cost of machinery and equipment.[8] According to current projections, future factories will not yield an adequate financial return unless significant advances are made in equipment reliability and design[9].

One SETEC project, the Reliability Analysis and Modeling Program (RAMP), which is jointly conducted with seven equipment manufacturers, developed software for modeling the reliability of their equipment, including mean time before failure, life cycle cost, and reliability improvement. Such analysis allows manufacturers to redesign equipment so as to improve its performance. Since the project was completed in early 1992, over 150 copies of the RAMP software have been distributed to a wide range of equipment suppliers. Sandia trained 200 people to use the software.

In another SETEC project, Sandia is modeling plasma etch and deposition equipment[10]. Although plasma processing is the method of choice for most etching and deposition steps, the physical characteristics of plasmas are not well known, making them difficult to predict and control. Understanding the mechanism for transferring ions to the silicon wafer requires knowledge of

6 For example, in the last few years, IEM, Toshiba, and Siemens have agreed to jointly develop technologies to produce 256M DRAMs, and Intel has teamed up with Sharp to develop flash memories using 0.6- and 0.4-micron processes.

7 ''Sandia National Laboratories Complete Intitial SETEC Program/Sign New Work Agreement With SEMATECH,'' *SEMATECH Communique,* May/June 1992, p. 6

8 Semiconductor Industry Association *Annual DateBook: Global and US. Semiconductor Competitive Trends, 1978-1991 (San* Jose, CA: Semiconductor Industry Association 1992), p. 38

9 Semiconductor Industry Association, *Semiconductor Technology—Workshop Working Group Reports (San* Jose, CA: Semiconductor Industry Association, 1993), p. 14.

10 A plasma is an ionized gaseous discharge in which there is no resultant charge, the number Of Positive and negative ions being equal. Plasma processing occurs in a reactor, sometimes called a cell, where a high level of control is exerted over the gas temperature and electrical inputs. Plasmas can be used to etch, or remove material from, the patterned surface of a wafer, opening up windows that allow the electrical properties of the silicon in the patterned areas to be changed in subsequent steps. Plasmas can also be used to deposit layers of material on a wafer.

gas chemistry, cell structure and design, and the effects of temperature. Through SETEC, Sandia is attempting to use a supercomputer to develop and verify a basic model of plasma etching, after which it will modify and reduce the code to run on industry-standard mini computers. If successful, the model will reduce from years to months the time it takes equipment makers to bring new designs to market, while improving the uniformity of the etch (or deposition) and machine throughput.

A third SETEC project aims at developing a magnetically levitated stage for a wafer stepper. This technology would allow manufacturers to improve the alignment capability of their lithography equipment. To make complex ICs, patterns must be aligned to within about one-third of the minimum feature size. As linewidths narrow, overlay requirements tighten accordingly. For current ICs with 0.5-micron linewidths, patterns must be aligned to within 150 nanometers (rim); by 2001, the overlay requirement will be 50 to 70 nm.[11] Current technologies may not be able to meet such strict requirements, but proof-of-concept versions of the magnetically levitated stage have demonstrated alignment within 20 nm. Coupled with a new interferometer under development at Sandia, the stage could achieve 0.5-nm stability.

Contamination-Free Manufacturing--Sandia established a Center for Contamination-Free Manufacturing (CFM) through a CRADA with SEMATECH in 1992. The center conducts and coordinates research in cost-effective contamination-free manufacturing technologies involving feature sizes as small as 0.2 microns and removal of defects as small as 0.01 microns (the size of bacteria). The CFM uses Sandia's MDL to conduct experiments that verify advanced semiconductor manufacturing concepts and to develop equipment that reduces the levels of contamination in integrated-circuit manufacturing. Research focuses on the effects of electrostatic fields, chemical particulate, thermal radiation, and electromagnetic radiation (including light) on circuit yield and performance.

Contamination is a primary cause of reduced yields in semiconductor manufacturing. Impurities can arise out of processing chemicals, wafer handling systems, process chambers, and air in the factory. As IC feature sizes become smaller, manufacturers must try to simultaneously reduce the density of defects on a wafer and their size. In 1993, manufacturers could typically tolerate approximately 30 defects on a 6-inch wafer; by 1998, the defect density must be reduced to 20 defects per 8-inch wafer; and by 2004, it must be reduced to Just 5 defects per 16-inch wafer.[12] Whereas in the early 1990s 1-micron contaminants were of little concern, current manufacturing practices cannot tolerate defects larger than 0.1 micron, and defects down to 0.01 micron are quickly becoming a problem. Particles of this size cannot be seen optically and are otherwise difficult to locate on a wafer. New techniques must be invented to detect them.

CMT currently consists of seven projects, which fall into four categories and are included in a 1993 CRADA between Sandia and SEMATECH. In one project, Sandia is developing sensors for detecting contaminants generated during wafer processing. These sensors will enable manufacturers to detect contaminants in real time, allowing for immediate corrective action before fabrication is complete. The sensors will have to be rugged enough to operate in harsh processing environments and be able to monitor gas and chemical purity for unwanted moisture and other particulate at the few parts-per-billion level.

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11 This is roughly the diameter of 150 to 200 atoms. Semiconductor Industry Association, *Semiconductor Technology-Workshop Working Group Reports* (San Jose, CA: Semiconductor Industry Association 1993), p. 37.

12 Semiconductor Industry Association, Semiconductor *Technology—Workshop Working Group Reports*, op. cit., p. 3.

Table 2-3—Los Alamos CRADAs in Microelectronics

Project title	DOE funding ($K)
Supercritical $C0_2$ Cleaning of Particulate	$1,766
Electromagnetic Simulation: High-frequency Computer Circuit Calculations	454
Conductive Oxide Electrodes for Ferroelectric Memory Development	559
Modeling and Simulation of Electronic Devices	2,770
High-temperature Superconductor Devices	3,875
Diamond Technology for Particle and X-ray Detectors	520
Total	$9,944

SOURCE: Charles Fowler, Manager, Technology Transfer, U.S. Department of Energy, personal communication, Aug. 10, 1993.

Another type of sensor is being developed for microenvironments. Microenvironment are small plastic containers used to protect and transport wafers between processing steps. Usually the same container is used to transport the same set of 25 wafers from the time they are shipped to the factory until wafer processing is completed. Microenvironment can be a major source of contamination, especially if a film is introduced into the container or if the plastic walls of the container begin to out-gas. The film and/or gas has the potential of ruining all 25 wafers. For wafers containing 100 microprocessors valued at $300 each, the loss of just one container costs $750,000.

Sandia engineers are investigating two ways of monitoring the microenvironment. The first uses the wafers themselves as sensors. Silicon wafers demonstrate a property called total internal reflection. Light directed into a clean crystal will reflect off the inside walls without any loss of intensity. Thus, the microenvironment can be tested by shining light through a window in the wall. The other method of testing the environment uses an electrical vibrating crystal to generate a surface wave across the wafer. Contaminants will retard the wave progress along the wafer.

Other CFM projects include an evaluation of a high-frequency ultrasonic (or megasonic) cleaning mechanism for wafers and several modeling projects that attempt to predict the generation of contaminants during wafer processing and find ways to remove those particles before they reach the wafer.

Los Alamos National Laboratory

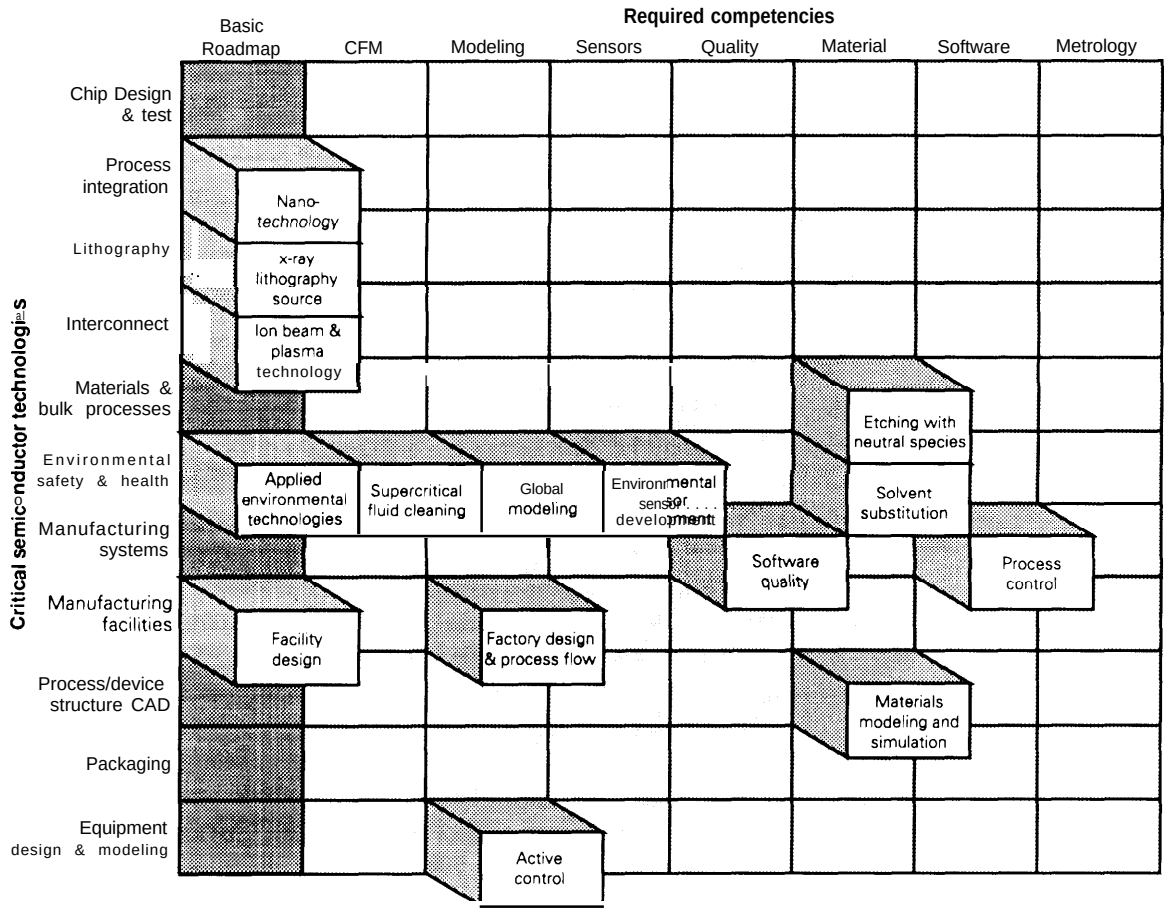
Los Alamos does not have a history of IC fabrication, and its R&D programs in semiconductor technologies are more limited than Sandia's. As a result, Los Alamos has had less interaction with industry in developing semiconductor technologies. In August 1993, Los Alamos had six active CRADAs related to microelectronics, totaling almost $10 million of in-kind laboratory contribution (table 2-3). The number of ongoing programs at Los Alamos that are relevant to the SIA roadmaps is small compared with Sandia (figure 2-4).

Nevertheless, the lab's people and facilities constitute several strong core competencies important to semiconductor manufacturing. Those in which Los Alamos could play a lead role include computer-aided design (CAD) for semiconductor devices and circuits, the materials from which they are made, and the processes used to manufacture them; modeling of semiconductor fabrication facilities; and environmental safety and health (ES&H). Los Alamos' experience with beam technologies could also give it a supporting role in lithography and materials processing.

Modeling and Simulation

Modeling and simulation based on high performance computing is a particular strength of Los Alamos, The lab may be able to play a lead

Figure 2-4-Los Alamos' Ongoing Programs in Semiconductor Technology



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p.37.

role in the development of tools for modeling IC wafer fabrication processes, an area called Technology CAD, or TCAD. Los Alamos is already working with the Semiconductor Research Corporation (SRC) **to** define its role in the development of TCAD technologies.

Los Alamos performs extensive modeling of materials to atomic detail. This work can contribute to both the device and process modeling needs of the semiconductor industry. The lab is developing detailed three-dimensional simulations for devices and circuits to account for the interaction of materials, geometry, and packaging. These computer codes are designed to predict the performance of advanced devices for which conventional simulations are inadequate. The goal of this work is to provide validated design tools for future generations of devices and circuits.

Los Alamos has specialized modeling and simulation capabilities that, when used in conjunction with the capabilities of the other laboratories, can address the needs for process modeling and can contribute to the design of improved process chambers. For example, chemical vapor deposition (CVD) technology is used widely **to** deposit materials such **as** oxides and nitrides of silicon on wafers in the production of ICs. The

design of CVD chambers can be improved substantially by modeling and simulation, thereby improving chip yield and cost.

Los Alamos's modeling capabilities can also be applied to the analysis of complete factories. Such models would allow a full semiconductor manufacturing process to be simulated, including product flows, waste generation, and cost. Such codes may be important in analyzing the cost of future semiconductor fabrication facilities. The cost of building and equipping a new integrated circuit factory today is projected to be over a billion dollars. Even after production starts, it usually takes six months before yields are high enough to make a profit. In order to gain and maintain leadership in semiconductor sales, the industry is striving to offset these costs by improving productivity, increasing quality, and reducing cycle times[13].

Factory modeling has only recently been applied to semiconductor facilities [14]. One reason for this delay is the sheer complexity of the manufacturing process. Random yields, diverse equipment characteristics, unpredictable equipment downtime, material flows, and the problems inherent in using a single facility for both production and research have made modeling difficult. Moreover, most of the more than 300 steps required to produce a single IC require high levels of precision and process control. Between 80 and 100 different machines may be used on a typical production line. Collecting process data at each of these stations requires large computing resources: approximately 240,000 transactions occur each day in a wafer fab.

In support of DOE's efforts to consolidate weapons production facilities, Los Alamos created custom simulations for each DOE manufacturing plant. In addition to performance parameters such as throughput and cycle time, the simulation tracked all material flows, waste streams, and worker exposures. Though not yet tested in the semiconductor industry, these capabilities could help semiconductor manufacturers better plan their production facilities (box 2-C).

Los Alamos' modeling capabilities are made possible by extensive computing facilities. In December 1991, DOE named Los Alamos one of two national High-Performance Computing Research Centers (HPCRC). The HPCRC will attempt to promote technology transfer in advanced computing to industry, academia, and other laboratories through the operation of a computational laboratory, the Advanced Computing Laboratory (ACL). These facilities can make important contributions to the semiconductor industry in TCAD.

Environmental Safety & Health

Los Alamos currently plays a lead role in DOE's program of environmental remediation. In 1993, the lab budgeted almost $200 million for environmental cleanup. While much of this program is tailored to clean-up of nuclear wastes, a number of projects address issues of interest to the semiconductor industry. For example, Los Alamos is working with the Joint Association for the Advancement of Supercritical Fluids to find alternatives to solvents used for precision cleaning in the electronics industry. Through the DOE Industrial Waste Reduction program, Los Alamos is researching ways to recycle metals from waste streams. Los Alamos' Life Cycle Activities project supports work with the Microelectronics and Computer Technology Corporation (MCC) on recyclable workstations and with Motorola on materials return and reuse. The lab is also working with the EPA, the American Electronics Association, and other DOE labs to develop an information retrieval system to access environmental information of relevance to industry. Finally, the lab is working with the American Electronics

13 R. Uzsoy, C. Lee, L. Martin-Vega, "A Review of Production Planning and Scheduling Models in the Semiconductor Industry, Part I: System Characteristics, Performance Evaluation and Production Planning," *IIE Transactions*, vol. 24, no. 4, Sept. 1992, p. 47.

14 Ibid.

Box 2-C-Commercial Application of Los Alamos' Process Modeling Capabilities

Though Los Alamos has not yet applied its factory modeling capabilities to a semiconductor plant, its experience in other portions of the electronics industry demonstrates the efficacy with which codes developed for defense applications can be used to solve commercial problems. One example is Los Alamos's work with Quatro, a small New Mexico business that manufactures printed wiring boards. In the United States alone, the market for printed wiring boards was estimated at $5.5 billion in 1993. Sales by U.S. companies were estimated at $2 billion.

Quatro wanted to build a printed wiring plant that was economically competitive internationality and environmentally benign. The company approached both Sandia and Los Alamos in early 1992 to request help finding a commercially available software package for the factory design. Upon further investigation it was found that any commercially available package would require an extensive effort to modify to include environmental considerations and worker exposure. Thus the company turned to Los Alamos for the simulation.

Applying previously developed code, two engineers--one from Los Alamos and one from Quatro--worked only eight hours to develop a baseline system that accurately portrayed Quatro's existing production facility. With the baseline completed, the engineers used the simulation to optim ize the factory's 120 machine processes. Because of federal and state environmental regulations, pollution prevention was a primary concern. Employing the tool, the engineers were able to completely eliminate many hazardous materials from Quatro's waste stream, including 1,560 pounds of chelated copper, 312 pounds of formaldehyde, and 1,200 pounds of tin and lead per year. Through recycling, the new factory will save on the transportation costs of 63,600 gallons per year of spent etchant, and water use will be reduced to one-third its original level.

The project was completed only 18 months after Quatro decided to undertake the plant study. Without Los Alamos' assistance and code, the baseline system itself could have taken a full man-year of effort to design. As it is, the plant simulation, plant design, detailed costing, and blueprints are finished. The company is currently seeking a combination of private and public funding (about $5 million) to build and initiate operations. Quatro estimates its plant modernization program will substantially increase the number of jobs in the company.

Association to develop alternative manufacturing technologies for manufacturing printed wiring boards.

Applications of Beam Technologies

Another area in which Los Alamos can make a special contribution is in the application of beam technologies (laser beams, electron beams, and ion beams) to semiconductor manufacturing. For example, Los Alamos is developing intense soft x-ray sources based on linear accelerators. These sources can generate light with a wavelength of 13 nm for use in projection lithography systems capable of drawing O. l-micron linewidths. Los Alamos is also working on large-scale ion-beam etching systems that may be of value in the low-cost manufacture of high-density microelectronics packaging (such as multichip modules). These systems potentially offer high levels of throughput at low cost.

Other applications of ion beam technology could allow thin films to be deposited onto silicon or gallium arsenide wafers with greater efficiency than is possible using commercial laser technology. Still other work is pursuing an ion implantation technique based on plasma immersion processes that allows shallow doping of large areas of silicon. Such processes may become important in the development of multiple-layer ICs. Though still in the laboratory stage, Los Alamos hopes to

form an industry partnership to build a prototype system.

Los Alamos has been working with energetic beams of neutral (uncharged) particles for etching and thermal processing. Neutral beams are superior to ion beams for etching feature sizes less than 0.5 micron because they cause less structural damage to the substrate material.[15] Neutral beams can also grow insulating layers while avoiding many of the problems associated with thermal etching processes.[16] Los Alamos would like to team with an industrial partner active in chip processing to create prototype production equipment using hot neutral sources.

Lawrence Livermore National Laboratory (LLNL)

Like Los Alamos, Lawrence Livermore has not manufactured ICs as part of its mission. The lab does, however, run several R&D programs in semiconductor technology that contribute to portions of the SIA roadmap (figure 2-5), Of LLNL's $1 billion operating budget in 1993, approximately $80 million supported R&D in areas related to semiconductor technology. In addition, LLNL, like the other DOE laboratories, has expanded the scope of its cooperative R&D with industry, By the end of 1992, LLNL was contributing $72 million to 84 cooperative agreements with industry; over $30 million was for CRADAs in microelectronics (table 2-4)

The areas in which LLNL is most capable of contributing to the SIA roadmaps are in x-ray lithography, IC packaging, and other applications of laser technology. Lawrence Livermore has developed world-class scientific and technical expertise in high-power lasers and electro-optics. The lab has extensive experience in the technology of laser-generated soft x-rays, soft x-ray optics and diagnostics, and precision metrology. LLNL has also worked on applications of laser technology to doping semiconductors. Most of this work is conducted at the Center for Applications of Laser and Electro-Optic Technologies (CALEOT), which maintains 20,000 square feet of laboratory space for R&D on advanced lithography and on laser material processing

Soft X-ray Projection Lithography

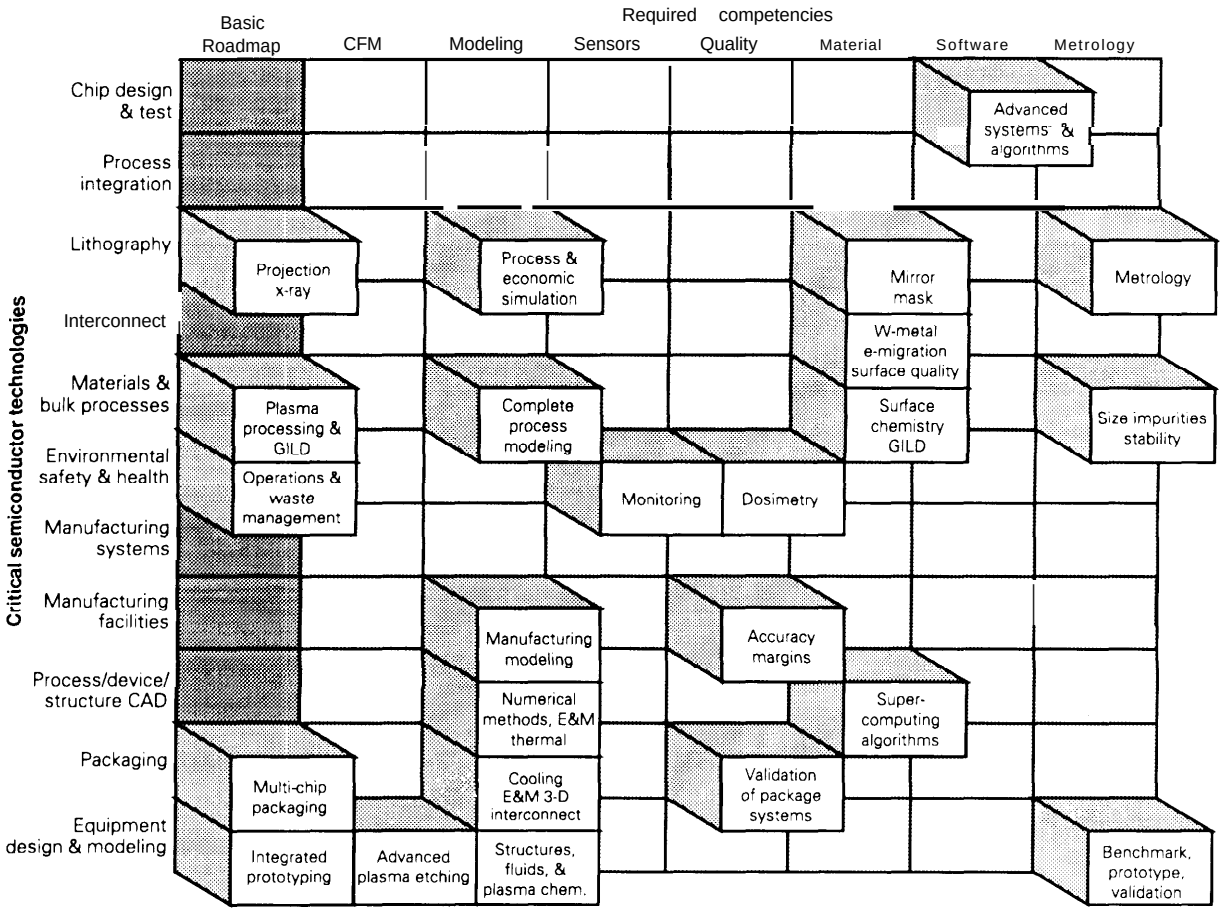
LLNL has a number of programs in soft x-ray projection lithography that could enable it to take a lead role in a larger, national x-ray lithography program, The appeal of soft x-ray projection lithography as a lithographic strategy for U.S. industry derives largely from its potential to project features of 0.1 micron or smaller. This reduction in size could provide a 25-fold improvement in integrated circuit density by the end of this decade.

LLNL, Sandia, Lawrence-Berkeley Lab (LBL, another of DOEs multi-program labs), and industrial organizations are building the prototype systems. AT&T and LLNL devoted about $8 million between 1989 and 1992 to develop and characterize high-performance coatings for the multilayer mirrors that direct the x-rays from their source to the mask. LBL and LLNL have spent $4 million on x-ray interferometry systems to measure the characteristics of x-ray optics. GCA-Tropel has submitted a CRADA proposal to the labs to further pursue this work. LLNL and Micrion Inc. have devoted about $2 million to mask patterning, damage, and repair studies. AMD, DuPont, KLA, and Micrion have submitted a CRADA proposal to LLNL to develop defect-free coating technology and inspection and repair capabilities. Ultratech Stepper and Jamar also have CRADAs with LLNL in soft x-ray projection lithography.

15 Ion beams can break down thin insulating layers of material and build up charge in localized areas, causing deformation of the side walls etched into the substrate,

16 In gallium arsenide devices, for example, thermal processes used to grow a layer of oxide can result in the formation of metallic arsenic and can induce disorder in the lattice structure of the substrate.

Figure 2-5—Lawrence Livermore's Ongoing Programs in Semiconductor Technology



SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p. 44.

Additional lithography research is being conducted by LLNL's Center for Applications of Laser and Electro-Optic Technologies (CALEOT). Lasers developed by the lab were to be used by Hampshire Instruments to support work in proximity x-ray lithography and could supplant excimer lasers used for UV lithography systems. The company folded before the project could be completed. The solid state glass laser developed by CALEOT is being inserted into a state-of-the-art commercial lithography system.

Laser Applications: Gas Immersion Laser Doping (GILD)

Lawrence Livermore National Laboratory and Stanford University are working together on an innovative doping process which significantly reduces the number of steps required to make integrated circuits. The process, called Gas Immersion Laser Doping (GILD), replaces currently ion implantation processes and, in practice, can reduce lithographic processing steps (among the most expensive in a fabrication facility) by 46

Table 2-4—Lawrence Livermore CRADAs in Microelectronics

Project title	DOE funding ($K)
Cost-Effective Machining of Ceramics	1,646
Interconnects for Multichip Modules	2,817
Computer-Aided Design of Plasma Etch Reactors	4,800
Compact Soft X-ray Exposure System	10,458
Fabrication of Non-Planar Devices	1,065
Soft X-ray Projection Lithography	9,800
Total	$30,586

SOURCE: Charles Fowler, Manager, Technology Transfer, U.S. Department of Energy, personal communication, Aug. 10, 1993.

percent--cutting costs while improving yield and device performance.

GILD uses a relatively simple process to diffuse dopant atoms into a silicon wafer. A silicon wafer is immersed in an atmosphere of dopant gas. An excimer laser beam is then directed through a patterned mask, melting the wafer surface at specific locations and causing the dopant molecules to diffuse into the silicon. The ion implant (conventional) technique directs a high-energy stream of dopant ions into the silicon wafer. But before the ion implantation can be done, the wafer surface must be prepared by applying a special coating, called a resist, to areas that must be shielded from the ion stream. The resist preparation includes a lithographic exposure, etching, and a cleaning operation. After the ion implantation, the resist must be stripped off, requiring plasma processing and several cleaning operations. All told, ion implantation takes 13 steps compared with GILD's one (figure 2-6).

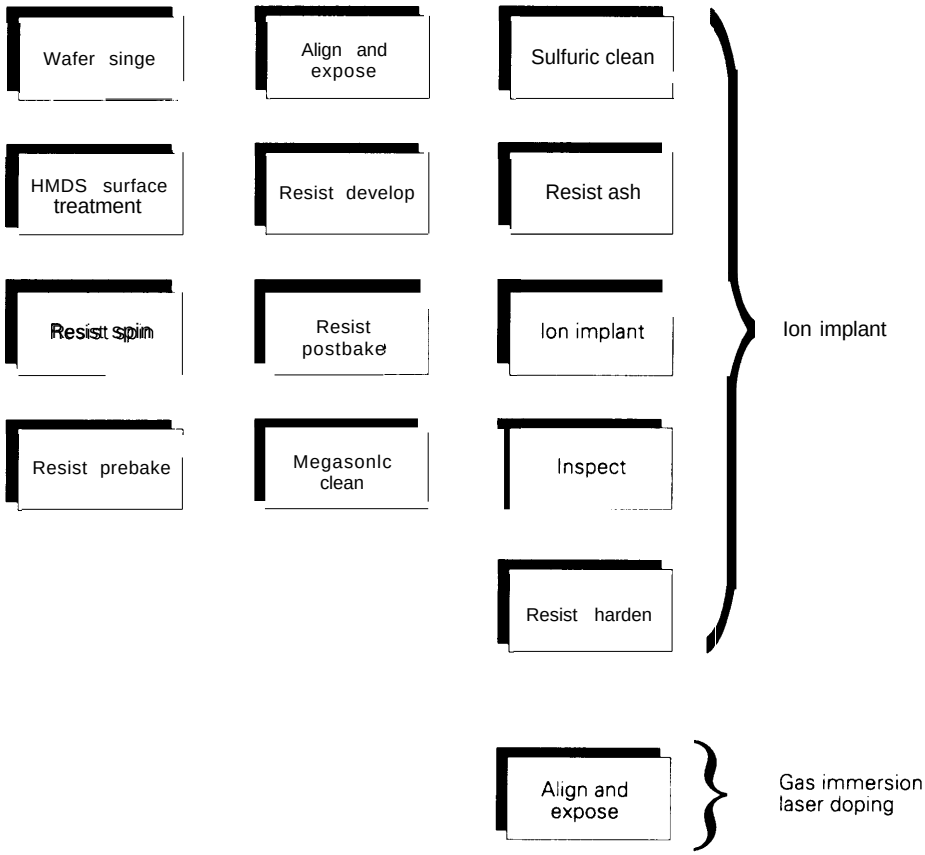
GILD not only reduces the number of steps for doping, it also provides better control over the process. Two critical processing factors for any doping technique are the dopant density at the junction and the junction depth. GILD controls the amount of dopant absorbed by the number of laser pulses at the junction while the junction depth is controlled by adjusting the laser intensity. At this time GILD is the only demonstrated technology that can produce junction depths shallow enough to meet the SIA roadmap junction depth requirements for the year 2001 and beyond. SIA specifies a maximum junction depth of 25 nm for the year 2001. GILD currently produces junction depths as shallow as 10 nm whereas ion implantation is at 40 nm. Other benefits over conventional processing include more uniform dopant distribution, the ability to fabricate narrower base regions, and the elimination of high-temperature anneals (which complicate multilayer processing by allowing dopants to migrate into adjacent layers), and compatibility with 0.2 micron and smaller feature sizes,

LLNL is already one year into a three-year project that is focused on process development and advanced equipment design to demonstrate suitability for manufacturing applications. The projection version of the GILD tool is compatible with the flexible fab or cluster tool concept being pursued by DoD's Advanced Research Projects Agency (ARPA) to help reduce the economies of scale inherent in semiconductor manufacturing. ARPA had provided some early funding to GILD to supplement laboratory funding, but future support is uncertain.

National Institute of Standards and Technology (NIST)

NIST supports semiconductor research through both its intramural and extramural programs. Intramural programs make use of NIST's own staff and facilities and are oriented almost exclusively toward metrology. Extramural programs are conducted by industry partners and can therefore explore technical problems outside

Figure 2-6--Processing Steps Required for GILD Versus Traditional Ion Implantation Techniques



SOURCE: Kurt Weiner, Lawrence Livermore National Laboratory, personal communication, Aug. 27, 1993.

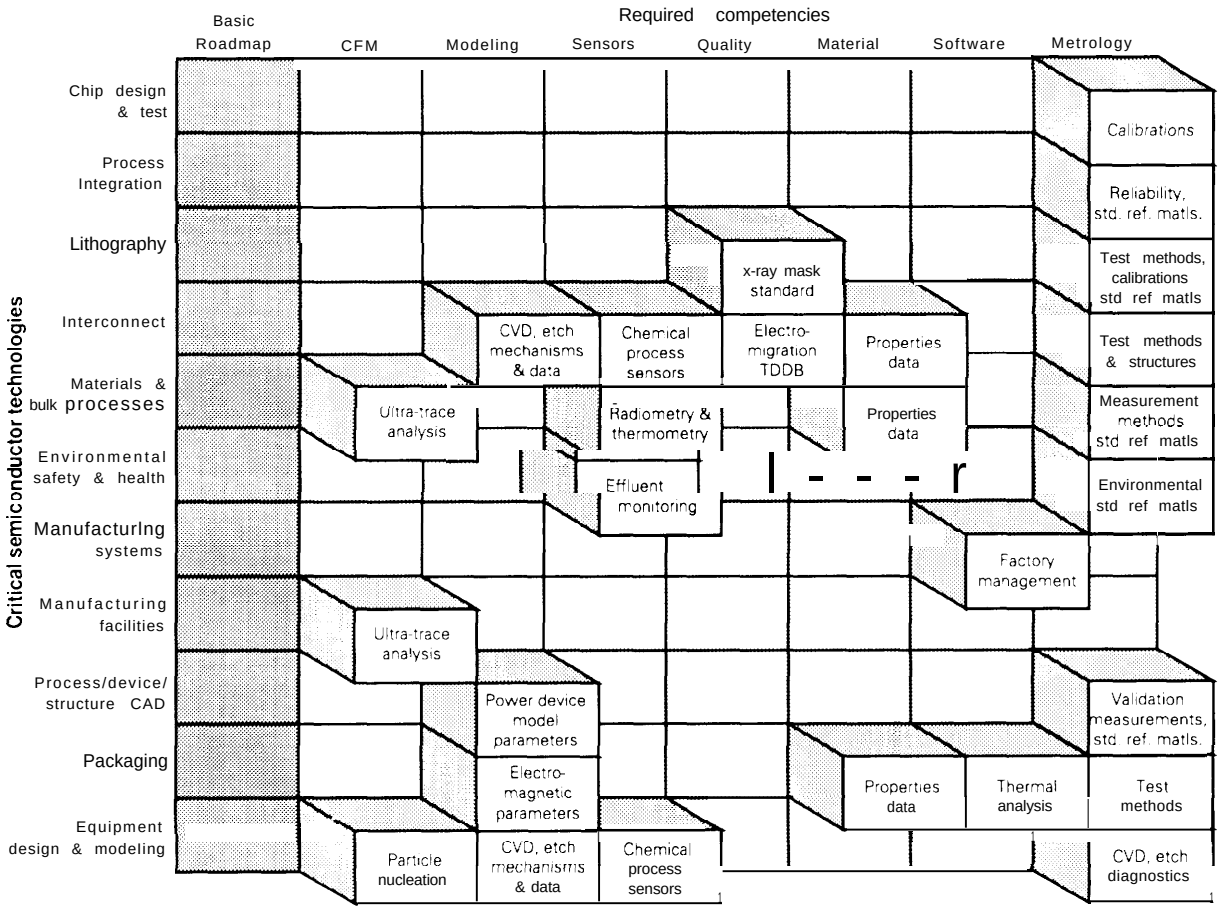
NIST's specific areas of expertise. Together, these programs give NIST the capability to contribute to many areas of semiconductor technology.

Intramural Programs

NIST's intramural programs in semiconductor technology are conducted largely by its Semiconductor Electronics Division, which has an operating budget of about $7 million and a staff of 43, about 35 of whom are full-time researchers. An additional $2.5 million of work is performed by other NIST divisions responsible for chemistry, physics, computer science, and materials science. The programs conducted by these divisions match many of the requirements of the SIA roadmap (figure 2-7). Primary thrusts of the current research program are on semiconductor materials measurements; selected device properties, theory, and models; process control measurements based on test structures and supported by machine learning analytical techniques; and optical and non-optical critical dimension metrology (see box 2-D).

One example of NIST's work is the ellipsometer developed by the Materials Technology group. This device uses polarized light reflected obliquely off a silicon wafer to measure the thickness of deposited films. NIST used this ellipsometer to develop standard reference materials, available in

Figure 2-7—NIST's Ongoing Programs in Semiconductor Technology



SOURCE: Avtar S. Oberai, 'The OTA Report on Federal Labs and the Semiconductor Industry: Partners in Technology," contractor report prepared for OTA, June 1993, p.46.

50-, 100-, and 200-nm thicknesses and certified to an accuracy of half a nanometer, so that industry can verify its own measurement systems. NIST's initial offering of sets of the standard reference materials sold out quickly at $1,300 apiece, and the sets are still in demand.

NIST's semiconductor technology program is being expanded by the Office of Microelectronics Programs as new funding can be obtained to draw on the many other technical resources present at NIST. New work has begun on plasma etching processes to develop the data necessary for the creation of physically based process models. Additional research is underway to measure the properties of materials used in semiconductor device packaging, and on extensions to the existing work described above. Both the structure of existing work and plans for new work are being adjusted to address the measurement needs of the national semiconductor roadmap, which specifically identifies NIST roles in the area of metrology and reference data.

NIST has also participated in projects sponsored by SEMATECH. NIST found and corrected a number of sources of errors in the light-intensity measurements in a developmental lithography system. It had appeared that the lithography system was not meeting its light output specifica-

Box 2-D—NISI% Role in Resistivity Measurement

NIST has a long history of helping semiconductor manufacturers and their suppliers measure the resistivity[1] of silicon wafers used to manufacture ICs. Before NIST initiated its program in resistivity measurement in the early 1970s, difficulties in correlating measurements of resistivity between silicon suppliers and IC manufacturers resulted in some 7 percent[2] of all silicon shipments being rejected by manufacturers. Comparable losses in terms of today's silicon market would cost the U.S. semiconductor industry well over $1803 million a year.

Suppliers custom-make silicon to the buyer's specifications, the most important of which is the acceptable resistivity range. Resistivity indicates the silicon's purity, uniformity, and suitability for device purposes. Often, inaccurate measurements either caused buyers to accept orders that were out-of-specification, resulting in low production yields, or caused them to reject orders that could have been acceptable. The lack of measurement agreement was so commonplace that silicon vendors began to keep a log of adjustment factors that helped to compensate for the difference between their measurements and the measurements of their customers.

in 1960, the American Society for Testing and Materials (ASTM) asked NIST (then the National Bureau of Standards) to take the lead in improving measurement techniques of the resistivity of silicon. Most companies, at the time, used the four-probe method for measuring resistivity. The process used one pair of probes to send a known amount of current through the wafer; another pair of probes measured the voltage drop across a section of the wafer. Resistivity was calculated using a simple formula relating the current, the voltage, and the spacing of the probes. The process gained much popularity because it was non-destructive and efficient. NISTspent several years studying the problem with the help of over 22 companies. The effort resulted in the development of correction factors and a standardized procedure for making the measurement. The overall accuracy was improved by an order of magnitude.

The most obvious savings realized from the improvement was a reduction in material rejection or waste caused by a lack of measurement agreement between the buyer and the seller. In addition, buyers were able to reduce the previous levels of testing necessary to achieve measurement agreement with the seller. The most significant benefit, but hardest to quantify, is the gain in manufacturing yields resulting from improved production control.

Upon release in 1967, the NIST correction factors and measurement procedure became a world standard. Shortly thereafter, NIST began selling a silicon wafer standard reference material (SRM) so that suppliers and buyers can check and calibrate their measurement instruments. The SRM, too, has become a de facto standard, used throughout the world.

Today NIST is working on improving the resistivity measurement required to take the industry to 0.2-micron linewidths. Two atomistic methods are being developed. One essentially sandblasts a hole into the material using argon ions,The ratio of silicon atoms to dopant atoms coming out of the hole is subsequently measured, Resistivity is based on the ratio. The other method measures resistivity by mapping atoms on an atomic scale. The goal is to reduce t he measurement uncertain y from the current 1.6 percent to 0.8 percent.[4] The procedures for the new method will be released by 1995.

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1 Resistivity is the resistance that a centimeter cube of a material Offers to the passage of electricity.

2 improvement *in the Precision of Measurement of Electrical Resistivity of Single Crystal Silicon: A Benefit-Cost Analysis,* J. French, National Bureau of Standards, Report Number S07, Sept. 1967.

3 Seven percent of the $s.4 billion market for semiconductor grade silicon in 1993.

4 Personal communication, R. Scace, NIST, April 1993.

tions, but the problem was entirely a matter of measurement error. In another project, NIST is conducting a round-robin calibration experiment on mass flow controllers, used universally for controlling gas flows in semiconductor manufacturing equipment, but often found to be inaccurate. Errors in these controllers arise from calibration uncertainties, incorrect installation practices, and variations in the composition of gas mixtures. The experiment is aimed at the frost of these effects; subsequent work will address the other issues. These projects have resulted in the establishment of new calibration services at NIST for ultraviolet light meters and for mass flow controllers.

NIST supports a wide range of working relationships, from a single phone call or visit to extended residence of industrial, academic, and government researchers at NIST under several forms of agreements that include CRADAs. As of spring 1993, the Semiconductor Electronics Division had signed about 10 CRADAs with industry, each averaging $200,000 of NIST contribution. These figures correlate to one CRADA active or pending for every four full-time technical employees. In addition, the Semiconductor Electronics Division had many guest researchers working in its facilities.

NIST's CRADAs tend to be smaller than those of the DOE labs, reflecting the smaller scale of many metrology projects and the agencys smaller budget. The DOE labs' larger budgets enable them to mobilize many researchers to attack large problems requiring extensive facilities; a typical NIST project may involve only two to three full-time research personnel.

Extramural Programs

In addition to its intramural research program, NIST also manages extramural semiconductor research conducted under the Advanced Technology Program. Through ATP, NIST provides funding to individual companies and consortia to develop precompetitive, generic technologies. ATP is a cost-shared program in which industry typically provides more than half the total project funding and sets research goals and objectives. All projects must pass a technical evaluation and a business plan evaluation to help ensure that the programs are technically feasible and that the participating companies have a viable plan for commercializing the resulting technology. The goal of the program is to help companies apply research results to the rapid commercialization of new scientific discoveries and to the refinement of manufacturing technologies. The program can assist joint R&D ventures with technical advice or it can provide start-up funding or a minority share of the cost, or lend equipment, facilities, and people to the venture.

ATP has supported a number of semiconductor projects. Out of the 60 grants awarded during ATP's first three competitions, 18 are related to semiconductor technology. Participating companies plan to contribute $45 million to these 18 projects and requested just under $50 million in funding from ATP, to be spread out over periods of one to five years. In 1993, ATP provided $7.8 million in matching funds for microelectronics technology projects. These projects span a broad spectrum from manufacturing equipment to semiconductor devices to systems. Under one program, Spire Corp. will develop advanced sensors for a metal-organic chemical vapor deposition chamber used to produce diode (semiconductor) lasers. In another program, Nonvolatile Electronics, Inc. will develop anew type of random access memory (RAM) device that will not lose data when turned off.

COORDINATION OF LAB ACTIVITIES

Together, the semiconductor programs run by the DOE and NIST labs address many of the issues associated with the SIA roadmap, OTA's industry panel, after reviewing the labs' capabilities, identified several areas in which these labs could work effectively (table 2-5). However, each individual cell on the SIA roadmap will require many complementary projects to address near-,

Table 2-5—Possible Semiconductor Focus Areas for Federal Labs

- **Perfect process chambers**
  - Modeling/verification
  - Science knowledge base
  - Environmental safety and health (sensors)
  - Environmentally conscious manufacturing
- **Metrology**
  - Calibration services
  - Standards/reference materials
  - Reference data
  - Measurement methods
  - Diagnostic techniques
- **Wafer handling**
  - Contamination
  - Mechanism design for high reliability
  - Algorithms
  - Software assurance
- **Material systems**
  - Chemistries
  - Contamination-free manufacturing
  - Point-of-use generation/disposal
- **Lithography**
  - invention/commercialization gap
  - Soft x-ray
  - Sources/stages/alignment
  - Electron beam/ion beam technology and prototypes
  - Metrology for mask and water analysis
- **Technology computer aided design (TCAD)**
  - Algorithms for design simulation
  - Algorithms for process synthesis
  - New computing tools
  - TCAD framework
- **Manufacturing systems**
  - Factory design and modeling
  - Flexible scalable factories
  - Sensors
  - Large wafer equipment design/technology
- **Packaging**
  - Cooling
  - Thermal analysis budgets
  - Energy efficiency
  - Array bonding
  - Stress/thermal/electro-magnetic modeling
  - Low stress, encapsulants
  - Multichip packaging technology
- **New materials**
  - Advanced metallization (i.e., copper) dielectric/package materials
  - Thin dielectrics
  - Characterization of materials
- **Device physics**
  - Use of advanced computing techniques from process and device to system analysis and synthesis
  - Nanotechnology
- **Contamlnatlon-free manufacturlng research**
  - Defect and contamination modeling
  - Detection, measurement, and analysis
  - Wafer cleaning and transport
  - Clean gases, liquids, equipment, and processes
- **New chemistries**
  - Neutron beam for low-damage, high-throughput etching and deposition
  - Environmentally sensitive materials
  - Chemical recycling/re-use

SOURCE: Avtar S. Oberai, "The OTA Report on Federal Labs and the Semiconductor Industry," contractor report prepared for the Office of Technology Assessment, June 1993, pp. 51-52.

mid-, and long-term issues. Industry, universities, and the labs will each have roles in any program to address these needs. Proper coordination of these organizations will be required to ensure effective use of the labs' capabilities.

Coordination with industry will be required to make sure that laboratory programs meet commercial requirements. To date, the DOE weapons labs have concentrated their technology development programs on issues of importance to the defense community; these labs have only limited experience working on commercial technologies or in a commercial environment in which cost is a primary concern and product generations change rapidly. Making the transition will require time and considerable industry guidance. The SIA roadmaps represent a first step in this direction, in that they express, in a form that is easy to communicate, industry's consensus on its technology needs for the next fifteen years. Continued industry participation will be needed, however, to ensure that laboratory programs to meet these needs are properly implemented and

properly coordinated with industry and university R&D efforts.

Additional coordination will be needed to eliminate or prevent unnecessary redundancy between laboratory programs. At this point, however, the potential for such overlap appears limited. One reason is that the capabilities of the DOE weapons labs and NIST are, in many ways, complementary. DOE labs have the skill set, expertise, and funding to work on large-scale R&D programs, especially those that require multi-disciplinary teams and large, expensive facilities. The DOE labs are set up to work on the higher-risk, longer-duration projects and to deliver operating prototypes, as well as an underlying precommercial knowledge base. NIST is best suited to solving measurement problems and delivering results in a form suitable for use by the industry. Measurement may be a demanding problem requiring significant fundamental research prior to developing a technique suited for practical use, or it may require off-the-shelf NIST technology.

Furthermore, while several labs may claim a competency in a particular technology area, these areas are so broad that planned programs are unlikely to overlap. For example, all three DOE laboratories are strong in numeric simulation and modeling; however, they use this competency to accomplish separate mission responsibilities. Sandia's modeling capabilities are targeted toward plasma modeling and chemical vapor deposition chambers; Los Alamos uses its modeling capabilities to simulate factories and develop active control systems for use with real-time sensors; Lawrence Livermore's modeling capabilities support work in areas such as packaging, structures, and lithography. In addition, both LLNL and NIST have ongoing programs in metrology to support x-ray lithography, but LLNL's capabilities in forming aspheric mirrors are complemented and supported by NIST's capabilities in measuring the precise curvature of the mirror's surface. Similarly, all three DOE laboratories have established major efforts in environmental safety and health for weapons work that may be relevant to semiconductor processing and environmentally conscious manufacturing. Sandia has capabilities in sensors and monitoring for quality; Los Alamos supports work in solvent substitution and clean manufacturing technologies; Lawrence Livermore has research programs in dosimetry and waste management.

In addition, the labs have expressed a commitment to achieve the required coordination and have made several attempts to coordinate their research efforts. Sandia recently signed a Memorandum of Agreement (MOA) with NIST on their activities in metrology. The first industry to be addressed under the Sandia/NIST MOA is the U.S. semiconductor industry. The intent of this program is to maximize cooperation and minimize duplication so that the resources of the two institutions are used most effectively. In addition, the new National Center for Advanced Information Component Manufacturing (NCAICM) established by Congress at Sandia will coordinate research by the three DOE weapons labs and ARPA in the areas of flat panel displays and microelectronics, Projects under this program will be funded through ARPA and performed jointly by industry and the DOE labs. NIST and Sandia have also coordinated their efforts in x-ray lithography through lab visits and transfers of personnel. Such efforts may prove highly effective in enhancing the ability of the laboratories to contribute to commercial semiconductor technology.

The Semiconductor Industry

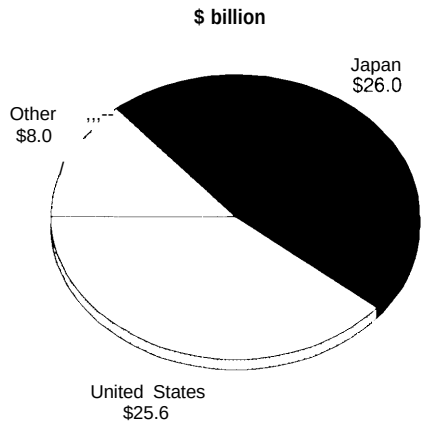
3

Over the past three decades, semiconductor manufacturing has become increasingly vital to the U.S. economy. Not only does the U.S. semiconductor industry generate over $25 billion in annual sales and employ over 200,000 workers, but, as an enabling technology for most electronic products, it is essential to the generation of millions of high-wage, high-skill jobs and sales of over $300 billion in such industries as computers, telecommunications, and industrial equipment. Products based on semiconductor technology contribute in turn to productivity gains in many sectors of the U.S. economy.

Nevertheless, the U.S. semiconductor industry faces several challenges that threaten its future competitiveness. International competition has eaten away at U.S. market share, in both the world and domestic markets. Many competitors receive direct support from national governments that have targeted semiconductor technology as a central part of their industrial development plans and have initiated programs to boost the commercialization of semiconductor technology. In addition, the costs of research and development (R&D) and new production facilities are growing exponentially, while sources of patient capital are rapidly eroding. With short product cycles, semiconductor firms are having difficulty supporting the rapid pace of investment and are looking for new sources of financing, often through joint ventures with foreign competitors. Materials and equipment suppliers are also facing financial difficulties.

To date, most U.S. policy in support of semiconductor technology has been limited to ensuring fair trade and protecting

Figure 3-1—Share of World Semiconductor Production by Nation, 1992



SOURCE: Office of Technology Assessment, 1993; based on data from Semiconductor Industry Association, ***Annual Databook: Global and U.S. semiconductor Competitive Trends-1978-1991*** **(San Jose,** CA: Semiconductor Industry Association, 1992), p. 12.

national security.[1] Through the Semiconductor Trade Agreement (STA), the U.S. government attempted to open the Japanese market to U.S. producers. Federal funding has concentrated on R&D, the bulk of which has been funded by the U.S. Department of Defense (DoD). Recently, DoD has supported the Semiconductor Manufacturing Technology consortium, SEMATECH. Concern over flagging competitiveness of semiconductor manufacturers in a time of declining defense budgets has, however, induced considerable discussion of means for ensuring the continued success of the U.S. semiconductor industry. It has become increasingly evident that government policy can enhance many areas of technological competitiveness in the industry, and may be necessary in order to preserve its strength. Federal laboratories may have a role to play in working with industry to develop next-generation semiconductor technologies.

A STRATEGIC INDUSTRY

The semiconductor industry holds a strategic position within the U.S. and global economies. In 1992, sales of semiconductor devices topped $60 billion worldwide; U.S. shipments totaled $26 billion (figure 3-1).[2] These figures include sales of all electronic components based on semiconductor technology:[3] integrated circuits (ICs) such as microprocessors and memories; discrete components such as transistors and diodes; and other semiconducting devices such as solar cells and photo diodes. Within the U.S. economy, the most significant of these categories is ICs, which comprised 73 percent of total U.S. semiconductor shipments in 1991, a fraction that has remained fairly constant over the past decade (figure 3-2).[4] Beyond their purely financial effects, integrated circuits, which pack thousands of interconnected circuits onto a single chip, also allow the creation of innovative new electronic products unimaginable with individual, discrete devices. ICs also necessitate the development of sophisticated production machinery and processes, and have large effects on other parts of the U.S. economy.

Contributions to the U.S. Economy

The semiconductor industry contributes disproportionately to job and revenue growth throughout the U.S. economy. Semiconductor manufacturers employed 220,000 workers in the United

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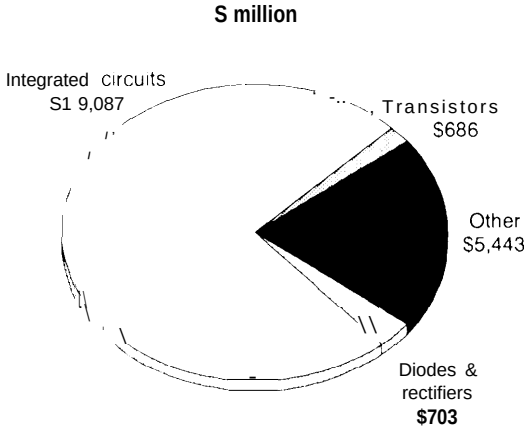
[1] Through NIST, the government has supported the basic metrology that industry needs to manufacture competitive products, but this support has not been as large or as extensive as that for national security.

[2] SEMATECH, 1993 *Annual Report,* p. 6; and Electronic Industries Association 1993 *Edition Electronic Market Data Book* (Washington, DC: Electronic Industries Association% 1993), p. 98.

[3] Semiconductor technology refers to an entire class of materials-and the devices made from them-that have conductivity in between that of an insulator and a true conductor such as metal. Semiconductors derive their conducting characteristics from carefully controlled amounts of impurities (or "dopants"), such as phosphorus, boron, or aluminum, which are inserted into crystals of an otherwise nonconducting material such as silicon or gallium arsenide.

[4] Electronic Industries Association op. cit., footnote 1, p. 98.

Figure 3-2—U.S. Semiconductor Sales by Device Type, 1992 (Estimated)



SOURCE: Office of Technology Assessment, 1993; based on data from Electronic Industries Association, ***1993 Edition Electronic Market Data*** Book(Washington, DC: Electronic Industries Association, 1993), p. 98.

States at the beginning of 1993.[5] Many of these jobs are highly knowledge-intensive, reflecting the large amounts of R&D required to stay competitive in the industry.[6] Only 42 percent of all semiconductor workers were production workers at the beginnin g of 1993, a figure considerably lower than the 68 percent average for all U.S. manufacturing industries. Moreover, many of the production jobs in semiconductors require high levels of skill, involving the operation and maintenance of highly sophisticated production equipment; simple assembly jobs have been either automated or moved off-shore. As a result, hourly wages for production workers in the semiconductor industry averaged $14.23, considerably higher than manufacturing in general and most other electronics sectors (table 3-l).

Table 3-l-Comparison of Employment and Earnings in Semiconductors With Other Manufacturing Industries, January 1993

Industry	Employees (thousands) Total	Production	Hourly wages
Semiconductors	**220**	**93 (42%)**	**$14.23**
All manufacturing	**17,939**	**12,185 (68%)**	**$11.61**
Autos	**827**	**635 (78%)**	**15.52**
Aircraft	**581**	**273 (470A)**	**17.03**
Chemicals	**1,063**	**557** (52%)	**14.69**
Industrial equipment	**1,934**	**1,167 (60°/0)**	**12.61**
Electronic and electrical equipment	**1,538**	**979 (64%)**	**11.14**

SOURCE: U.S. Department of Labor, Bureau of Labor Statistics, ***Employment and Earnings,*** April 1993.

The semiconductor industry supports a wide-ranging base of suppliers who provide semiconductor manufacturing equipment (SME), control software, gases, chemicals, and silicon substrates. The world market for equipment and materials totaled about $20 million in 1992, with the U.S. market comprising about half of that.[7] On the equipment side, U.S. SME vendors earned $5.5 billion in sales in 1992, 58 percent of which was from U.S. semiconductor manufacturers. SME manufacturers employed over 28,000 workers in 1991.8 U.S.-based materials suppliers earned over $1 billion in revenues in 1992, mostly from sales to U.S. companies.

Even larger effects occur in downstream markets. Semiconductor technology is the key to most modern electronic products: computers, consumer electronics, communications equipment, and industrial equipment. Manufacturers are incorporating semiconductors into products such as automobiles and aircraft as well[9], but

5 U.S. Department of Labor, Bureau of Labor Statistics, "Employment and Earnings, " April 1993, p. 83.

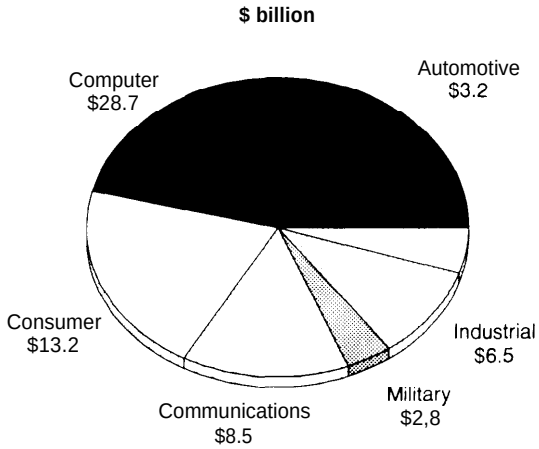
6 Despite the globalization of the industry and the fact that some 50 percent of U.S. semiconductor chips are shipped overseas, American corporations perform about three-quarters of their high value-added wafer fabrication in the United States.

7 National Advisory Committee on Semiconductors, *Attaining Preeminence in Semiconductors* (Washington, DC: National Advisory Committee on Semiconductors, February 1992), p. 9.

8 Personal communication from Peggy Haggerty, Vice President, SEMI/SEMATECH; data from VLSI Research.

9 Approximately 3 to 5 percent of the value of new automobiles is electronics; for commercial and military aircraft, 15 to 30 Percent "the value may be electronics.

Figure 3-3-Worldwide Sales of Semiconductor Devices by Customer, 1992



SOURCE: Dataquest, Inc.

Table 3-2—U.S. Factory Sales and Employment in Electronics by Industry Group, 1992

Sector	Sales (millions)	Employees (thousands)
Communications equipment	$68,097	477
Computers and peripherals	56,360	395
Consumer electronics	9,183	61
Industrial and medical electronics[a]	33,969	279
Semiconductors	27,388	221
Other related products/services[b]	55,875	NA
Electronic components	36,756	374
Total	$287,628	1,807

a Includes control and processing equipment, test and measurement equipment, nuclear electronic equipment, medical electronic equipment, robots, accessories and components, and other electronic systems and equipment.
b Includes estimates of electronic content of the annual sales of industries, such as autos and aircraft, considered partially electronic, as well as computer and software services (but not prepackaged software).
NA = Not applicable.

SOURCE: Electronic Industries Association, 1993 *Edition Electronic Market Data* Book (Washington, DC: Electronic Industries Association, 1993).

approximately 45 percent of the worldwide semiconductor sales in 1992 went for use in computers (figure 3-3). Consumer electronics and communications together purchased another 35 percent of output, while automotive and industrial applications totaled 15 percent of the market. U.S. industries that depend upon semiconductor technology together produced almost $300 billion in manufactured goods and employed over 1.8 million workers in 1992 (table 3-2), making electronics the second largest basic industry in the United States (behind chemicals) and the largest industrial employer.[10]

By 1995, electronics-related industries are expected to comprise 25 percent of all manufacturing.11 U.S. employment in semiconductors and the electronics industry overall is likely to decline marginally through 2005, as is employment in manufacturing generally,[12] due to rising worker productivity, slowing rate of growth of the labor supply as the population ages, and a decline in defense spending. Nevertheless, increases in productive output should continue, especially in the areas of computers and semiconductors, which are projected to grow fastest of all manufacturing areas. Estimates of growth are for 7.6 percent annually in computers and for 5.6 percent annually in semiconductors, both well above the 2.3 percent growth anticipated for all manufacturing industries. [13]

Contributions to National Security

Semiconductor technology is vitally important to national security. Throughout the Cold War, U.S. defense policy was based on the availability of superior technology to overcome the numerical superiority of Warsaw Pact forces. Integrated circuits became integral components of nuclear missiles, precision-guided munitions, early warn-

lo SEMATECH, 1992 *Annual Report,* p. 7.

[11] Ibid., p. 7.

[12] Max L. Carey and James C. Franklin, "Industry Output and Job Growth Continues Slow Into Next Century," *Monthly* Labor *Review, November* 1991, pp. 45-94.

[13] Ibid., pp. 58-59.

ing and surveillance systems, aircraft, and communications systems. Concern over the continued development of advanced microelectronics technologies and over foreign dependence on such technologies [14] led the military to invest heavily in semiconductor R&D and to develop procurement regulations governing U.S. content.

While procurement budgets may fall in concert with the declining defense budget, military support of semiconductor R&D is likely to continue at steady or increasing levels. The Advanced Research Projects Agency's (ARPA) funding for electronics manufacturing technology jumped from $98 million in 1991 to over $330 million in 1993. With declining personnel rosters and fewer new starts for major weapons programs, the military will probably rely more on improved semiconductor technology to maintain national security and upgrade existing weapons platforms.

The commercial semiconductor industry is the probable source of many of these components. Commercial semiconductors are in many ways technically superior to their defense counterparts and, due to their larger scales of production, are considerably lower in price.

COMPETITIVE HISTORY OF THE U.S. SEMICONDUCTOR INDUSTRY

Because semiconductor manufacturing has such a strong influence on national economies, many countries--including European nations and Japan—have launched vigorous campaigns to develop indigenous semiconductor industries and gain global market share.[15] Government polices at home and abroad have altered the competitive dynamics of the industry. Though dominating early markets, U.S. semiconductor manufacturers are now increasingly challenged by international competitors.

From the mid-1950s through the early 1980s, the United States was the undisputed leader in virtually all segments of the semiconductor industry. U.S. manufacturers dominated world markets for ICs, manufacturing equipment, and supplies. They invested more than all other nations in new plant and equipment as well as R&D and pioneered new technologies. Throughout the 1980s, however, foreign rivals increasingly challenged U.S. semiconductor manufacturers and, by 1987, had secured approximately 63 percent of the global market for semiconductors. Japanese manufacturers are the primary competitors; at their zenith in 1988, they controlled some 52 percent of the market. Since 1989, U.S. manufacturers have staged a modest resurgence, regaining market share from the Japanese and re-establishing market leadership in 1992 with an estimated 43.8 percent share of the world market (versus 43.1 percent for Japan).[16] These changes reflect a combination of industry initiative and government policy.

Early U.S. Dominance

Early American dominance in semiconductors stemmed from the nation's lead in entering the field. Both the transistor and the IC were invented in the United States. Work on solid-state amplifiers began during the 1930s at Bell Laboratories after researchers realized that future switching would need to occur through electronic means, and that future markets would be large enough to justify investment in new technology. These

[14] See Institute for Defense Analyses, *Dependence of U.S. Defense Systems on Foreign Technologies* (Washington, DC: Defense Technical Information Service, December 1990).

[15] Japan has launched a series of initiatives coordinated by the Ministry of International Trade and Industry (MITI) to stimulate development of semiconductor technology and electronic products. In the 1980s, the European Community initiated the JESSI program to develop semiconductors and the ESPRIT program to promote information technology generally. See Thomas R. Howell, et al., *The Microelectronics Race: The Impact of Government Policy on International Competition* (Boulder, CO: Westview Press, 1988), chapters 3 and 4.

[16] Statistics from VLSI Research, Inc., as cited in T. R. Reid, "U.S. Again Leads in Computer Chips," *Washington Post*, Nov. 20, 1992, p. Al.

efforts resulted in the discovery of the transistor by William Shockley, John Bardeen, and Walter H. Brattain in 1947. Jack Kilby at Texas Instruments, Inc. patented the first integrated circuit in 1959 at about the same time that Robert Noyce at Fairchild Camera developed planar processing techniques, upon which current manufacturing is based.

Though commercial interests stimulated work in semiconductor technology, government interest was largely responsible for large-scale production of ICs that led to early domination of the industry by U.S. firms. U.S. industry initially expressed skepticism about ICs. IBM, then the largest single private-sector customer for semiconductor devices, used discrete transistors rather than ICs in its 360-series computer. In 1962, NASA announced plans to use ICs in the Apollo program's guidance computer, and soon thereafter the Air Force stated its intent to use them in the Minuteman II guidance system. These programs allowed U.S. manufacturers to get the economies of scale required to make semiconductors affordable for commercial use and to demonstrate and improve their reliability .17

The Japanese Challenge

Japanese companies did not begin producing semiconductors until the 1960s. For many years their products suffered from low yields and high prices. By the mid-1960s, Japanese manufacturers were achieving yields of just 10 percent, compared with 25 percent for their U.S. competitors. Prices were often three times those in the United States. In 1971 Japanese manufacturers sold at more than 20 percent below cost in order to compete with U.S. manufacturers, and as late as 1972, the semiconductor divisions of the major Japanese producers had failed to turn a profit.[18]

In the late 1970s, however, several Japanese companies rose to worldwide prominence in semiconductor manufacturing, due in part to assistance from the Ministry of International Trade and Industry (MITT). Through MITI, the Japanese government provided financial assistance, low-interest loans, accelerated depreciation schedules, and other measures that lowered capital costs and enabled semiconductor manufacturers to continue investing in plant and equipment despite large losses. In addition, MITI organized and helped fund several industry-wide R&D programs, including the successful VLSI Project (1976 to 1979) that targeted dynamic random access memory (DRAM) chips. Over the next several years, Japanese companies achieved higher yields and productivity and lower costs than American firms, particularly in memories, driving many U.S. manufacturers out of the market by the mid-1980s. The U.S. share of the world market for all ICs declined from about 57 percent in 1982 to 39 percent in 1991, reaching its low point of about 37 percent in 1988. Japanese market share rose from 33 percent to 47 percent during the same time (figure 3-4).[19]

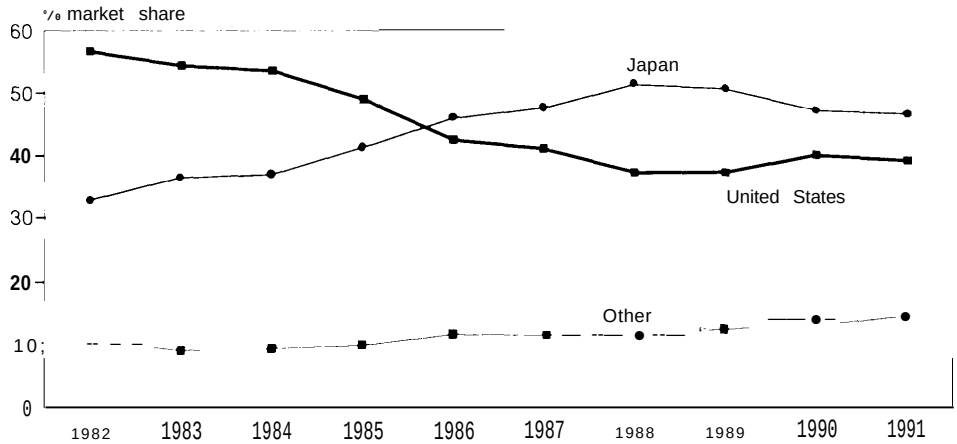
Japanese competition has been most noticeable in markets for commodity chips, such as DRAMs, that are the least dependent on design capabilities and the most dependent on manufacturing capabilities and quality. Between 1978 and 1992, the U.S. share of the global DRAM market declined from about 75 percent to less than 20 percent; Japanese market share grew from 25 percent to 54 percent during the same period (figure 3-5). In more design-intensive, higher value-added market segments, U.S. companies maintained a

17 Arthur J. Alexander, The *Problem of Declining Defense R&D Expenditures*, JEI-14A (Washington, DC: Japan Economic Institute, April 16, 1993), p. 11.

18 U.S. Congress, Office of Technology Assessment, *Competing Economies: America, Europe, and the Pacific Rim*, OTA-ITE-498 (Washington, DC: U.S. Government Printing Office, October 1991), p. 249,

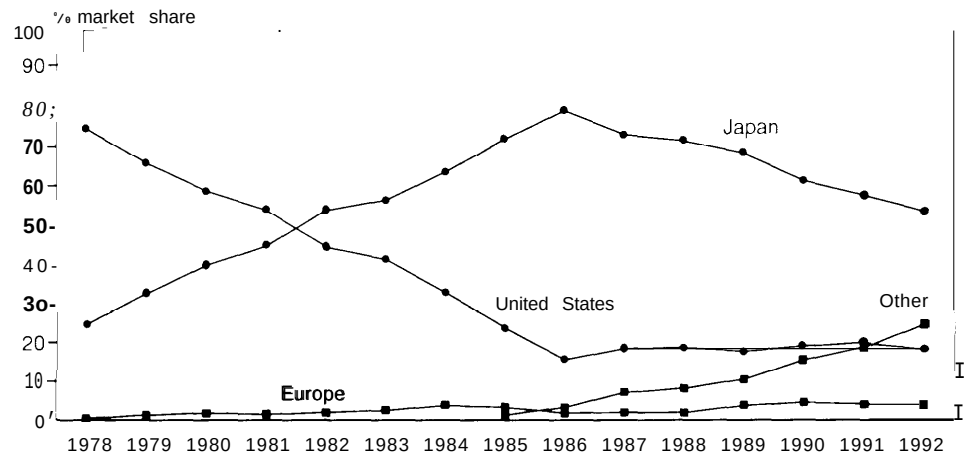
19 Semiconductor Industry Association and Dewey Ballantine, *Creating Advantage: Semiconductors and Government Industrial Policy in the 1990s* (San Jose, CA: Semiconductor Industry Association 1992), p. 9.

Figure 3-4-Semiconductor World Market Shares, 1982-1991



SOURCE: Semiconductor Industry Association, ***Creating Advantage: Semiconductors and Government Industrial Policy in the*** 7990s (San Jose, CA: Semiconductor Industry Association, 1992), p. 9.

Figure 3-5—Worldwide DRAM Market Share, 1978-1992



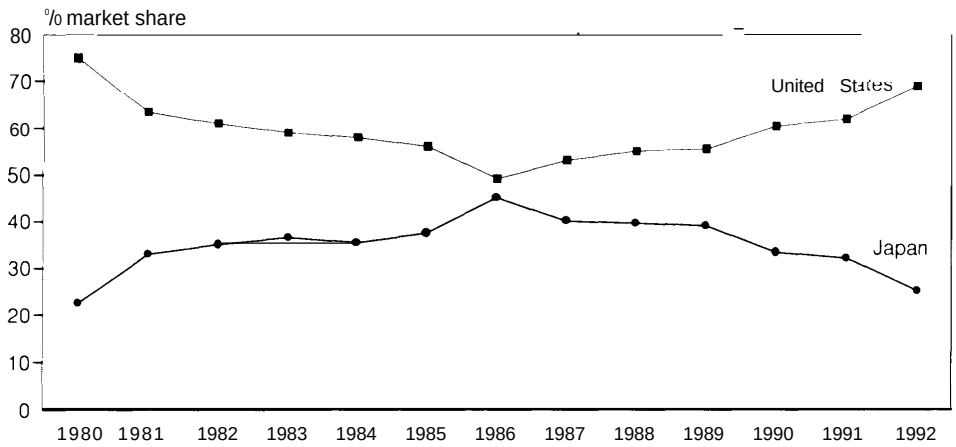
SOURCE: Dataquest, Inc.

dominant position, but the lead was trimmed significantly. U.S. share of the market for microcomponents and other types of microcontrollers declined from 75 percent in 1980 to just under 69 percent in 1992 (figure 3-6), while Japanese market share rose from 21 percent to 25 percent. In the market for application-specific integrated circuits (ASICs), which include custom and semi-custom chips, U.S. market share also declined, from 60 percent in 1984 to about 53 percent in 1992, but the United States remained the market leader (figure 3-7).

Reasons for Japanese Success

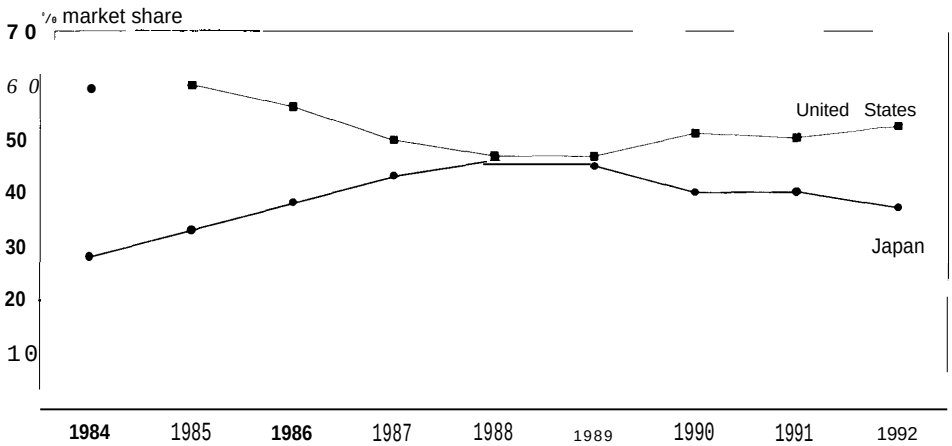
Japan's success in semiconductors resulted not just from increased funding of R&D. Japan also used a successful mix of financial, technological, and industrial resources to ensure that programs

Figure 3-6-Share of World Market for Microcomponents, 1980-1992



SOURCE: Dataquest, Inc.

Figure 3-7-Share of World Market for ASICs, 1984-1992



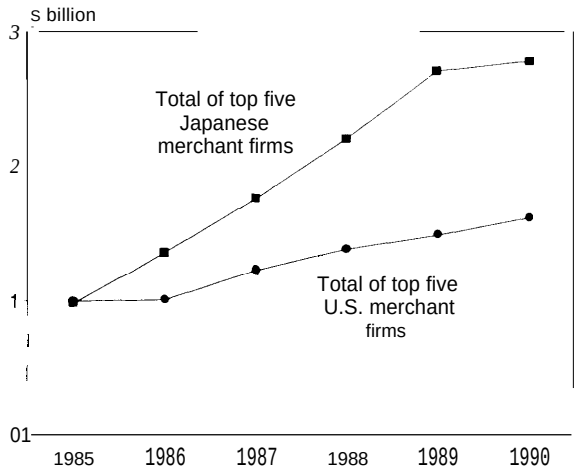
SOURCE: Dataquest, Inc.

were developed rapidly and efficiently, and were pursued over the long term. At the same time, Japanese firms pursued a strategy of expanding market share rather than increasing profitability, often accepting substantial short-term losses in order to establish their market presence and achieve long-term growth. Other differences between Japanese and U.S. trade practices and industry structure (outlined below) also contributed to the Japanese success.

Availability y of Capital

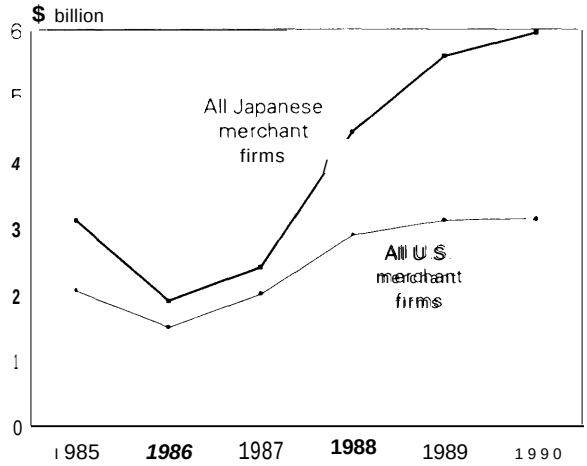
Since 1982, Japanese semiconductor manufacturers outspent their U.S. competitors on R&D and capital goods. In 1988, Japanese capital spending was nearly $2 billion higher than that of the United States; by 1990, Japanese semiconductor manufacturers were spending $6 billion on capital goods versus $3 billion in the United States. R&D spending by the top five Japanese producers also rose from near parity with the United States in 1985 to nearly $1 billion more by

Figure 3-8-Semiconductor R&D Spending



SOURCE: Dataquest, Inc.

Figure 3-9-Semiconductor Capital Spending



SOURCE: Dataquest, Inc.

1990. These differences in expenditures occurred despite the fact that U.S. producers had higher sales that the Japanese until 1986 (figures 3-8 and 3-9).[20]

These spending differences reflect significant differences in government policy and industrial structure in the two nations. By designating microelectronics as a priority industry, the Japanese government increased its attractiveness to prospective lenders and investors; further, the lending policies of the Japan Development Bank, which makes loans to designated priority sectors at MITI's recommendation, have signaled to commercial banks that the government favors microelectronics companies and has thereby mobilized capital for the semiconductor industry .21

Japanese companies also benefited from a lower cost of capital during the 1980s. Although capital costs in Japan have approached those in the United States in recent years, and direct comparisons are difficult to make, Japanese costs appear to have been much lower.[22] Keiretsu banks are a primary source of capital for their affiliated semiconductor producers. During the 1970s, the Japanese semiconductor producers' relationships with the keiretsu banks enabled them to finance aggressive capital expansion through heavy borrowing. While in the 1980s the leading Japanese producers reduced their reliance on debt as a source of capital, their special relationship with the banks remained a critically important asset.[23] Combined with lower interest rates, these relationships helped mitigate the risk associated with large financial outlays.

The structure of the Japanese semiconductor industry also supports greater capital expenditures. Most semiconductor manufacturers in Japan are part of large, vertically and horizontally integrated conglomerates with large assets. Giants like Nippon Electric Corp. (NEC), Hitachi,

20 National Advisory Committee on Semiconductors, *Attaining Preeminence in Semiconductors* (Washington, DC: National Advisory Committee on Semiconductors, February 1992), p. 23.

21 Thomas R. Howell, op. cit., footnote 15, p. 65.

22 National Advisory Committee on Semiconductors, *A Strategic Industry at Risk* (Washington, DC: National Advisory Committee on Semiconductors, November 1989), p. 17. See also Richard P. Matteone, "A Capital Cost Disadvantage for Japan?' Morgan Guarantee Trust, Tokyo, April 1992.

23 Thomas R, Howell, op. cit., footnote 15, p. 65.

and Toshiba are fully integrated; they put their chips into their own products. Integration allows closer cooperation between IC suppliers and systems integrators. More importantly, integration (vertical or horizontal) can make capital available from internal funds outside the IC division, provided other divisions are earning healthy profits. Deep pockets are a particular advantage during market slowdowns, when prices decline. They allow companies to fund long-term R&D and forego immediate returns for long-term growth in market share. This capability allowed Japanese firms to continue investing in R&D and expand capacity during recessions that curtailed U.S. investment. The Japanese then entered the market first for 64-kilobit (64K) and 256K DRAMs, gaining noteworthy competitive advantage.[24]

The U.S. semiconductor industry is dominated by 'merchant' manufacturers who are independently owned and sell their output on the open market. ''Captive" suppliers such as IBM sell the vast majority of their output to their parent company and do not compete on a global basis .25 The merchant portion of the industry has been the source of considerable innovation within the United States. It has achieved low cost production by standardizing designs for many customers' needs. Companies such as Intel, AMD, and TI are not constrained by the capacity of their own systems divisions, but can expand supply to meet market demand. Owners of captive companies often rely on merchant producers to satisfy peaks in their demand.[26] However, merchant companies have often lacked the financial resources to maintain high levels of investment during general recessions.

Trade Practices

Differences in U.S. and Japanese trade practices have allowed Japanese semiconductor manufacturers to gain a strong foothold in the U.S. market while limiting U.S. participation in the Japanese market. Throughout the early 1980s, in particular, the United States did little to regulate or control the import of semiconductor products from Japan. U.S. electronics companies purchased semiconductors from either U.S. or Japanese suppliers, depending on differences in quality or price. But U.S. semiconductor manufacturers alleged that Japanese semiconductor manufacturers used unfair trading practices to gain market share in the United States. The U.S. International Trade Commission (ITC) found that Japanese manufacturers' dumping of 64K DRAMs in the U.S. and other global markets in 1985 inflicted serious damages to U.S. firms.[27] A similar conclusion was reached in the ITC's investigations of the impact of Japanese dumping on U.S. producers of 256K DRAMs and Erasable Programmable Read-Only Memories (EPROMs). Between 1981 and 1982, and again in 1984 to 1985, Japanese dumping of 64K and 256K memories crippled U.S. competitors. The result was a virtually complete withdrawal by U.S. firms from the DRAM market by the end of 1985. Of 11 U.S. merchant firms that produced 16K DRAMs in 1980, only two remained in the market at the 256K level, and these companies accounted for less than 10 percent of world sales.[28]

In contrast, U.S. firms have encountered two types of barriers preventing the sale of their products in Japan: restrictions on investment, and trade barriers. During the 1960s, foreign semiconductor companies were prohibited from establish-

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[w] Ibid, p. *62*.

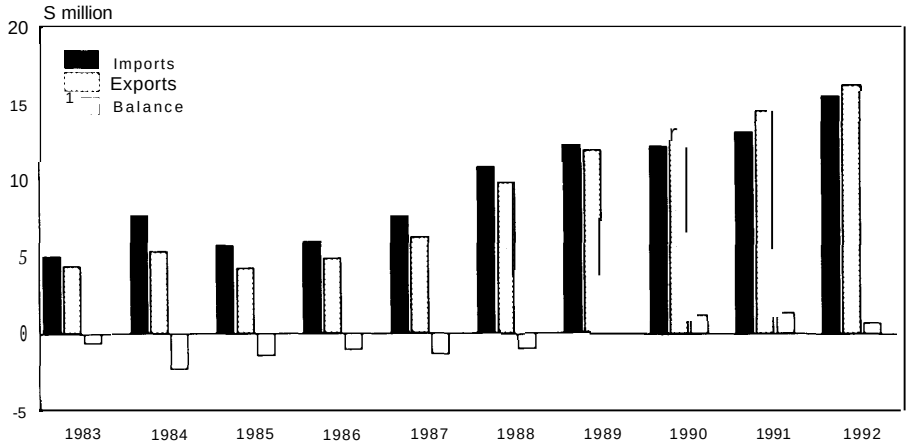
25 IBM recently announced that it will sell ICS on the merchant market. This strategy reflects a corporate restructuring that will disaggregate the company into a larger number of profit centers.

26 National Research Council, Competitive Status *of the US. Electronics Industry (Washington* DC: National Academy Press, 1984), p. 45.

27 U.S. International Trade Commissio, *64K Dynamic Random Access Memory Components from Japan*, PP. 19-20.

28 Semiconductor Industry Association, *Creating Advantage*, Op. Cit., p. 105.

Figure 3-10--U.S. Trade in Solid State Devices



SOURCE: Electronic Industries Association, 1993 ***Edition Electronic*** Market ***Data Book*** (Washington, DC: Electronic Industries Association, 1993), p. 114.

Table 3-3-Market Sizes and Market Shares by Geographic Base of Headquarters, 1991

Market	Size ($B)	Market share by nationality of firm (percent) U.S.	Japan	Other
United States	**$15.4**	70	20	**10**
Japan	**20.9**	**12**	**86**	1
Europe	**10.1**	**45**	**15**	40
Rest **of world**	**8.2**	**43**	**34**	**23**
Total	**$54.6**	**39°A**	**47"/.**	**14%**

SOURCE: Office of Technology Assessment, 1993; based on Semiconductor Industry Association, ***Annual Databook: Global and U.S. Semiconductor Competitive Trends, 1978-1991*** (San Jose, CA: Semiconductor Industry Association, 1992), p. 12.

ing subsidiaries in Japan without prior approval of the Japanese government; consent was usually withheld unless companies agreed to form joint ventures with Japanese fins. U.S. companies had difficulty forming ventures with Japan's major electronics companies because MITI favored alliances between Japanese firms over international joint ventures. In addition, MITI required U.S. firms to transfer technology to their partners as part of the deal.[29]

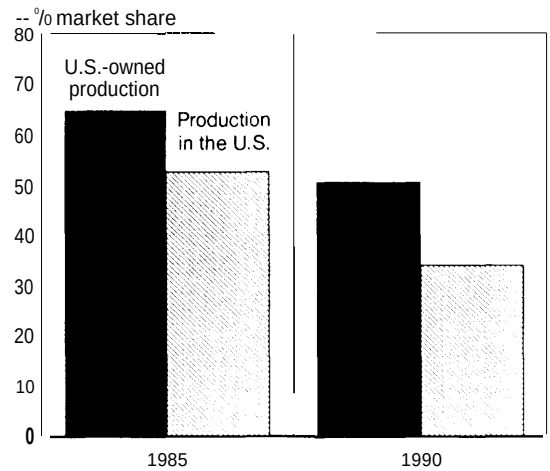
Even with market liberalization between 1974 and 1975, U.S. companies could secure only limited shares of the Japanese market. Japanese semiconductor companies are often divisions of larger conglomerates or of keiretsu that also include producers of electronic goods. These producers tend to purchase components from within their own group, to the detriment of foreign manufacturers. Japanese companies further maintain that U.S. semiconductor firms lack the support and testing facilities of Japanese manufacturers and that U.S. chips have a higher defect rate.[30]

Though dominant in other regional markets, U.S. firms have been unable to penetrate the Japanese semiconductor market and have therefore lost a large share of the total world market (table 3-3). The trade balance has also shifted. Between 1983 and 1987, the U.S. trade deficit in semiconductors increased from $620 million to almost $1.4 billion, due mostly to increasing imports from Japan and stagnant export growth (figure 3-10). Though the United States had run a trade deficit in semiconductors prior to this date,

29 U.S. Congress, Office of Technology Assessment, *Competing Economies: America, Europe, and the pacific Rim,* OP. cit., P. 249.

30 Sheridan Tatsuno, "Japanese Companies Give U.S. Chipmakers A Blunt Opinion of Their Products," *New Technology Week,* Sept. 23, 1991, p. 6.

Figure 3-11—U.S. World Market Share in Electronics Production



SOURCE: American Electronics Association as cited in National Advisory Committee on Semiconductors, ***Attaining Preeminence in Semiconductors, Third Annual Report to the President and the Congress,*** (Washington, DC: National Advisory Committee on Semiconductors, February 1992), p. 21.

it was based mostly on imports from U.S.-owned assembly facilities overseas. Almost 80 percent of all U.S. semiconductor imports were from offshore facilities in 1976.[31] But starting in 1978, the United States began running a growing deficit with Japan. In 1992, the United States imported $4.4 billion in solid-state components from Japan, but exported only $1.5 billion to Japan.[32]

Shifting Location of Downstream Markets

U.S. inability to penetrate the Japanese semiconductor market has been compounded by the tremendous growth of the Japanese market. U.S. semiconductor manufacturers have witnessed a gradual migration of their customer base to Asia. Between 1985 and 1990, the percentage of the world's electronic systems produced in the United States declined from 52 percent to 35 percent (figure 3-1 1). This trend is the result of both the movement of U.S. electronics production out of the United States in search of lower-wage labor and the development of Asia's domestic electronics industry. Growth in electronics manufacturing in Asia has stimulated local demand for semiconductors. As a result, the Japanese market for semiconductors has grown faster than the U.S. market and is now the largest in the world, totaling $21 billion, or 38 percent of the world market, in 1991 (figure 3-12).

Supplier Industries

The success of the semiconductor industry depends on the success of its suppliers: the semiconductor manufacturing equipment and the materials industries. Throughout the 1980s, U.S. materials and equipment suppliers lost market share to foreign competitors. Between 1985 and 1989, the global market share of U.S. equipment suppliers dropped from about 60 percent to almost 40 percent; Japanese suppliers increased their market share from 35 percent to almost 50 percent. In 1980, nine of the top 10 equipment suppliers in the world were U.S.-owned. By 1990, Japanese companies held five of the 10 top slots, including the top two (table 3-4).

U.S.-based materials suppliers proved no more successful, maintaining only 23 percent of the $9.2 billion world market in 1990. Suppliers in Japan captured 64 percent of the market and held the top four slots in terms of total sales. Moreover, much U.S.-based production is foreign-owned. U.S.-owned firms supplied only 13 percent of the total market for materials, and Japanese-owed firms held a 73 percent share.[33] Of the five largest

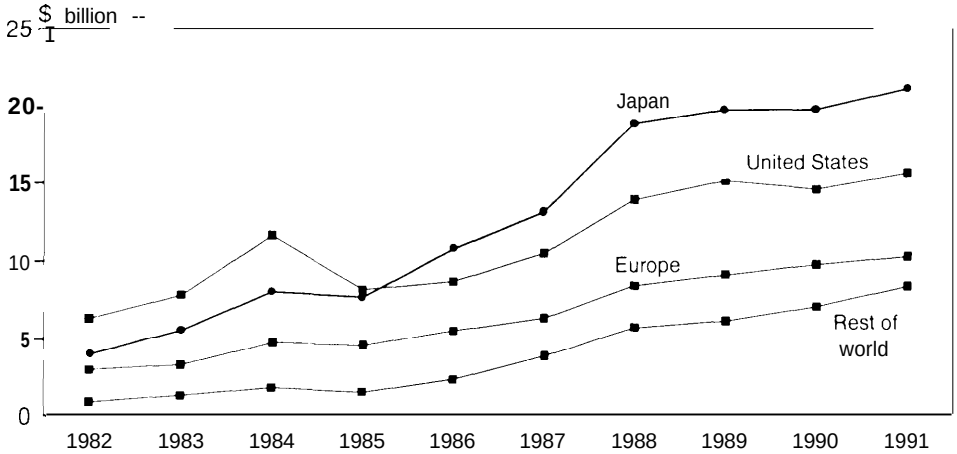
31 U.S. Department of Commerce, International Trade Administration, *U.S. Industrial **Outlook, 2978*** (Washington DC: U.S. Government Printing Office, 1978), p. 308,

32 Electronic Industries Association op. cit., footnote 2, p. 114.

33 U.S. International Trade Commission, *Global Competitiveness of U.S. Advanced Technology Manufacturing Industries: Semiconductor Manufacturing and Test Equipment,* USITC publication 2434 (Washington DC: U.S. International Trade Commission, September 1991), p. 4-15.

34 These suppliers were Kyocera, Shin-Etsu Handotai, NTK, and Sumitomo (all Japanese), and Huels from Germany.

Figure 3-12-Growth of Regional Semiconductor Markets



SOURCE: Semiconductor Industry Association, ***Annual Databook: Global and U.S. Semiconductor*** Competitive ***Trends-1978-1991*** (San Jose, CA: Semiconductor Industry Association, 1992), p. 13.

Table 3-4-Top 10 Semiconductor Equipment Suppliers in Worldwide Sales

1980	Sales	1990	Sales
Company (nationality)	($M)	Company (nationality)	($M)
Perkin-Elmer (US)	151	Tokyo *Electron* (J)	*706*
GCA (US)	116	*Nikon* (J)	*696*
Applied Materials (US)	115	Applied Materials (US)	572
Fairchild (US)	105	*Advantest* (J)	*423*
Varian (US)	90	*Canon* (J)	421
Teradyne (US)	83	*Hitachi* (J)	304
Eaton (US)	79	General Signal (US)	286
General Signal (US)	57	Varian (US)	285
Kulicke and Soffa (US)	47	Teradyne (US)	215
Takeda Riken (J)	46	SVG (US)	204
Total	$888	Total	$4,108

NOTES: US = United States; J = Japan.

SOURCE: SEMATECH, "Strategic Overview," December 1991, p 1-7; data from VLSI Research.

suppliers in 1990, four were Japanese and the fifth was German.[34]

Moreover, the fragmented structure of the U.S. semiconductor industry permeates the supplier industry as well. Throughout the 1980s, U.S. semiconductor manufacturers maintained arms-length relationships *with their* primary suppliers. In contrast, Japanese manufacturers maintained closer linkages to their suppliers. This enabled Japanese manufacturers to gain early access to new production equipment and to influence its design.

The U.S. Response

The loss of U.S. share in the memory market to Japan triggered alarms throughout industry and government in the United States. Though a commodity good with low profit margins, DRAMs were considered the primary technology driver for the entire semiconductor industry throughout

the 1980s.[35] The design of DRAMs is fairly straightforward compared with microprocessors and other logic devices, but in order to achieve greater capacity, transistors must be packed more closely together. The design of next-generation DRAMs therefore precipitates advances in lithography and manufacturing capability for achieving higher device densities and smaller linewidths. Logic devices typically lagged behind DRAMs in these areas. In addition, the large volumes characteristic of DRAM production allow for greater evaluation and refinement of production techniques. With large production runs, the effects of process changes upon yield can be more easily determined and the learning that manufacturers gain can be applied to other types of devices manufactured with a similar process. High-volume production also provides manufacturers a way of amortizing the cost of new fabrication facilities (or fabs), which can then be converted for use in manufacturing other devices, such as logic, and for gaining experience with new processes.

Faced with the prospect of continuing its downward slide in market share, the U.S. semiconductor industry took serious measures in the 1980s to regain its international competitiveness. Central to these efforts have been industry collaboration and government cooperation. Government and industry have become partners in reinvigorating an industry that is often considered a strategic national asset. Industry participation has been coordinated primarily by the Semiconductor Industry Association (SIA), an organization that, since its inception in 1977, has gained considerable political influence and has come to represent its member companies effectively. SIA has worked with the federal government to stimulate U.S. research in semiconductor technology, ameliorate trade frictions, and strengthen linkages between semiconductor manufacturers and their suppliers. These efforts have resulted in the formation of the Semiconductor Research Corporation (SRC), SEMATECH, and a series of Semiconductor Trade Agreements (STAs) with Japan.

Semiconductor Research Corporation

SRC was founded in 1982 as an industry-led consortium to coordinate and fund basic university research in technologies of interest to the semiconductor industry. Membership in SRC has grown rapidly to some 70 organizations in 1992. Most members are individual corporations who contribute a freed portion of their total revenues, but other members are government agencies and government/industry consortia, such as SEMATECH and the Microelectronics and Computer Technology Corporation (MCC).[36] With a small staff in Research Triangle Park, North Carolina, SRC manages an external research budget of about $30 million per year. These resources are dedicated to three complementary missions: to support research in universities bearing on long-range industry needs; to increase the flow of graduate students with direct experience related to mainstream interests of the semiconductor industry; and to stimulate interest among university faculty in silicon-related activities and thereby increase the demand for government research support in this area.

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35 Only recently has this notion been challenged. LSI Logic, Inc. has developed a 0.6-micron process for manufacturing ASICs that rivals state-of-the-art DRAM factories, convincing many analysts that DRAM production is not the only way to drive improvements in manufacturing processes.

36 As of 1992, SRC had 26 full and 33 affiliate members from industry three associate members from Los Alamos National Laboratory, the Microelectronics and Computer Technology Corporation and SEMATECH; and seven members from government, including the National Science Foundation, NIST, the National Security Agency, and other Department of Defense research organizations, who collectively support one full membership for the U.S. government. lb apply for full membership in SRC, companies must manufacture, use, or sell semiconductors. Affiliate and associate members must conduct R&D in support of semiconductor devices within the United States or Canada. Affiliate and associates members do not have representation on the board of directors.

SRC's contribution to university research is evident. Between 1982 and 1992, SRC funded $200 million in university research contracts, supporting hundreds of faculty members and thousands of graduate students. This research generated over 8,000 published reports and 41 patents, with another 38 patents filed.[37] Member firms have access to all these research findings and results. More importantly, SRC finding has helped create interdisciplinary university research programs on silicon-based devices. Though comprising over 90 percent of industry sales, silicon devices received little attention by university researchers a decade ago; the limited semiconductor research at universities was aimed at compound materials (such as gallium arsenide), which have unique electrical properties and are of particular interest to DoD, but have fewer commercial applications.[38] SRC funding now represents about half of all U.S. support for silicon semiconductor research at universities and research institutes.

Transferring research results to industry has not always been easy. Most research projects need further work before they can be commercialized. In addition, finding the appropriate end-user for a specific technology can be difficult. Nevertheless, in 1992, SRC created a new Technology Insertion Program to help move SRC research results into participating companies. These programs are aimed at improving SRC's transfer of technology to industry.

Despite the difficulty with technology transfer, SRC has been highly effective in training personnel for careers in the semiconductor industry and in stimulating personnel exchanges between industry and universities. Member companies are encouraged to send technical personnel to university research centers for extended periods of time to gain exposure to advances in academic research. In addition, members often use their access to students as a means of selecting future employees. Over 1,000 of SRC's graduate students have been hired by industry, bringing with them intimate knowledge of new semiconductor processing techniques.

As a consortium, SRC has also played a key role in helping industry reach consensus on a number of issues. Through its advisory boards, sponsored workshops, and planning documents (like SRC 2001), SRC has developed early industry roadmaps and research agenda for key technologies. These tools have helped SRC raise national interest in issues of importance to the semiconductor industry and attract government attention to industry problems. Furthermore, by maintaining management control of industry's university research funding, SRC has not only advanced a close match between university efforts and industry needs, but has also reduced duplication of research efforts. Though overlap can lead to different and useful results, the high cost of research in the semiconductor industry makes elimination of redundancy a necessity. SRC's success in these areas is widely credited with strengthening the global competitiveness of the U.S. semiconductor industry and improving relations between government, industry, and academia.

SEMATECH

The federal government has also supported SEMATECH, a consortium founded by 14 member companies in 1987 to help U.S. manufacturers recapture world leadership in the semiconductor industry. The group, with facilities and staff at its headquarters in Austin, Texas, proposed to meet this goal by developing within five years a process for manufacturing chips with 0.35-micron feature size on 8-inch wafers. In Decem-

37 *Semiconductor Research* Corporation, *A Decade of Service to the Semiconductor Industry: 1992 Annual Report* (Research Triangle Park, *NC:* Semiconductor Research Corporation 1992), p. 2.

38 Markets for compound semiconductors are growing, however. Gallium arsenide ICs are now widely used in wireless communications systems; compound semiconductors are used as laser sources in telecommunications systems and compact disc (CD) players.

ber 1987, Congress authorized DoD to provide SEMATECH with five years of funding at a level equal to industry's contribution, expected to be $100 million per year. DoD assigned ARPA responsibility for working with SEMATECH in April 1988.

SEMATECH originally planned to create new production processes in-house for manufacturing next-generation semiconductors, but later decided that its primary goal should be to develop a strong base of semiconductor manufacturing equip ment suppliers. Without strong suppliers, U.S. semiconductor manufacturers could not keep up with their Asian competitors, who have closer contacts with Japanese equipment makers and thus have earlier access to the most advanced Japanese semiconductor manufacturing equipment. At SEMATECH's inception, U.S. semiconductor equipment suppliers were losing market share at the rate of 3.1 percent per year.[39] Semiconductor manufacturers expected to purchase less than 40 percent of their submicron equipment from U.S. suppliers.[40]

SEMATECH established a number of partnerships with U.S. equipment manufacturers to help them develop next-generation production tools. It also brought the semiconductor industry toward consensus as to its future requirements, especially for new semiconductor manufacturing equipment. As a result, equipment manufacturers have been able to produce equipment to one set of industry specifications rather than to diverse company specifications. In addition, SEMATECH has standardized methodologies for evaluating candidate manufacturing technologies, both analytically and experimentally. Perhaps most important, SEMATECH's Partnership for Total Quality program has improved communications between semiconductor manufacturers and their suppliers. While some suppliers had previously maintained close relationships with preferred customers, SEMATECH replaced and repaired those that had been severed and created a much broader set of ties. In this way, information that is not easily quantified can be exchanged directly between users and suppliers of manufacturing equipment.

While critics claim that SEMATECH has benefited only its member companies, others credit the consortium with contributing to the recent improvement in the health of the entire semiconductor equipment industry. Since 1990, equipment manufacturers have reversed their declining market share and currently command 53 percent of the world market, versus 38 percent for Japan.[41] U.S. semiconductor manufacturers now purchase over 70 percent of their equipment domestically. Motorola's new wafer fabrication facility in Austin, Texas, which was originally planned to include 75 percent foreign tools, now has an 80 percent U.S. tool set.[42] Production yields of U.S. semiconductor manufacturers, which were 60 percent versus Japan's 79 percent in 1987, have improved to 84 percent versus 93 percent in Japan.[43] U.S. equipment manufacturers have also increased their market share in Japan, commanding almost 20 percent of the Japanese equipment market in 1992, up from 15 percent in 1990.[44]

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39 Peter Burrows, "Bill Spencer Struggles to Reform SEMATECH," *Electronic Business,* May 18, 1992, *p.* 58.

40 SEMATECH, *1991 Annual Report,* p. 2.

41 Data from VLSI Research Inc. as cited by Peggy Haggerty, Vice President, Public Policy and Administration, SEMI/SEMATECH, personal communication, July 20, 1993.

42 SEMATECH, 1991 *Annual Report,* p. 18

43 Us. General Accounting Office, "Federal Research: SEMATECH's Technological Progress and Proposed R&D Program," GAO/RCED-92-223BR, July 1992, p. 10.

44 Data from VLSI Research Inc. as cited by Peggy Haggerty, Vice President, Public Policy and Administration, SEMI/SEMATECH, personal communication% July 20, 1993.

Bilateral Trade Agreements

Other than its participation in SRC and SEMATECH, much of which was justified on the basis of national security, federal attempts to boost the competitiveness of the civilian semiconductor industry have been limited almost exclusively to trade considerations. Government polices have been designed to level the playing field by reducing foreign trade barriers and curbing unfair trade practices-specially dumping—that have injured U.S. semiconductor manufacturers. Trade frictions have been characteristic of the semiconductor industry since the early 1980s, when U.S. manufacturers began complaining of difficulties entering the Japanese market and accusing Japanese firms of dumping products in the United States.

The federal government frost attempted to redress these grievances through the negotiation of a bilateral agreement with Japan in 1983, after imports of low-cost 16K and 64K DRAMs from Japan inflicted heavy losses on U.S. manufacturers. While the agreement contained several recommendations to promote U.S. access to the Japanese market and halt dumping, it lacked proper enforcement and by 1985 was defunct, as U.S. market share in Japan plummeted and Japanese companies began dumping 256K DRAMs and EPROMs in the United States.[45]

A second attempt was made after U.S. manufacturers and the U.S. Department of Commerce filed antidumping suits against Japanese firms in 1985, and the SIA filed a petition for retribution against manufacturers who were eventually found guilty of dumping. Through the Semiconductor Trade Agreement of 1986, the United States attempted to sway Japanese producers to sell at cost-based prices and to ensure U.S. manufacturers enhanced access to Japanese markets. A separate side letter to the STA sought commitments by Japan to encourage its semiconductor manufacturers to increase purchases of U. S.-produced semiconductors, with the goal of increasing the foreign share of the Japanese market to at least 20 percent by the end of 1991.[46] Nevertheless, few steps were taken to implement this requirement, and in April 1987 President Reagan announced formal sanctions against Japanese electronics producers. This action, coupled with prospects that Japan might be labeled a priority country under the Super 301 provisions of the Omnibus Competitiveness Act of 1988 and be subject to retaliatory actions by the United States, induced significant changes in Japan's attitude toward the STA. Efforts were soon undertaken to boost foreign sales, including the formulation of market access plans and specific company promises of increased purchases.

The 20 percent target was not reached by 1991, but given signs of improvement, the SIA and the Computer Systems Policy Project lobbied the U.S. government to negotiate anew semiconductor agreement with Japan. Under this accord, Japan agreed to reach the 20 percent mark by the fourth quarter of 1992. By the fourth quarter of 1992, U.S. companies had achieved 20.2 percent, though market share declined the following quarter. Despite efforts by the Clinton administration to get further firm, numerical commitments of market share, many U.S. companies thought such measures unnecessary because they had already become an integral part of Japanese supply networks.

FUTURE CHALLENGES TO THE U.S. SEMICONDUCTOR INDUSTRY

While the efforts of the U.S. government and industry have been somewhat successful in enhancing the competitiveness of U.S. semiconductor industry, additional efforts will undoubtedly

45 Thomas Howell, op. cit., footnote 15, p. 102.

46 According to the SIA, the Japanese government originally denied the existence of the side letter and later argued that while committing them to encouraging Japanese companies to increase foreign purchases, it did not commit them to impose numerical procurement quotas on companies.

be necessary. U.S. manufacturers may have regained market leadership in semiconductors and equipment, but Japanese competitors will likely reassert themselves in the near future. Much of the recent slowdown in Japanese semiconductor production is the result of a serious recession that has reduced local demand for semiconductor products. A resurgence of demand could boost production and Japanese market share once again.

U.S. and Japanese semiconductor manufacturers will be faced with a number of additional challenges over the next decade. Industry will need to surmount many technological obstacles in both semiconductor design and manufacture in order to meet future requirements for more complex, sophisticated integrated circuits. At the same time, the industry will have to face increasing costs for R&D and production that could threaten the ability of individual manufacturers to meet their goals.

Technology

Future integrated circuits will offer considerable advantages over existing ICs. Although the specific path of technological development cannot be accurately predicted more than a few years into the future, realistic predictions can be made on the basis of historical trends in IC capability. Since 1959, the number of components per circuit in the most advanced integrated circuits has doubled every year, following a trend line referred to as Moore's Law.[47] This trend reflects two underlying processes: continued reductions in the size of individual devices (e.g., transistors) on each chip-which thereby allow more devices to be packed into each square centimeter of chip-and the simultaneous increases in the size of each die (or chip) .48

As of 1992, state-of-the-art manufacturers could produce 4M DRAMs containing over 300,000 gates per chip on 132-mm^2 chips using 0.5-micron feature sizes. In order to stay on the Moore's Law curves, by the year 2007 they will have to produce 16-gigabit (G) DRAMs containing over 20 million gates on 1,000 mm^2 chips with O.10-micron feature sizes.[49] Future ICs will have greater power demands and will be able to operate on just 1.5 volts of electricity versus the 3.3 to 5 volts required of current portable and desktop systems. Maximum operating speeds will rise from 120 megahertz (MHz) to 1,000 MHz, allowing faster computation. Other criteria will also improve (table 3-5).

Achieving these specifications in the timeframe indicated will require industry to overcome numerous technical hurdles. A recent workshop sponsored by the SIA and attended by representatives of the semiconductor industry, its suppliers, government, and the national labs, analyzed the technological advances necessary to achieve these goals, in keeping with the Moore's Laws projections. The results of this workshop represent a consensus view on industry needs and requirements for the next 15 years. The group identified 11 major areas in which technical progress will be critical (table 3-6). While each area presents a number of difficulties, lithography may prove the most critical (box 3-A). Workshop participants also identified eight cross-cutting competencies that pervade these 11 technology areas. Advances in these specific competencies, outlined below, will allow further progress in the technology areas.

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47 Moore's Law is named after Gordon E. Moore who first noted the trend in 1964 and predicted it would continue. Robert N. Noyce, "Microelectronics," *Scientific American,* September 1977.

48 U.S. Congress, Office of Technology Assessment, *Miniaturization Technologies,* OTA-TCT-514 (Washington, DC: U.S. Government Printing Office, November 1991), p. 13.

49 Semiconductor Industry Association, *Semiconductor Technology: Workshop Working Group Reports,* (San Jose, CA: Semiconductor Industry Association, 1993), p. 3.

Table 3-5—Overall Roadmap Technology Characteristics

Characteristic	1992	1995	1998	2001	2004	2007
Feature size (microns)	0.50	0.35	0.25	0,18	0,12	0.10
Gates per chip (millions)	0.3	0.8	2.0	5.0	10.0	20.0
Bits per chip						
DRAM	16M	64M	256M	1G	4G	16G
SRAM	4M	16M	64M	256M	1G	4G
Wafer processing cost ($/cm^2)	$4.00	3.90	3.80	3.70	3.60	3.50
Chip size (mm^2)						
logic	250	400	600	800	1,000	1,250
memory	132	200	320	500	700	1,000
Wafer diameter (mm)	200	200	200-400	200-400	200-400	200-400
Defect density (defects/cm^2)	0.10	0.05	0.03	0.01	0.004	0.002
Levels of interconnect (for logic)	3	4-5	5	5-6	6	6-7
Maximum power (watts/die)						
high performance	10	15	30	40	40-120	40-200
portable	3	4	4	4	4	4
Power supply voltage						
desktop	5	3.3	2.2	2.2	1.5	1.5
portable	3.3	2.2	2.2	1.5	1.5	1.5
Number of 1/0's	500	750	1,500	2,000	3,500	5,000
Processing speed (MHz)						
off chip	60	100	175	250	350	500
on chip	120	200	350	500	700	1,000

NOTES: DRAM . Dynamic Random Access Memory; SRAM - Static Random Access Memory; I/O - input/output.

SOURCE: Semiconductor Industry Association, ***Semiconductor Technology Workshop Reports*** (San Jose, CA: Semiconductor Industry Association, 1993), p. 3.

Materials

There is a critical need for a wide range of high-quality materials for the IC industry, but, to date, industry has undertaken little coordinated materials research. Materials needs include improvements in all feedstock materials, including silicon wafers; wet and dry chemicals used for etching and cleaning; construction materials for equipment and plant; consumables such as resists, masks, ceramics, glasses, metal sputtering targets; packaging materials; and advanced substrate materials (insulators such as glass) on which groups of ICs can be produced and interconnected. Specific needs for substrate materials include dielectrics that are effective insulators at thicknesses of just 50 angstroms; materials for storage cells and capacitors; materials that can be integrated with highly conductive metals for interconnects; and materials for encapsulating and protecting bare chips.

New materials can Provide a competitive advantage for fabrication equipment. Of particular importance may be surface-treated materials for use in construction of etch chambers and other corrosive environments and special materials such as those used in construction of electrostatic chucks.

Metrology

Advances in the ability to measure the results of processing operations are essential to maintain the close production tolerance needed by future

Table 3-6-Technical Areas Identified in SIA Roadmaps

Technical area	Required advances
Chip design and test	Enhanced computer-aided design tools to help engineers design ICs with more devices and complicated interconnections.
Lithography	Reductions in the linewidth and overlay capabilities to allow smaller devices to be drawn on a semiconductor (processes other than photolithography such as x-rays, electron beams, or ion beams may be needed); compatible mask and resist technologies.
Materials and bulk processes	Improvement in processes used for creating oxides and depositing films on the semiconductor wafer; advances in temperature control, mass flow control, materials purity, and modeling of bulk processes.
Manufacturing systems	More robust systems to handle increased volume of data used in lot scheduling and planning, wafer tracking, work-in-process control, failure analysis support, cost accounting, purchasing, and capacity planning; new software tools for managing flexibility in the factory configuration, including process equipment, product mix, and manufacturing technology,
Process/device/structure CAD	New computer-aided design tools to model new processes, circuits, factory equipment, and manufacturing systems; 3-D models to characterize processes such as ion implantation and diffusion. Use of such models will help limit the amount of experimentation needed to bring new processes on-line,
Equipment modeling and design	Advances in models of manufacturing tools for lithography, plasma etching, thermal processing, and epitaxy to allow design of new tools that can reduce base equipment costs, reduce time-to-market through integrated design tools, and improve predictability of performance.
Device/process integration	Progress along the Moore's Law curves will require continued attention to troth front-end (design) and back-end (assembly and test) issues. Advances in process integration will ensure the compatibility of progress in these two areas.
Interconnect	Advances in dielectric and metal film formation and etch processes to allow multiple layers and more complex patterns of interconnection, and therefore higher operating speeds and chip densities.
Environmental safety and health	Means to limit the use of chemicals and processes that are harmful to human health and the environment, or to reduce the risk associated with their use.
Packaging	Advances in the packages that house ICs to ensure the integrity of the electrical signals and the power provided to the chip.
Manufacturing facilities	Advances in wafer handling systems and raw materials systems (for wafers and gases); development of smaller "micro-fabs" that can efficiently produce small batches of wafers, yet be scaled up for mass production, and the manufacturing tools required to support them.

SOURCE: Office of Technology Assessment, 1993; based on Semiconductor Industry Association, *Semiconductor Technology* Workshop ***Reports*** (San Jose, CA: Semiconductor Industry Association, 1993).

Box 3-A–Advances in Lithography

Central to future advances in semiconductor manufacturing will be advances in lithography. Lithography is the primary technology driver for boosting the performance of integrated circuits. Lithography includes exposure, resist processing, coating and developing, masks, and their associated processing. It is also the dominant cost factor in semiconductor fabrication, accounting for 35 percent of the processed wafer cost,

Table 3-7—Requirements for Lithography Systems

	1992	1995	1998	2001	2004	2007
Leading Edge DRAM size (bits)	16M	64M	256M	1G	4G	16G
Resolution (rim)	500	350	250	180	120	NA
Overlay (nm)	150	100-200	75-95	50-70	35-50	NA

NOTES: M = megabits; G = gigabits; nm = nanometers; NA = not available.

SOURCE: Semiconductor Industry Association, *Semiconductor Technology Workshop* Reports (San Jose, CA: Semiconductor Industry Association, 1993), p. 37.

In order to further reduce the size of the individual devices on an integrated circuit, continued improvement will be needed in both the resolution and overlay capabilities of lithography systems (table 3-7). Resolution determines the width of the smallest line that can be etched into the silicon wafer. Overlay capability refers to the ability of the system to properly align subsequent layers of integrated circuit on top of those below it. Both depend strongly on the wavelength of light used in the *exposure* **(shorter wavelengths allow higher resolution for narrower linewidths) and on the method used to project the light onto the wafer. In projection lithography systems, a mask about five times the size of the desired pattern is placed between the light source and the wafer and is focused by a series of lenses onto the wafer below. In direct overlay or proximity systems, a mask the same size as the desired integrated circuit is placed directly over the silicon wafer and exposed to the light. Projection systems allow greater resolution and overlay capability and are used in most current systems, but may require sophisticated optics for future, higher-resolution systems.**

(continued *on next page*)

IC technology. Lithography process control, for instance, requires that lines and spaces be measurable to within one-third of the minimum dimension. The present realistic capability for wafer measurements is O.15 micron. Therefore, new measurement methods must be developed to control processes with critical dimensions less than 0.5 micron to ensure adequate process control.

Measurement capability also limits process characterization. For example, surface measurements required to evaluate materials growth and etch processes limit modeling and characterization of these important processes. The inability to accurately analyze residual gases in process chambers is a major impediment to understanding chemical plasma processes. Similarly, metrology limits the device structure evaluation; today's methods for measuring vertical device structures cannot accurately resolve the sharp impurity gradients of the shallow junctions used in 0.25-micron processes.

Advances in metrology are necessary for improvements in contamination control. Present measurement techniques are capable of detecting 109 (one billion) heavy metal contaminant atoms per cm^2. Process controls required to achieve competitive process yields 15 years from now will require detection of 10^7 (ten million) atoms per cm^2. Advanced IC fabrication requires meas-

Box 3-A--Advances in Lithography--Continued

Current production-level lithography systems operate at optical wavelengths of light, typically either 436 nanometers (G-line) or 365 nanometers (I-line), generated by mercury vapor lamps. They yield a resolution of about 0.5 micron. Smaller linewidths will require shorter wavelength light, in the "deep ultraviolet" portion of the spectrum (248 or 193 nanometers), generated by excimer lasers. These wavelengths could generate linewidths as narrow as 0.18 microns, but difficulties in narrowing the depth of focus and diffraction could limit their applicability y past 0.25 microns. Alternative technologies may need to be sought.

One possibility is x-ray lithography, which uses significantly shorter wavelengths of light (about 5 nanometers), but otherwise operates much like an ultraviolet system. Proximity x-ray systems have been studied for several years, but require a bright source of x-rays such as a synchrotrons and cannot offer the resolution of projection systems. The latter constraint could limit proximity x-rays from being used past 0.18 microns. More recently, research has begun to focus on projection x-ray systems, which could offer linewidths of 0.12 micron or less and rely on less expensive sources of x-rays. Development of such systems would require significant advances in the manufacture of the necessary optics, a process that requires the creation of multiple-layered films with precisely controlled thickness.

Alternatively, smaller linewidths could be achieved with electron beam or ion beam techniques in which beams of high-energy electrons or charged particles (ions) are fired at the surface of the wafer. E-beams have demonstrated resolution as small as 2 nanometers in certain materials in a laboratory setting,[1] but are limited in their applicability to full-scale production lines because they can draw lines only one at a time. Ion beams can generate linewidths as small as 100 nm, but, as with e-beams, must be scanned across the entire wafer surface one step at a time. Research is being conducted on methods for increasing the throughput of such direct-write systems, but is still in the early stages.

[1] U.S. congress, Office of Technology Assessment, *Miniaturization Technologies*, OTA-TCT-514 (Washington, DC: U.S. Government Printing Office, November 1991), p. 37.

urement capabilities consistent with tight process controls. Advances in the science of measurement (i.e., metrology) are important to both semiconductor producers and equipment suppliers.

Sensors For Process Control

New low-cost, reliable, and sensitive sensors are necessary to increase the rate of learning in tool development, reduce the time to market for process equipment, improve tool and process controls, increase process yield, and reduce defects.

Greater use of real-time, in situ sensors is driven by economics. Sensors are the critical elements in closed-loop process control and are necessary for detecting process problems when they occur, so that corrective actions can be taken immediately. Sensors are also required to improve frost-pass success when introducing process variations.

Accurate control of even such commonly used processes as rapid thermal processing (RTP) and plasma deposition and etch requires new sensor approaches. The technique used to control todays RTP equipment (called back surface emission), for instance, leads to 50 to 200 degree Celsius temperature errors. Reliable RTP control requires new temperature sensors that are more accurate and more responsive to real-time front surface conditions.

Sensors that monitor gas and chemical purity and cleanliness are also of major concern. Gas analyzers, mass controller calibrators, chemically

selective sensors, and particle detectors are all essential to maintain process cleanliness. Environmentally conscious manufacturing will require recycling and reuse of chemicals not only to minimize waste, but also to reduce cost. Chemical generation and reuse will require sensors that can detect impurities at a parts per billion level for on-line monitors of chemical purity.

Modeling and Simulation

IC technology has developed faster that the capability for modeling and simulating its various elements. Cost and complexity of IC fabrication make the acquisition and application of advanced modeling and simulation tools an imperative.

Computer-based modeling and simulation have become essential in all areas of semiconductor technology. Models are now used for materials, devices, and processes, as well as for circuits and systems. In addition, entire fabrication equipment systems—from process chambers and wafer handling systems to the design and operation of complete factories-require modeling and simulation.

The physics base for models is still incomplete. Today's modeling and simulation tools are unreliable, incompatible with one another, and unable to cover the entire range of requirements. But, modeling and simulation are critical to the IC industry because of the need for faster implementation of error-free designs for chips, systems, and factories. Modeling and simulation have pervasive applicability and provide the tools necessary in the design, test, and production of materials, equipment, processes, factories, devices, systems, packages, circuits, and ICs.

The highly complex task of developing suitable models requires a vast range of skills, from physics and chemistry to electrical/mechanical engineering and computer science. These skills are developed in environments such as national laboratories, universities, computer systems producers, and the semiconductor industry.

Reliability and Quality

Existing manufacturing methods do not ensure reliability and quality of complex semiconductor products, particularly where the physical limits of the materials, processes, and structures are challenged. In submicrometer structures, processes and structures are being pushed to the physical limits of breakdown voltage, interconnect current-carrying capacity, stress, defect and contamination levels, alignment errors, and noise margins. Shallow junctions, trenches, stacks, capacitors, new device architectures, and ultra-thin interconnect lines each introduce new failure possibilities.

Commercial success of semiconductor technology in all applications depends on reliable, long-term performance to specification. With current technologies, however, the reliability of submicrometer devices cannot be determined in advance. A systematic approach to reliability engineering must be therefore be developed. Standard test environments, based on design rules and fabrication conditions, must be available to the entire IC community. Standard tests applied to standard test structures will simplify the interpretation and comparison of the resulting data. As they affect reliability, the roles of microstructure, topography, and stress must be determined. Both empirical and fundamental models must be developed and experimentally confined. Techniques such as design-for-reliability and an understanding of the relationships between process contamination and reliability are essential to a systems approach to reliability and quality.

Contamination-Free Manufacturing (CFM)

Impurities and particles are unintended contaminants in all IC manufacturing steps. Sources of contamination, which include processing materials (including chemicals and gases), process chambers, wafer handling systems, and facilities, contribute to reduced IC process yields. As products and process complexity increase, the size and density of defects or impurities must be substantially decreased.

IC producers expect to achieve yields close to 100 percent to meet cost and reliability goals. This requires processes, materials, equipment, and new fabrication facilities to be defect-free. A clear understanding of the generation, detection, and elimination technologies for unwanted impurities and particulate is critical.

Manufacturing-Critical Software Engineering

IC manufacturing process equipment is increasingly regulated by software-programmed controllers. Software failures are a major problem for today's fabrication equipment. This problem will worsen with greater equipment and factory automation. Provisions for the creation, upgrade, and maintenance of equipment and factory software are essential.

Improved software design for reliability and testing is key to efficient maintenance and reduced equipment failure rate. Developers of equipment control architectures must look beyond immediate applications to include expandability for future applications. Self-testing codes, modular structures to provide flexibility, use of efficient high-level languages, noise immunity, and interrupt timing standards are all important to improve software performance and reliability in the semiconductor factory. Other manufacturing-critical software-related issues include manufacturing databases, logistics planning, and factory and equipment control. These factory system applications must interact closely with equipment.

costs

The technical challenges outlined above will not only stretch the scientific and engineering talents of U.S. semiconductor manufacturers, they will also stretch their financial resources. R&D and production facilities are becoming more costly to the semiconductor industry, and without a radical change in manufacturing technology will continue to rise on their current trend lines. With product life cycles as short as three or four years for most semiconductor products, large investments in R&D and capital must be continually maintained. Although costs of capital seem to be converging in the United States and Japan, U.S. manufacturers may still beat a disadvantage compared with international rivals who often receive direct government support of commercial technology development and whose industry structure is more tolerant of large investments with longer payback periods. In the absence of other mechanisms, U.S. companies may be forced to enter into more strategic alliances to pool resources with other companies, both at home and abroad.

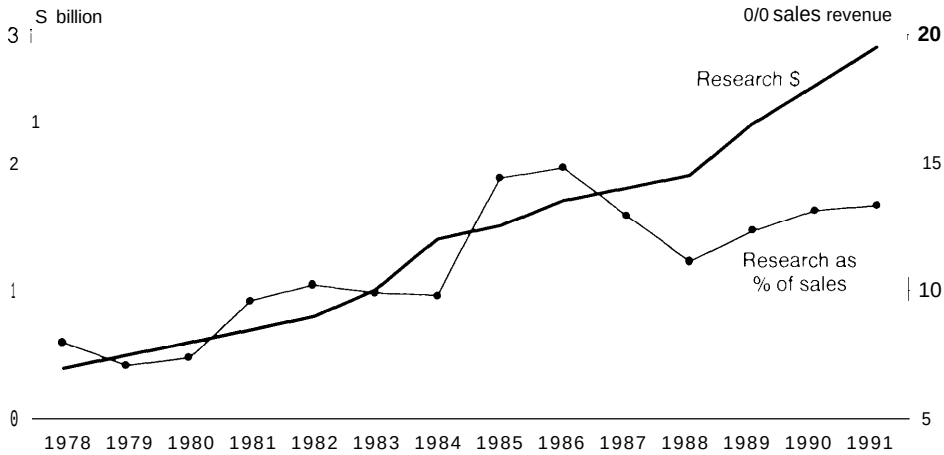
R&D

In order to remain competitive, U.S. manufacturers will have to maintain high levels of spending on R&D. The rapid pace of innovation in the semiconductor industry requires such investments to support new product and process development. As competition has grown, U.S. companies have been forced to increase their R&D spending. Between 1980 and 1991, annual R&D expenditures by U.S. merchant producers increased by a factor of five, from $600 million to $2.9 billion. This growth in R&D has far outpaced gains in sales revenues, reflecting the increasing R&D intensity of semiconductor manufacturing. As a result, R&D expenditures as a percent of sales increased from 7.4 to 13.3 percent since 1982 (figure 3-13). The semiconductor industry is now the most R&D-intensive of all major industrial sectors except computer software and services (figure 3-14).

Production Facilities

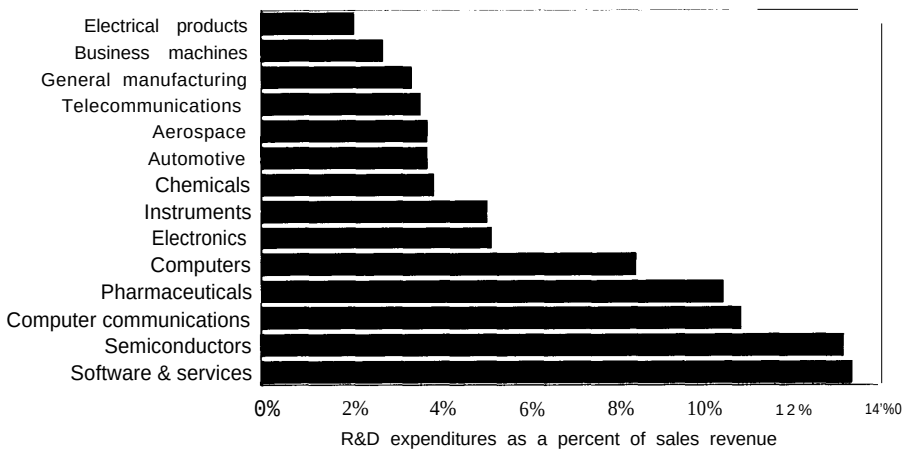
Cost for new production facilities are likely to continue growing over the next decade. Due to rising equipment costs and the increasing number of processes required for each new generation of semiconductor chip, the cost of a state-of-the-art wafer fab has risen from $25 million in 1989 to over $500 million in 1992, and is expected to

Figure 3-13—Sales Revenues and Expenditures on R&D in the U.S. Semiconductor Industry



SOURCE: Semiconductor Industry Association, *Annual Databook: Global and U.S. Semiconductor Competitive Trends—1978-1991* (San Jose, CA: Semiconductor Industry Association, 1992), p. 41.

Figure 3-14—R&D Expenditures in Key Sectors of U.S. Industry



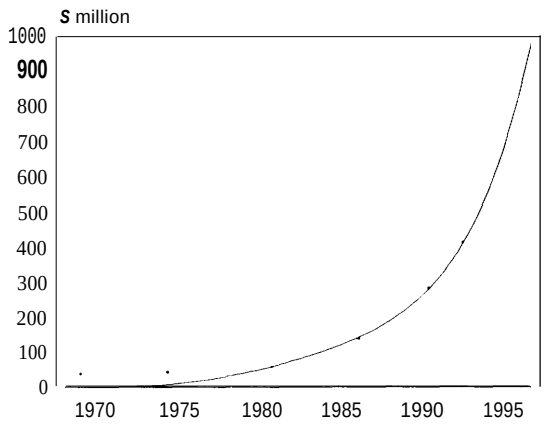
SOURCE: Semiconductor Industry Association, ***Annual*** Databook: *Global and U.S. Semiconductor Competitive Trends—1978-1991* (San Jose, CA: Semiconductor Industry Association, 1992), p. 42.

exceed $1 billion by 1995[50] (figure 3-15). About 75 percent of this cost is associated with fabrication equipment as opposed to land and buildings.[51] Processing a typical wafer now requires over 300 steps, conducted on hundreds of pieces of semiconductor manufacturing equipment, each of which can cost between $200,000 and $3 million, and each of which must be maintained in a clean environment that allows fewer than one O. 15-micron particle per cubic foot.

50 Wafers are disks of silicon on which hundreds of semiconductor chips are simultaneously produced.

51 Semiconductor Industry Association, *Annual Databook: Global and U.S. Semiconductor Competitive Trends, 1978-1991 (San Jose,* CA: Semiconductor Industry Association, 1992), p. 38.

Figure 3-15-Growing Cost of a Wafer Fabrication Facility



SOURCE: Arati Prabhakar, **Advanced Research** Projects Agency, "Flexible Intelligent Microelectronics Manufacturing," **briefing** to OTA on June 15, 1993.

Moreover, the rapid pace of technological innovation in the semiconductor industry requires companies to make these large investments in plant and equipment on a regular basis. New facilities may become outdated after only three years of operation. While they may then be used to produce other types of devices that do not rely on state-of-the-art processes, much of the equipment cannot be modified for next-generation chips. The advantages gained by being first to market (cost reduction through learning curves, market expansion) pressures companies to bring new facilities on-line rapidly.

Some alleviation of cost and economy of scale considerations could be achieved with more flexible manufacturing equipment. ARPA recently completed a program entitled Microelectronic Manufacturing Science and Technology (MMST) that investigated the economic benefits of flexible manufacturing systems to semiconductor manufacturers and developed rudimentary systems for flexibly processing small batches of wafers. Such technologies appear capable of reducing the economies of scale necessary for an efficient plant, but are applicable primarily to small batch manufacturing and will thus remain outside the purview of mainstream semiconductor manufacturers for some time.

ALTERNATIVES FOR FUTURE R&D

The high costs associated with continued success in the semiconductor industry are rapidly exceeding the financial capabilities of individual companies. Moreover, the long-term nature of the required investments exceeds the planning horizons of most U.S. corporations. In recent years, many companies have redirected their research dollars to short-term projects focused on near-term product development. The two U.S. companies that had formerly filled the gap between university research and corporate product development by focusing on initial prototype development, IBM and AT&T's Bell Laboratories, have redirected their R&D dollars to link research programs more closely to product development activities.

In order to make up for this growing deficiency, semiconductor companies have entered into strategic alliances with domestic, or more typically international, partners to pool their resources with other companies and share the risks associated with large R&D programs. An alternative source of R&D funding would be the federal government. The end of the Cold War provides an opportunity for the government to redirect its investment in defense technologies to programs more closely tied to commercial competitiveness. In this realm, federal laboratories may provide a key link in the R&D cycle.

Strategic Alliances

Many companies are financing R&D projects and production facilities in part through strategic alliances with domestic or international partners. While strategic alliances are not new to the semiconductor industry, their number has increased and their character has changed over the past decade. Throughout the 1970s and into the early 1980s, alliances between U.S. and Japanese companies were few and involved the licensing of

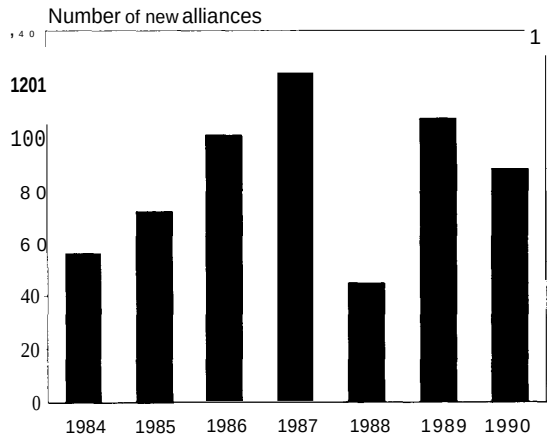
technology from small U.S. companies that lacked capital and manufacturing facilities to larger Japanese fins. By the late 1980s, the number of publicly announced strategic alliances announced each year had risen to about 100, about half of which, in 1990, were joint development agreements, joint fabrication agreements, or other types of joint ventures (figure 3-16).[52]

Strategic alliances are also becoming more prevalent among large U.S. semiconductor manufacturers such as IBM, Motorola, and Intel as development and production costs continue to rise, straining the financial resources of these companies. For example, IBM, Toshiba, and Siemens A.G. have teamed to develop technology for 256-M DRAMs, the cost of which no company could individually afford, given the low profit margins associated with memory devices. Similarly, Advanced Micro Devices Inc. and Fujitsu Ltd. agreed to establish a $700-million state-of-the-art joint fab for producing a new type of memory device called ''flash memories. '

These alliances allow companies to pursue technologies that might otherwise be too expensive to develop alone, and they provide ways of tapping into additional pools of funding. This is of interest not just to U.S. firms, but to Japanese companies as well. Overcapacity and a weak economy in Japan have pushed Japanese semiconductor manufacturers' capital spending levels down 29 percent in 1992; spending is expected to fall another 13 percent in 1993. Capital expenditures are likely to rise in North America by 13 percent in 1993, due in large part to a 25-percent increase by Intel Corp.

However, alliances raise concern about the possible transfer of U.S. technology abroad. Alliances are typically structured to team up U.S. technology and strengths in design and innovation with Japanese manufacturing capability. While the transfer of the product technology to Japan can be fairly easily accomplished, the transfer of manufacturing know-how back to the U.S. is more difficult. With manufacturing taking place in Japan, U.S. partners have difficulty learning from their Japanese partners. Therefore, such alliances may be more beneficial to Japanese companies than to U.S. companies. A recent report by the National Research Council warns that a continuation of strategic alliances of the kind found today in the semiconductor industry may prevent both the United States and Japan from developing the complementary capabilities they seek in their alliances.[53]

Figure 3-1 6-U.S.-Japan Semiconductor Alliances, 1984-1990



SOURCE: Bruce Kogut and Dong-Jae Kim, "Strategic Alliances in Semiconductor Firms," report to Dataquest, January 1991.

Greater Industry/Government Collaboration

An alternative to strategic alliances would be a greater government role in supporting semiconductor R&D and/or production. The government has many facilities capable of conducting research relevant to the semiconductor industry. With the end of the Cold War, resources that were

52 The number of actual alliances may be considerably larger than the number announced, perhaps by a factor of two or more. National Research Council, *U, S.-Japan Strategic Alliances in the Semiconductor Industry* (Washington, DC: National Academy Press, 1992), p. 32.

53 Ibid, pp. 2-3.

formerly devoted to defense missions maybe able to serve commercial purposes. The Department of Defense and the Department of Energy laboratories could serve as collaborators with industry on new technology development. NIST, which already has a mission to support industry, has developed a series of plans targeted to foster and support technological advances in the semiconductor industry.

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