Appendix C

The Decline of the U.S. DRAM Industry: Manufacturing

U.S. firms led the world in DRAM technology until the early 1980s. Japanese firms then gradually took control of the world market, in part because many U.S. producers could not match Japanese efforts at critical points in the technology's lifecycle. Heavy investment of money and manpower and close attention to highquality manufacturing were important factors in the Japanese success. In addition, Japanese efforts have been abetted by violations of trade law. As a result, Japanese firms now control 70 percent of the total world DRAM market and 85 percent of the advanced 1 Mbit DRAM market.

Two engineers designed Intel's (U. S.) pioneering 1K (1,000 bits or binary memory cells) DRAM in 1970-71 and just three engineers designed Intel's 16K DRAM. In contrast, one of today's major Japanese DRAM producers reportedly assigned 50 select engineers to design their IK DRAM and 100 to design their 16K DRAM. This allowed greater specialization, more careful attention to issues of manufacturability, and more rapid development of the designs.

Japanese firms invested heavily in plant and equipment in the mid-1970s. In contrast, U.S. producers cut investments due to the 1974-75 recession and were then unable to meet the demand when U.S. semiconductor markets boomed in 1979. Japanese producers stepped in—offering 16K DRAMs as licensed second sources for the industry-standard Mostek (U. S.) design—and, by the end of 1979, had captured 40 percent of the world 16K DRAM market.

Manufacturing quality began to appear as an issue in the late 1970s. Japanese 16K DRAMs, for example, had much lower failure rates than those of U.S. firms (table C-l)-even though nearly all began with the Mostek design. It took several years for U.S. firms to reduce failure rates to comparable or lower levels.

Table C-l—U.S.-Japan 16K DRAM Failure Rates (parts per million)

	1978	1979	1980	1981	1982
Japanese vendors	0.24	0.20	0.16	0.17	0.05
U.S. vendors	1.00	1.32	0.78	0.18	0.02

SOURCE: Hewlett Packard, William F. Finan, and Annette M. Lamond, "Sustaining U.S. Competitiveness in MicroElectronics: The Challenge to U.S. Policy," in *U.S. Competitiveness in the World Economy*, Bruce R. Scott and George C. Lodge (eds.) (Boston, MA: Harvard Business School Press, 19S5).

U.S. firms lost even more of the DRAM market in the next generation due, in part, to relatively less competitive manufacturing. Chiprnakers normally design chips as small as possible to reduce the likelihood that any one chip is contaminated by a stray microscopic dust particle and to increase the number of chips produced per wafer processed. Determined to leapfrog the Japanese in quality and cost, most U.S. producers designed much smaller and more sophisticated 64K chips than the Japanese, but were consequently slower than the Japanese in completing the designs and in solving related manufacturing problems.

In contrast, the Japanese successfully produced 64K DRAMs by slightly modifying and scaling up their 16K DRAM designs. The resulting chip was nearly 50 percent larger than the leading American designs, but they achieved good yields by using higher purity chemicals, by greater capital investment in cleanrooms and automation, and by superior quality-control techniques.

The simple design allowed the Japanese firms to get to the market first. High yields also lowered the overall cost per chip and gave them a greater production output per unit of capital investment and per labor hour than U.S. firms. By the end of 1981, the Japanese held 70 percent of the world 64K DRAM market. U.S. firms cut the Japanese share to 55 percent by mid-1983 after entering the market in volume, but most U.S. firms subsequently abandoned the market due to Japanese dumping in the mid-1980s and/or due to problems they encountered in manufacturing subsequent generations of DRAMs competitively.

Issues of manufacturing process arose again as firms made the transition from the 256K to the 1M (1,000,000 bits) DRAM. Table C-2 compares the production yields and costs for a lower-yield U.S. manufacturer-a major U.S. firm that subsequently dropped out of the DRAM business-with that of Toshiba, the world leader in 1M DRAM production.

The U.S. firm's design and manufacturing process had several serious shortcomings that allowed no marg. for error. For example, in etching the silicon wafer to create the circuit elements, the U.S. firm's process formed sharp vertical walls. In previous generations of DRAMs this would not have been a problem. But with the dimensions of the 1M DRAM circuitry shrinking to just 1/100 the diameter of a human hair, sharp vertical walls prevented

[1]Sources for this section include: Peter D. Nunan, Sematech, personal communications, May 11, June 22, Aug. 4, and Oct. 10, 1989; Brian Sante, "lK-Bit DRAM, 1970, " *IEEE Spectrum, vol. 25, No.* 11, 1988; William F. Finan, Jeffrey Frey, "Study of the Management of MicroElectronics-Related Research and Development in Japan," contractor report pared forthe Office of Technology Assessment, November 1988; *Competitive Edge: The Semiconductor Industry in the U.S. and Japan*, Daniel I. Okimoto, Takuo Sugano, and Franklin B. Weinstein (eds.) (Stanford, CA: Stanford University Press, 1984); William F. Finan and Annette M. LaMond, "Sustaining U.S. Competitiveness in Microelectronics: The Challenge to U.S. Policy", in *U.S. Competitiveness in the World Economy*, Bruce R. Scott and George C. Lodge (eds.) (Boston, MA: Harvard Business Press, 1985).

Table C-2—U.S.-Japan 1 M DRAM Manufacturing Cost Comparison

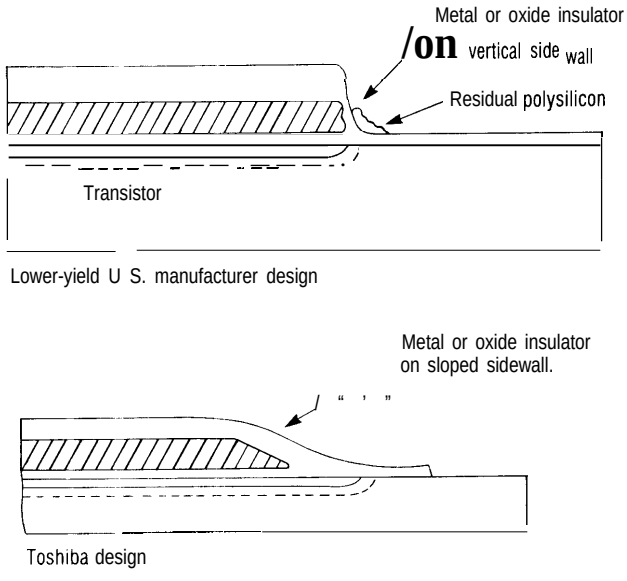
Operation	Lower yield U.S. manufacturer 3Q 1986	Toshiba 3Q 1986
Start wafer cost[a]	(Epi) $60.00	(Bulk) $25.00
Prooessed wafer cost	$335.00	$300.00
Chip size (square mm)	73	54
Total chips possible (assuming a 125 mm wafer)	151	205
Wafer probe yield	25%	68%
Number of good chips	38	139
Packaging cost	$0.25	$0.25
Assembly yield	92%	92%
Final test cost	$0.20	$0.20
Final test yield	85%	85%
Total manufacturing oost	$11.83	$3.31

NOTE: These are representative values to indicate relative manufacturing costs for these two firms at a particular time. These firms are at different points on the learning curve for IM DRAMs in 1986, but process design flaws probably would have prevented much higher yields for the U.S. firm.

[a]The starting wafers, Epi and Bulk, refer to different types of wafers.

SOURCE: Peter D. Nunan, Sematech, personal communications, May 11, June 23, Aug. 4, and Oct. 10, 1989.

Figure C-l-Cross-section of 1M DRAM Storage Cell



A. Cross-section of lower yield U.S. manufacturer's design showing the sharp mrners from which it was dificult to etch residual polysilicon.

B. Cross-section of Toshiba design showing the sloped sidewall.

SOURCE: Peter D. Nunan, Sematech, personal communication, Oct. 10. 1989.

subsequently deposited material from being effectively etched out of the comers, causing the circuitry to short-out (figure C-l).

The Toshiba engineers recognized this pitfall and developed a new technique which formed sloped rather than sharp vertical walls (figure C-l). The resulting process was highly robust. When transferred to Siemens in Germany and to Motorola in the United States, yields were high even with the very first wafers processed and even with relatively less experienced line workers.

Technical management and quality philosophy proved to be key problems for the U.S. firm. Its design engineers developed their DRAM process and prototypes in the laboratory, and then 'threw the design over the fence' to the manufacturing engineers. The design engineers recognized the difficulties of producing 1M DRAMs with their design: they attempted to compensate by specifying a high-quality starting wafer, by keeping the chip size relatively large, and by including a very large number of redundant memory cells on the chip as backup (table C-2). They were relying on inspection and correction after production to provide usable DRAMs rather than designing quality in.

The manufacturing engineers were unable to get (wafer probe) yields up to competitive levels under factory conditions. They protested that the process had no margin for error and was not readily manufacturable, but didn't have the resources or knowledge to do proper analysis and implement improvements. The designers insisted that they had developed a robust and manufacturable process and stayed away from correcting the problem. In contrast, the engineers and scientists who developed the Toshiba process were also responsible for improving the yield on the factory floor. Even if the Japanese had not been dumping DRAMs in the United States in the mid-1980s, the 1M DRAM design and manufacturing process of this low-yield U.S. manufacturer might never have been competitive.

The loss of the DRAM market may be particularly darnaging to the U.S. chip industry. DRAMs are known as a technology driver because they push the limits in certain kinds of process technologies. Loss of DRAM production will likely cause U.S. firms to lag the Japanese in developing certain kinds of manufacturing processes important in the production of many types of chips.

U.S. firms face formidable obstacles should they choose to reenter the DRAM market. From $5 to $10 million in the mid- to late-1970s, the cost of a single minimum-efficient scale, state-of-the-art DRAM production facility has risen to roughly $200 million today, and is expected to approach $400 million for the next-generation 16M DRAMs. The human skills to design and produce leading-edge DRAMs also take many years to develop.

Siemens has committed $1.6 billion to develop or acquire 1M and 4M DRAM technology and production facilities. Even armed with IBM's DRAM designs, however, U.S. Memories failed to raise $1 billion to enter

DRAM production. Similar investments needed for producing state-of-the-art semiconductors generally are all but impossible for small- and medium-sized firms. As a result, many American companies are forced to rely on Japanese and other foreign firms to produce their chip designs.

Some observers see the relatively low level of funding for Sematech—roughly $200 million per year-and the corresponding decision to not pursue large-volume production of DRAMs as critical constraints. They argue that a high-volume operation is essential for testing yield and reliability, and that issues of technical management and quality techniques-such as for the lower yield U.S. manufacturer described above-can otherwise be swept under the rug. As one Sematech engineer, frustrated by what he feels is an inadequate response to the Japanese challenge, put it,

> It's as if the Soviets, having already taken the lead in the space race, had announced in 1961 that they were going to send a man to the moon, and the U.S. response was to focus on selected aspects of rocket science.