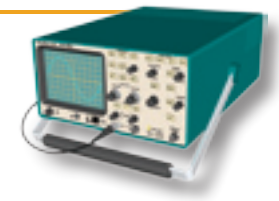
N0AX

HANDS-ON RADIO



Experiment #68 — Phase Locked Loops, the Basics

Phase locked loops are found in many types of radio equipment. They can be used as modulators, demodulators, oscillators, synthesizers, clock signal recovery circuits and the list goes on. Are they mysterious and difficult to understand? Not really, once you get to know each piece and do a little experimentation.

Background

The phase locked loop (PLL) has its roots in receiver design. It was invented in 1932 as a technique for stabilizing an oscillator's frequency.[1] The PLL was then adapted for use in television receivers, synchronizing the vertical and horizontal sweep circuits to the incoming video signal. In the 1960s and '70s, integrated circuit PLL chips became available and the technique soon became even more widespread.

Let's start with the name itself. *Phase* refers to the relative phase difference between an input signal and the loop's internal oscillator. *Locked* means that the oscillator's phase maintains a constant relationship of that of the input signal. This also means the frequencies of the two signals are the same, otherwise the phase difference would change. *Loop* comes from the feedback loop that controls the internal oscillator's frequency to remain in sync with that of the input signal. Thus, a *phase locked loop*.

Feedback is key to the PLL's function. Think back to the description of how an op-amp amplifier circuit works in Hands-On Radio Experiment #3.[2] Amplifying the difference in voltage between its input terminals, the op-amp output voltage changes and the external circuitry is configured to make that change reduce the difference, bringing the circuit back into balance. That kind of feedback loop uses a signal's amplitude (voltage and current) instead of frequency and phase as does the PLL.

Loop Components

The PLL has three basic components, seen in Figure 1 — the phase detector, the loop filter and a voltage-controlled oscillator (VCO). The output from the phase detector (C in Figure 1) is a signal that contains the frequency and phase difference between the input signal and VCO output. The loop filter creates the VCO control voltage based on the difference signal. The VCO changes frequency in response to the control voltage until the two frequencies are the same. Simple, no? Maybe we should slow down a little bit and look at each piece.

The VCO is a special type of oscillator that has a frequency controlled by an applied voltage. The frequency of the VCO without any control signal applied is called the *free-running* frequency, f_0. Depending on the circuit design, the VCO may be designed so that f_0 occurs with zero dc voltage input and a bipolar control signal, or at some non-zero dc voltage so the circuit can operate from a single power supply voltage.

Next, you may be wondering why I used a mixer symbol for the phase detector. It's because the phase detector is just that — a type of mixer. Experiment #66 provided the equations describing a mixer's output products, but ignored differences in phase between the input signals. Taking phase into account, the mixing product at the difference of the two input signal frequencies, f_A and f_B, is $\cos(2\pi[f_A - f_B]t + \theta)$, with θ representing the difference in phase between the signals. If the two signals have the same frequency and the phase difference is constant, then $f_A - f_B = 0$, leaving $\cos(\theta)$, a dc voltage that makes a fine VCO control signal.

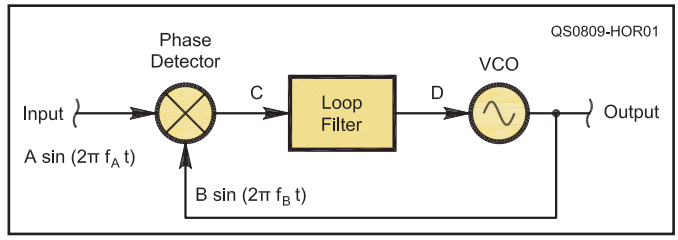


Figure 1 — The basic structure of a phase locked loop. The phase detector acts as a mixer, generating products at the sum and difference frequencies of its inputs. The filter extracts the dc component of the mixer output for the VCO to use as a control voltage.

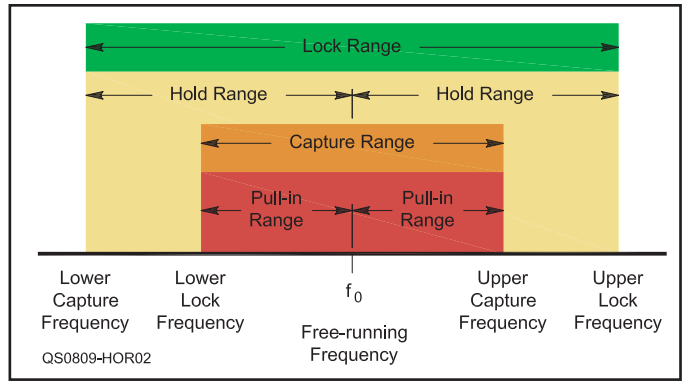


Figure 2 — The four frequency ranges that define a PLL's behavior. Lock range (and hold range) shows how far the PLL frequency can track an input signal. Capture range (and pull-in range) shows how far from the free running frequency the VCO will move to lock onto an input signal.

The high frequency of the sum product at $f_A + f_B$ is not suitable as a VCO control voltage and so must be removed. That is the job of the low-pass loop filter — to remove everything but the phase detector's $f_A - f_B$ product, along with the phase information. Depending on the design of the phase detector and the nature of the signals (sine, square, pulse), the loop filter may also need to convert short bursts of current into a smoothly varying voltage.

PLL Operation

After the PLL is turned on with no input signal, the VCO will oscillate at the free-

[1] **www.uoguelph.ca/~antoon/gadgets/pll/pll.html**.

[2] Hands-On Radio experiments are available online to ARRL members at **www.arrl.org/tis/info/HTML/Hands-On-Radio**. The first 61 experiments are also available as *ARRL Hands-On Radio Experiments* from the ARRL at **www.arrl.org/shop**.

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running frequency, f_0, until an input signal is applied. The phase detector generates sum and difference products, the loop filter removes the sum product, and the VCO output frequency begins to change. Assuming the input and VCO frequencies are not the same, the output of the loop filter (D in Figure 1) will be an increasing or decreasing voltage depending on which signal has the higher frequency.

This changing voltage causes the VCO to respond very quickly, reducing the difference between the VCO and input frequencies. Consequently, the loop filter's output voltage is also reduced, making smaller and smaller changes in the VCO frequency. Within a short time (typically a few milliseconds for RF PLLs) the VCO frequency is equal to that of the input signal and the loop is "locked." Any change in either the PLL input or VCO frequencies is tracked by a change in the loop filter output, keeping the two frequencies the same.

This process of adjust and hold is called *capture*. The minimum and maximum input frequencies to which the loop can move the VCO as it captures an input signal is called the *capture range* as shown in Figure 2. The segments of the capture range above and below f_0 are called the *pull-in range*. The pull-in ranges are not necessarily symmetrical.

If the control signal is proportional to the cosine of the phase difference, it will be zero when the phase difference is 90° (cos 90° = 0). It will be a maximum when the two signals are in phase (cos 0° = 1) or out of phase (cos 180° = –1). This defines the range over which the PLL can keep the input and VCO frequencies locked together. As the input frequency moves farther and farther from f_0, the VCO's free-running frequency, the loop's control action will keep the VCO frequency the same as the input frequency, but with a phase difference that gets closer to 0 or 180°, depending on which direction the input frequency changes.

If the input frequency has moved so far that the phase difference between it and the VCO frequency is either 0 or 180°, any further change will cause the control signal to move back toward its 90° value and the VCO frequency away from the input signal. The loop is no longer locked and the input and VCO frequencies are no longer the same. The range of input frequencies between the value at which the loop is locked with a phase difference of 0° and 180° is called the loop's *lock* range. The lock range above and below f_0 are called the loop's *hold ranges*. The lock range is not always centered on f_0.

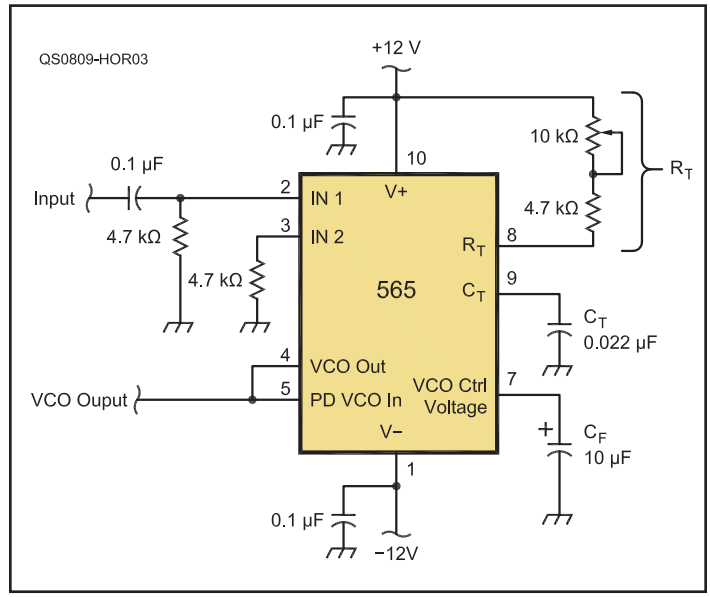

Figure 3 — The 565 integrated circuit PLL contains almost all of the circuitry necessary to build a PLL. Only a few discrete components are needed to set the VCO free-running frequency and loop filter time constant.

Building A PLL

The venerable 565 PLL IC, a fixture in electronics for nearly 40 years, is still widely used. Start by downloading the LM565 datasheet from **cache.national.com/ds/LM/LM565.pdf**. Familiarize yourself with the pin connections and browse some of the circuit examples.

Build the circuit shown in Figure 3. You'll need a bipolar power supply to do this experiment. Set the potentiometer to half-range, about 5 kΩ. Without connecting any input signal, apply power and use an oscilloscope or frequency counter to measure the free-running frequency at VCO out. It should be close to $f_0 = 1.2/4R_TC_T \approx 1360$ Hz.

Set your function generator to output a sine wave at the measured value of f_0. 0.5 to 1 V_{P-P} will be sufficient. Apply the sine wave to the PLL's input. Use a dual-channel oscilloscope to monitor both the function generator output and the VCO output. Use the function generator output to trigger the 'scope. The sine waves on both channels should be stable (because they are locked in frequency) but will be somewhat out of phase.

Slowly reduce the generator output frequency until the PLL loses lock — seen as one trace suddenly becoming unstable. That frequency is the lower limit of the PLL's lock range. Return the generator frequency to f_0 and then increase it until the PLL loses lock again at the upper limit of the lock range. Total lock range is the difference between these two frequencies.

Slowly reduce the generator frequency until the PLL suddenly captures the input signal and locks again — both traces will be stable. This frequency, the upper limit of the PLL capture range, will be somewhat lower than the upper lock range limit. Change the generator frequency to something below the lower limit of lock range you measured previously. Slowly increase frequency until the PLL captures the input signal at the lower limit of capture range. Total capture range is the difference between these two frequencies.

Capture range depends on the time constant of the loop filter, determined by C_F and a 3.6 kΩ resistor connected inside the IC. The time constant of the filter equals R × C = 3.6 kΩ × 10 µF = 36 ms. The larger the time constant, the smaller the capture range because the loop doesn't respond quickly enough. Replace C_F with smaller capacitors, down to 1 nF and see what happens to capture range as the loop reacts more quickly. Leave the circuit assembled for next month's follow-up experiments!

Parts List

- Capacitor — 0.1 µF ceramic, quantity 3.
- Capacitor — 0.022 µF ceramic or film.
- Capacitor — 10 µF, 25 V electrolytic.
- Phase locked loop IC — NE565.
- Potentiometer — 10 kΩ.
- Resistor — 4.7 kΩ, ¼ W, quantity 3.

Parts hint — the end of fishing season is a great time to find bargains on tackle boxes. They make terrific parts and tool organizers!

Recommended Reading

Many electronic experimenters have gotten their start in understanding PLLs by reading the classic tutorial Motorola application note AN535 "Phase Locked Loop Design Fundamentals." It's available at **www.datasheetcatalog.org/datasheet/motorola/AN535.pdf** and would make a good addition to your technical library.

Next Month

This month you manipulated the PLL by hand. Next month, we go live as we use a PLL to demodulate an FM signal. QST