# Constructing Virtual Architectures on Tiled Processors

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# Emulators and JITs for Multi-Core

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  - Growth applications are parallel
- Future architectures will be optimized for parallel applications
  - Hardware compatibility will be broken
- Future architectures will need to run legacy applications
  - Market forces will require future chips to run 1983 "Frogger" for DOS
  - Software re-verification on new architectures too costly

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Parameters for Multi-Core are different

- Core-to-Core latencies reduced

# Road Map

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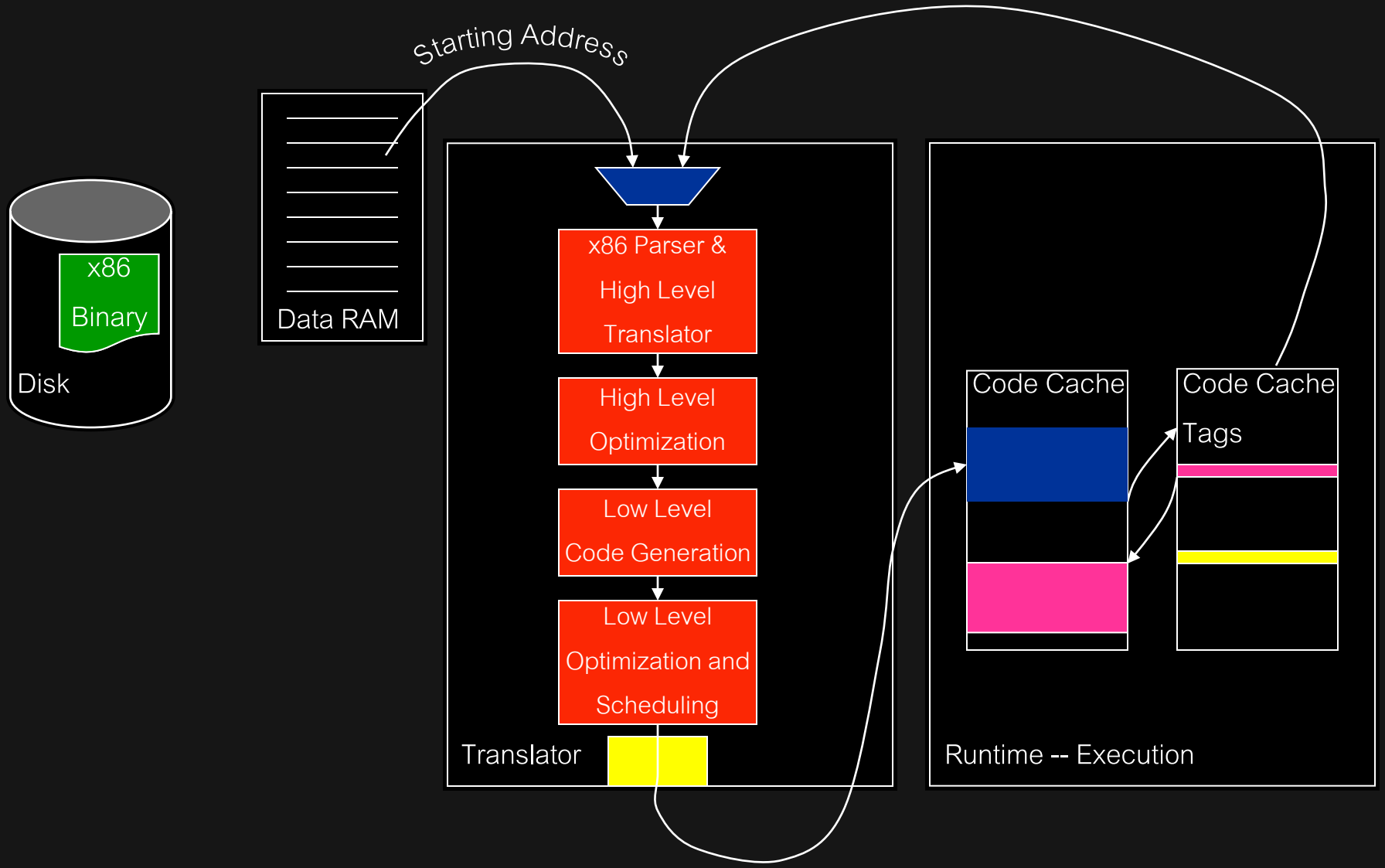
3. Static & Dynamic Architecture Reconfiguration

Proof of concept system

All software parallel translator: x86 on Raw

# Background: Translation



# Background: “Old” Parallel Translation

# 1. Pipelining Virtual Architectures

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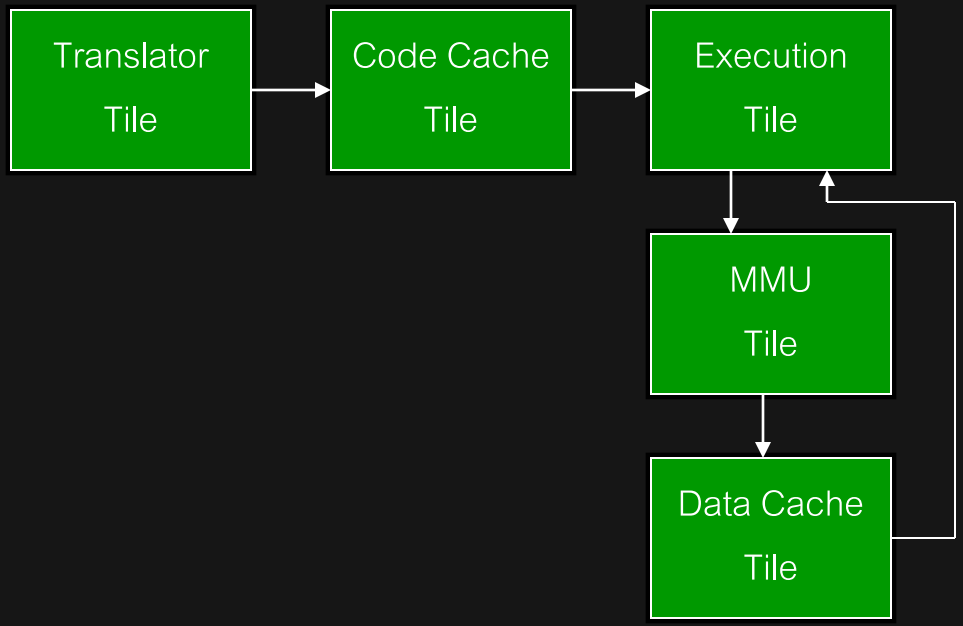

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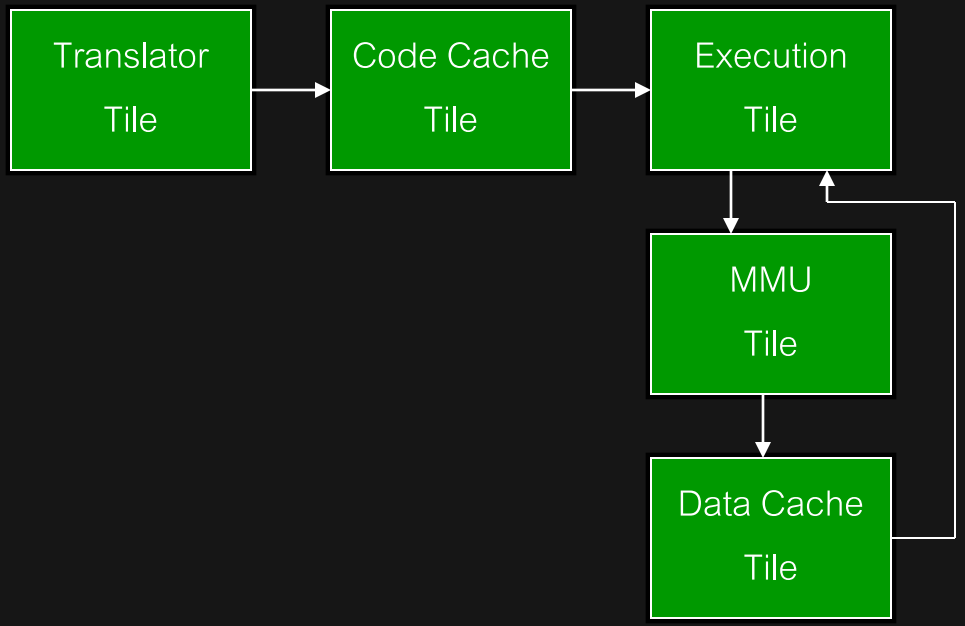


Utilize a Tiled Processor as fabric to construct virtual processor

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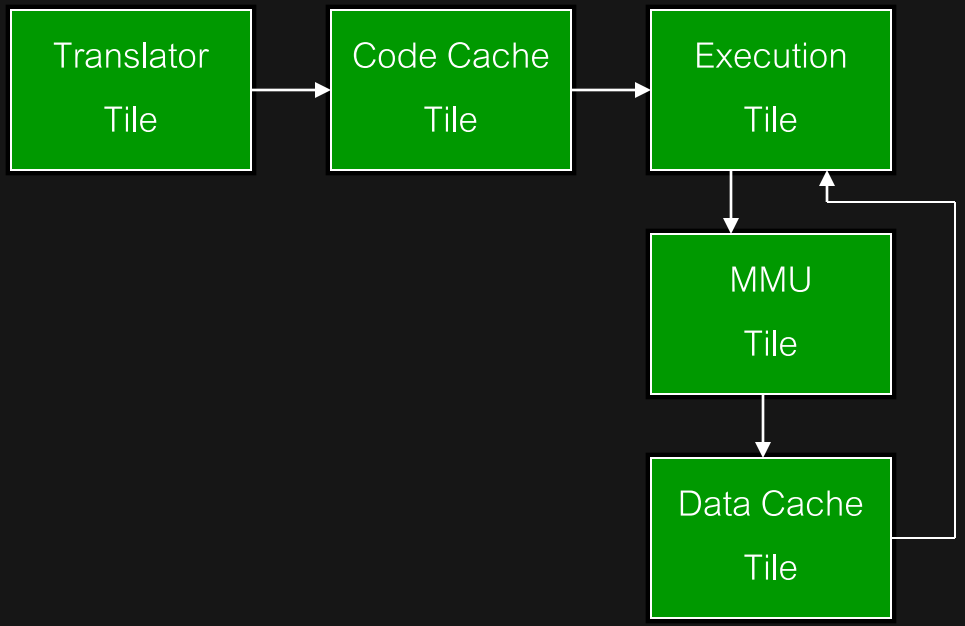
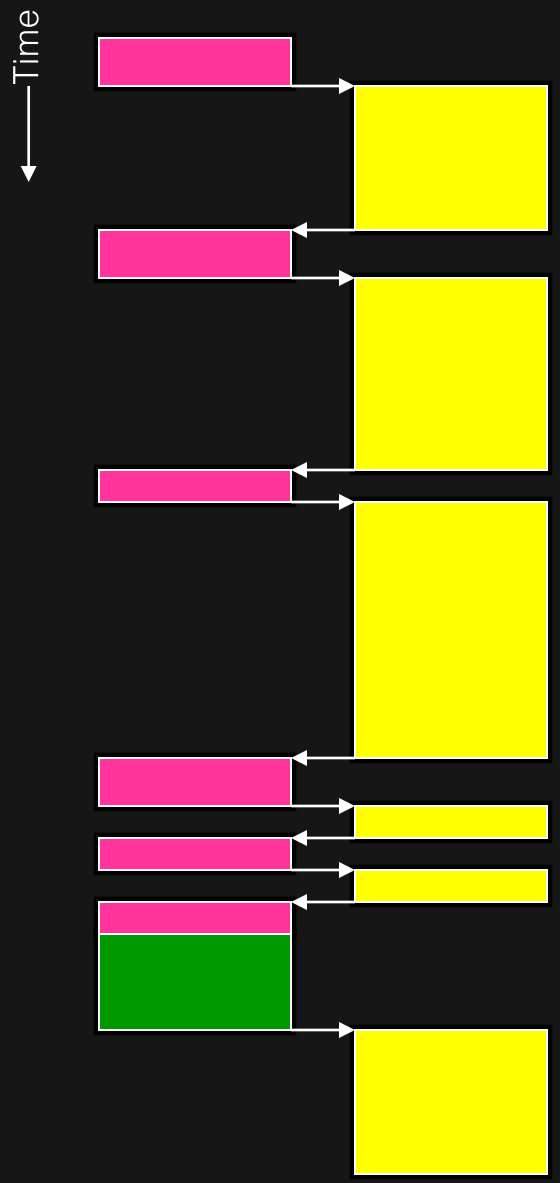
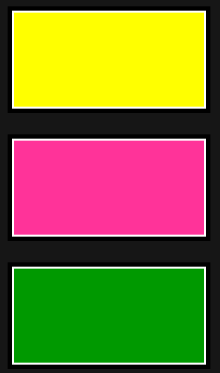



Utilize a Tiled Processor as fabric to construct virtual processor

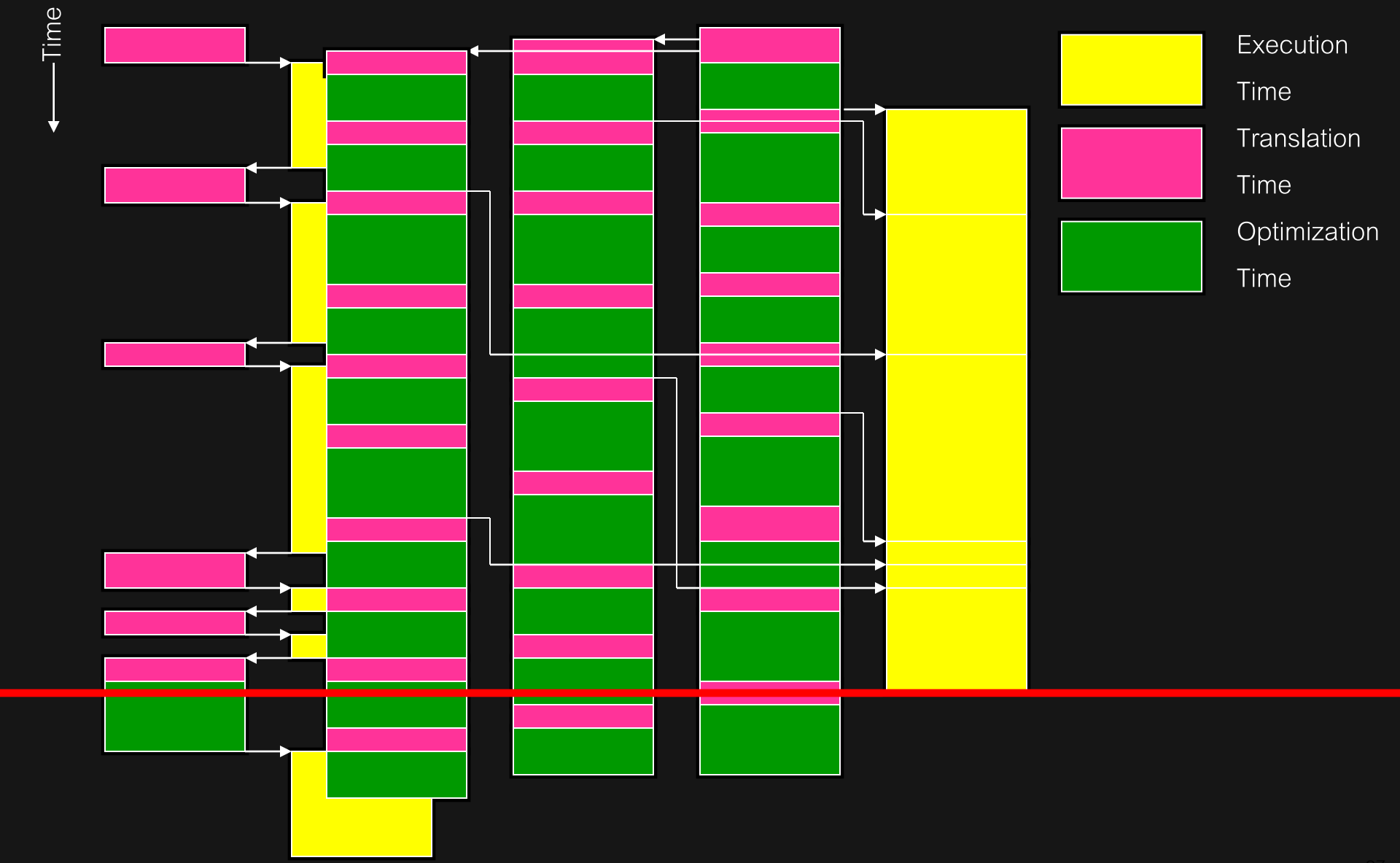
Coarse grain pipelining to exploit parallelism

# Sequential Translation



# 2. Speculative Parallel Translation



# 3. Reconfiguration

Different programs have different characteristics

Processor Architect uses benchmarks to choose “compromise” processor

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Static Reconfiguration

- Choose different virtual machine configuration based off application

Dynamic Reconfiguration

- Detect phases/programs dynamic needs and reconfigure at runtime
  - Cost to reconfiguration

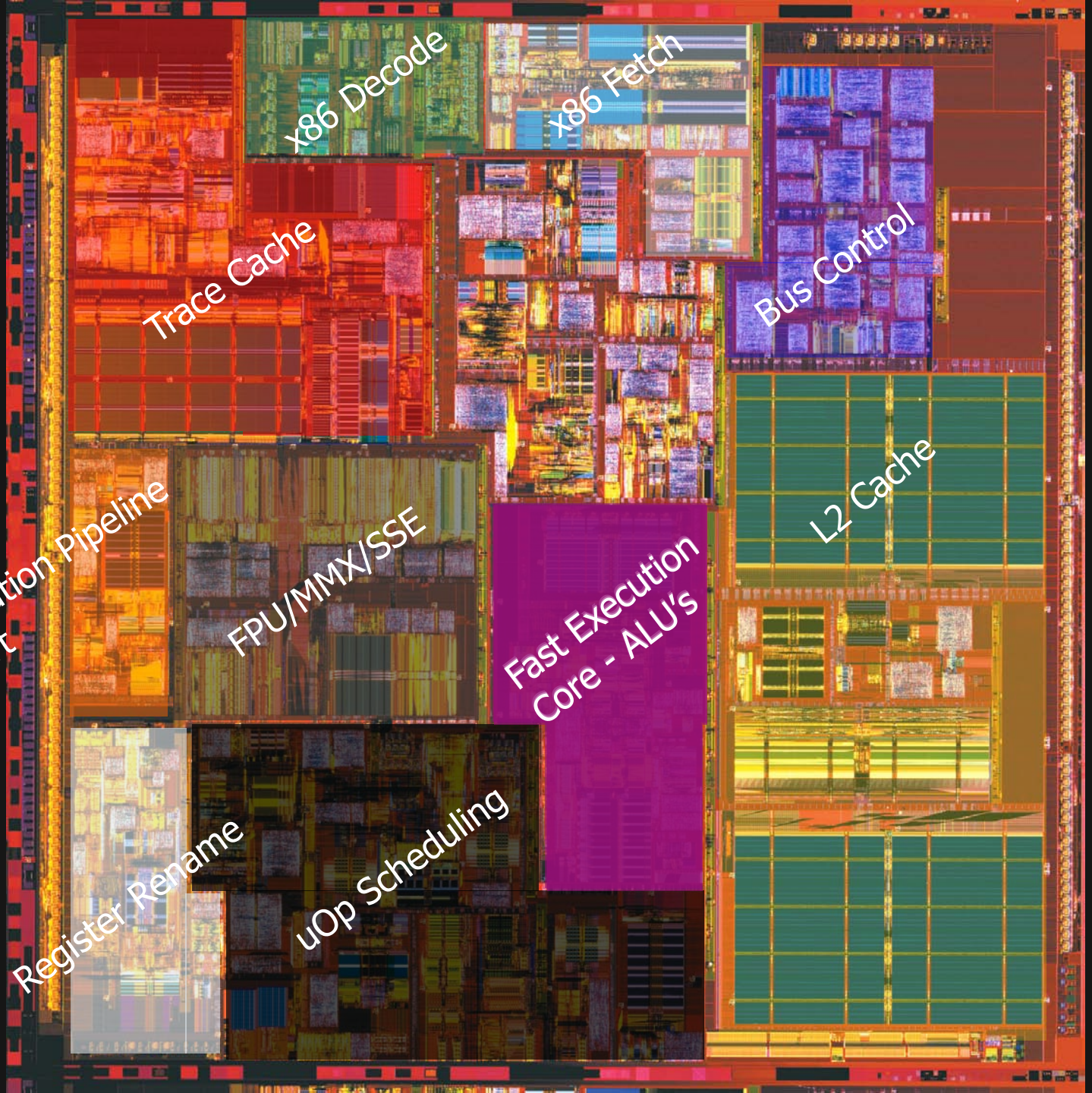
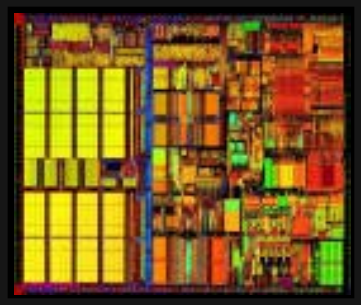



Photo Courtesy Intel Corp.

# Prototype System and Evaluation

# Background: Architectures



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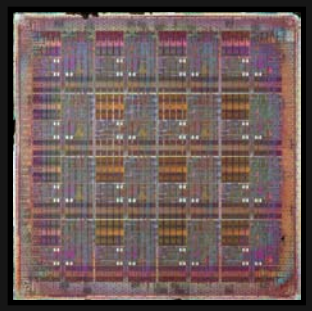
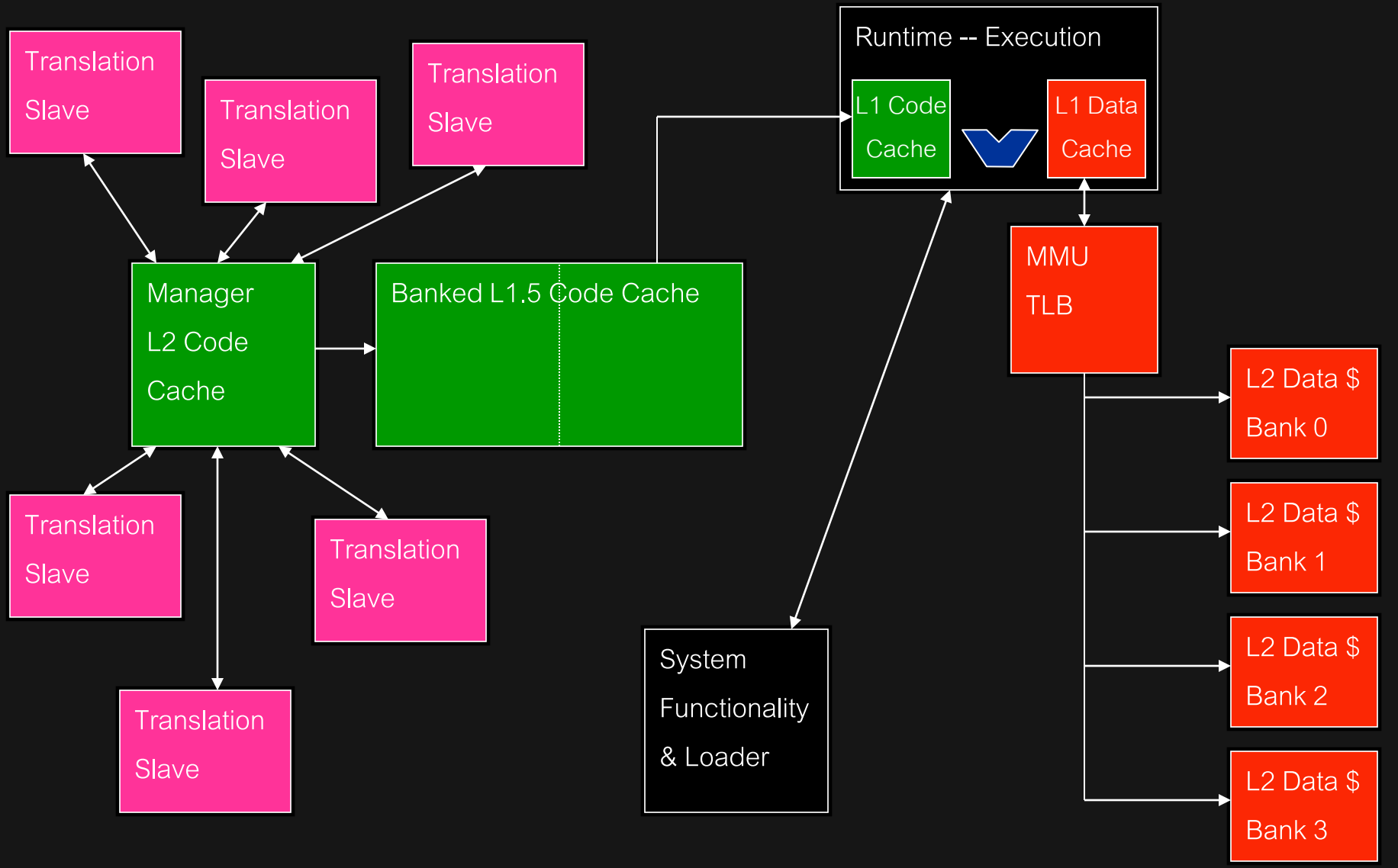


| | x86 (Pentium III) | Raw |
|---|---|---|
| ISA | CISC instruction set | RISC instruction set |
| | Hardware Virtual Memory (VM) | No VM |
| | Hardware Memory Protection | No Memory Protection |
| | Condition Codes used for branching | No Condition Codes |
| | Hardware instruction cache | Software managed instruction memory |
| Implementation | 1 superscalar processor core | 16 Processors arranged in 4x4 mesh |
| | 3-way parallelism | 4 low latency networks |
| | Out-of-order processor | In-order processors |

* Photo Courtesy Intel Corp.

# System Design



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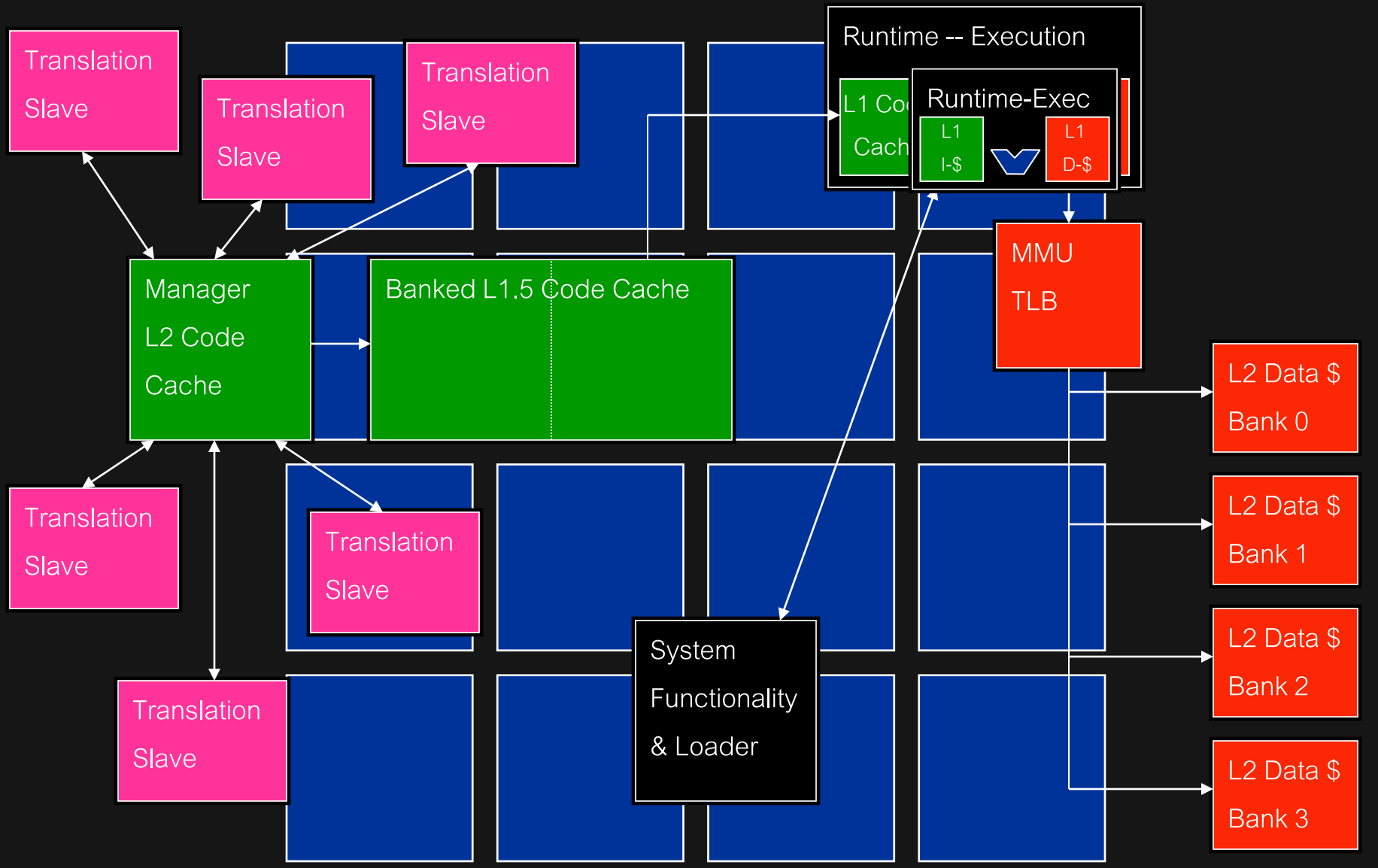


# Methodology

Cycle comparison of Raw vs. Pentium III

All results collected on real hardware

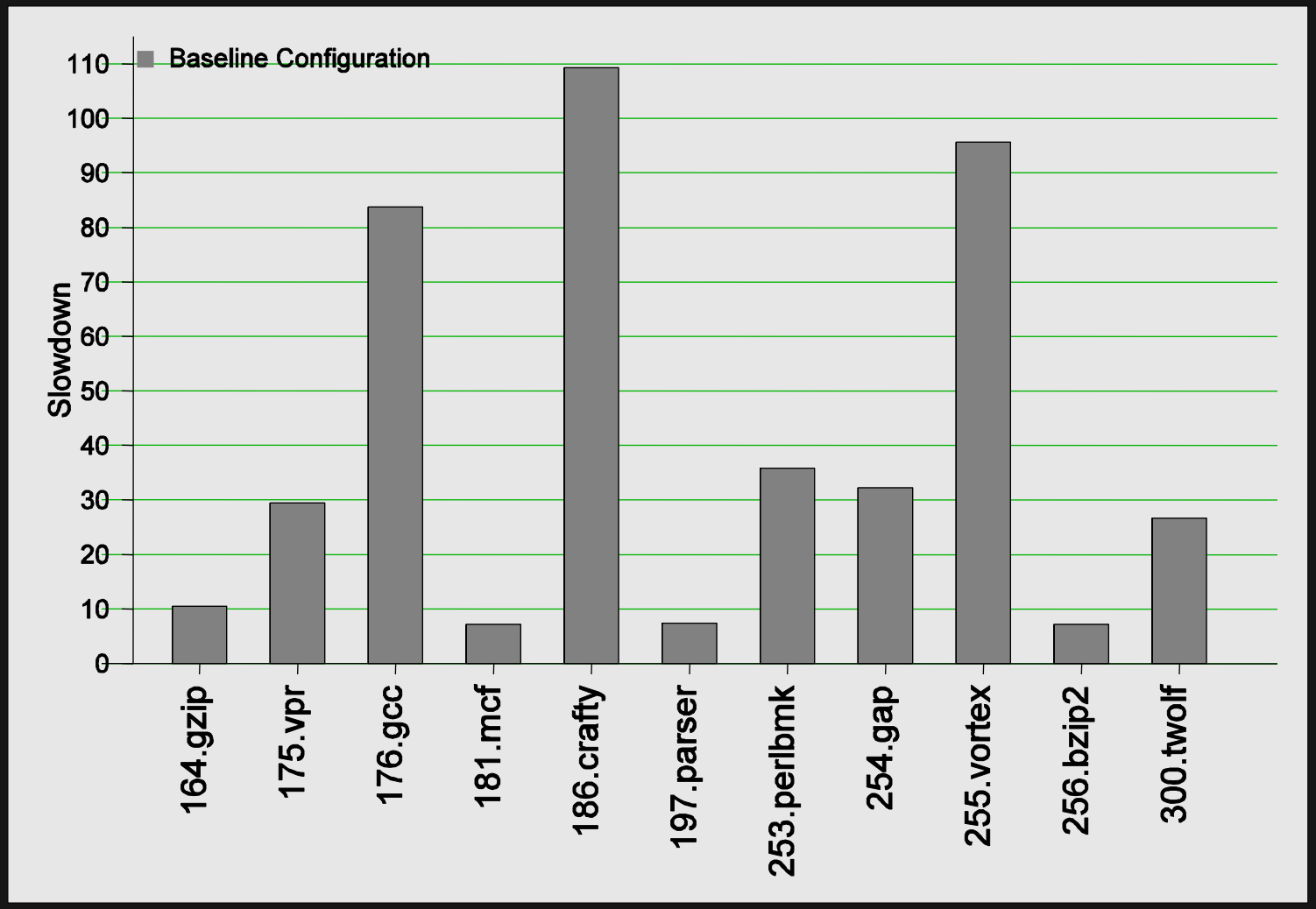
- No hardware added

Same binaries (unmodified)

Metric: Slowdown

- Raw executing x86 code compared by cycle against Pentium III

# Baseline Performance



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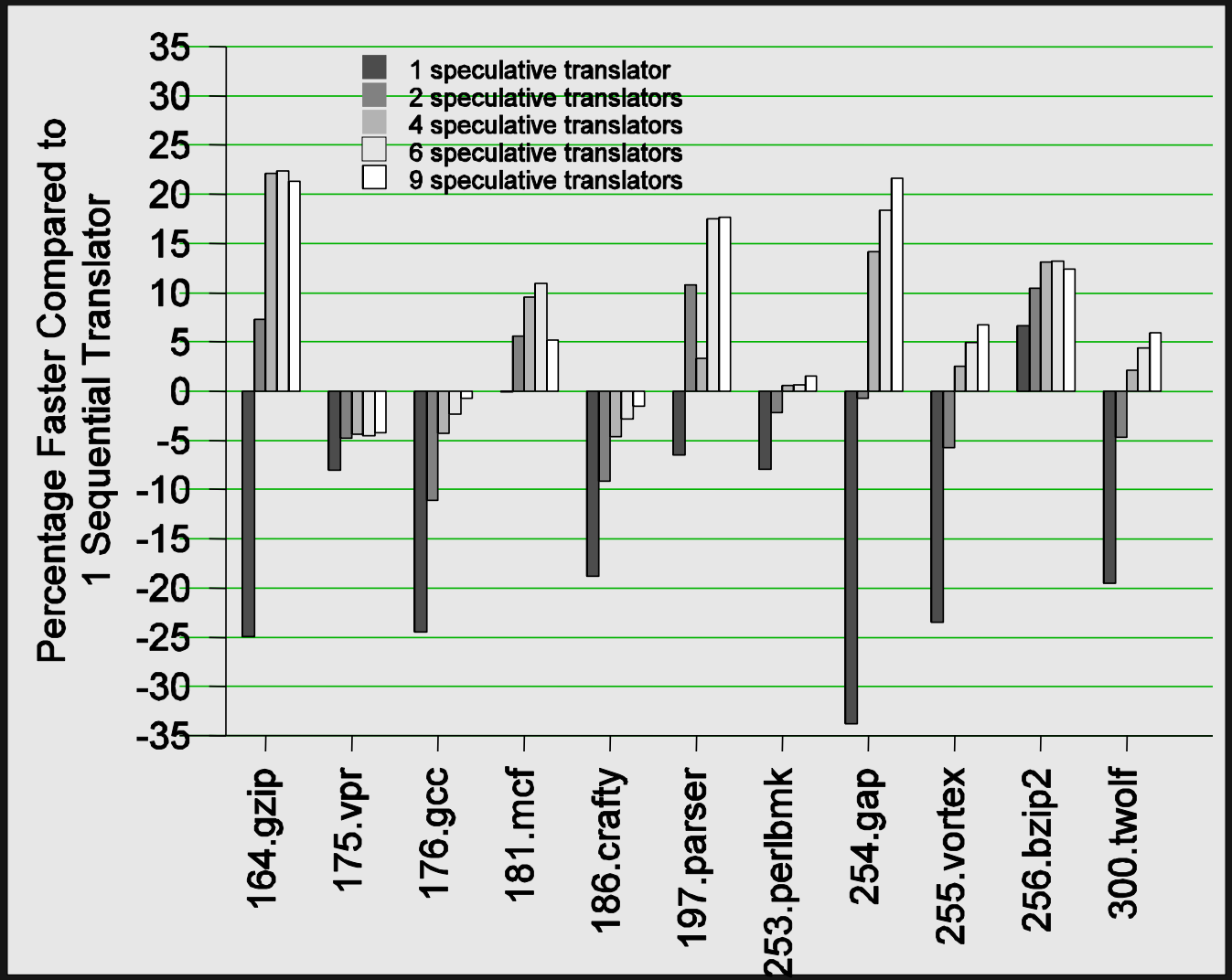

# L2 Code Cache Miss Rate

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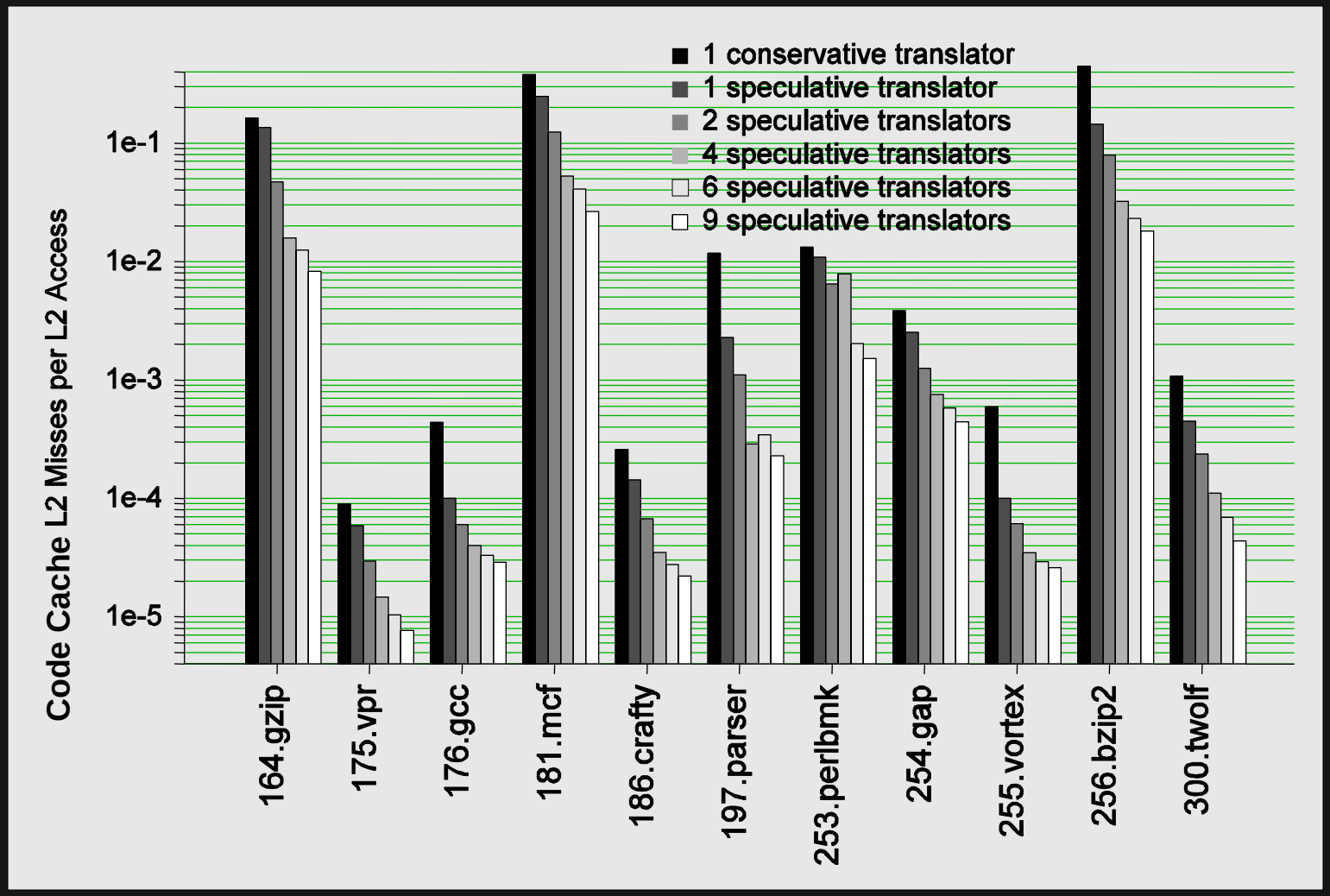
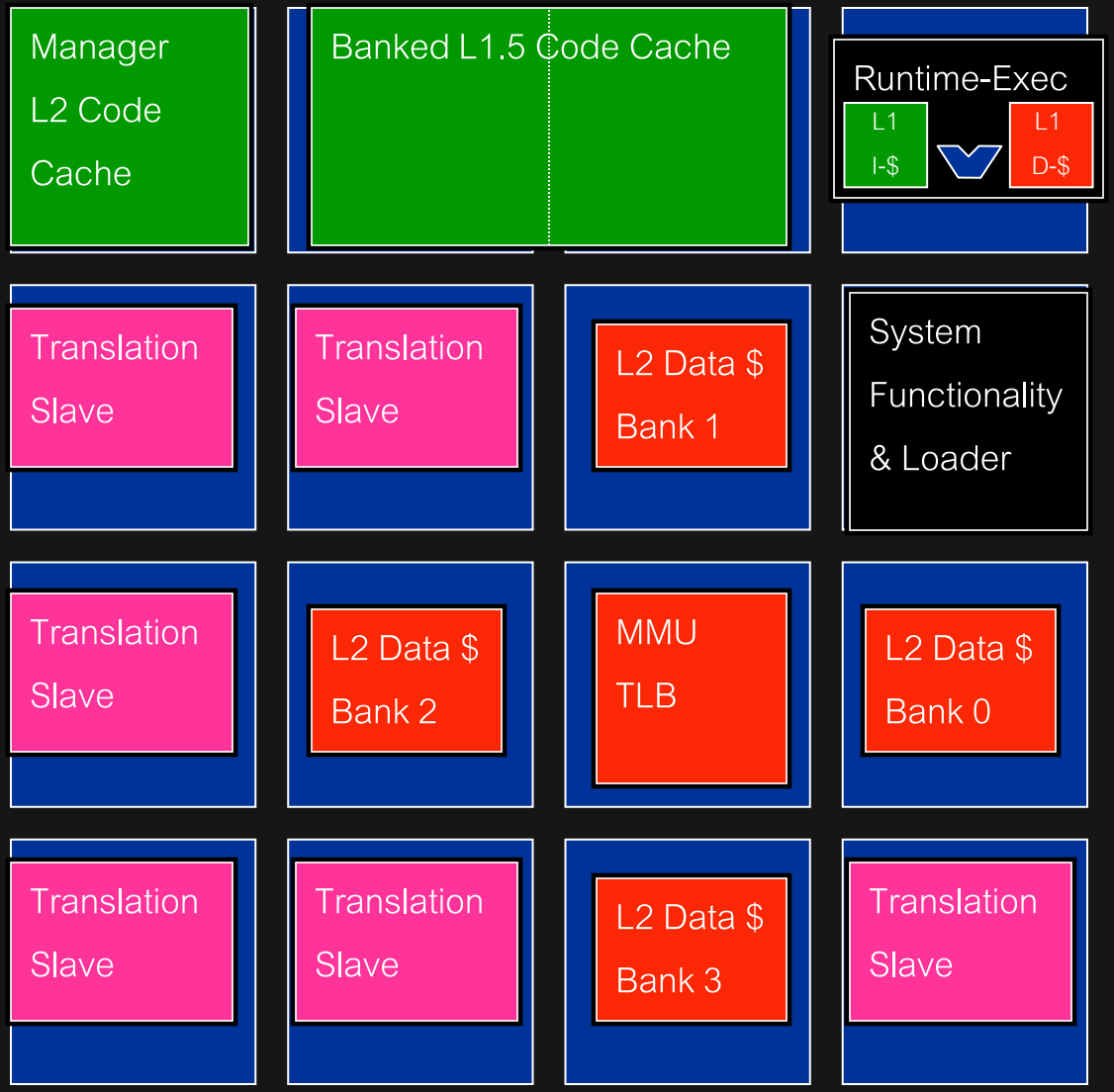


# 3. Static Reconfiguration



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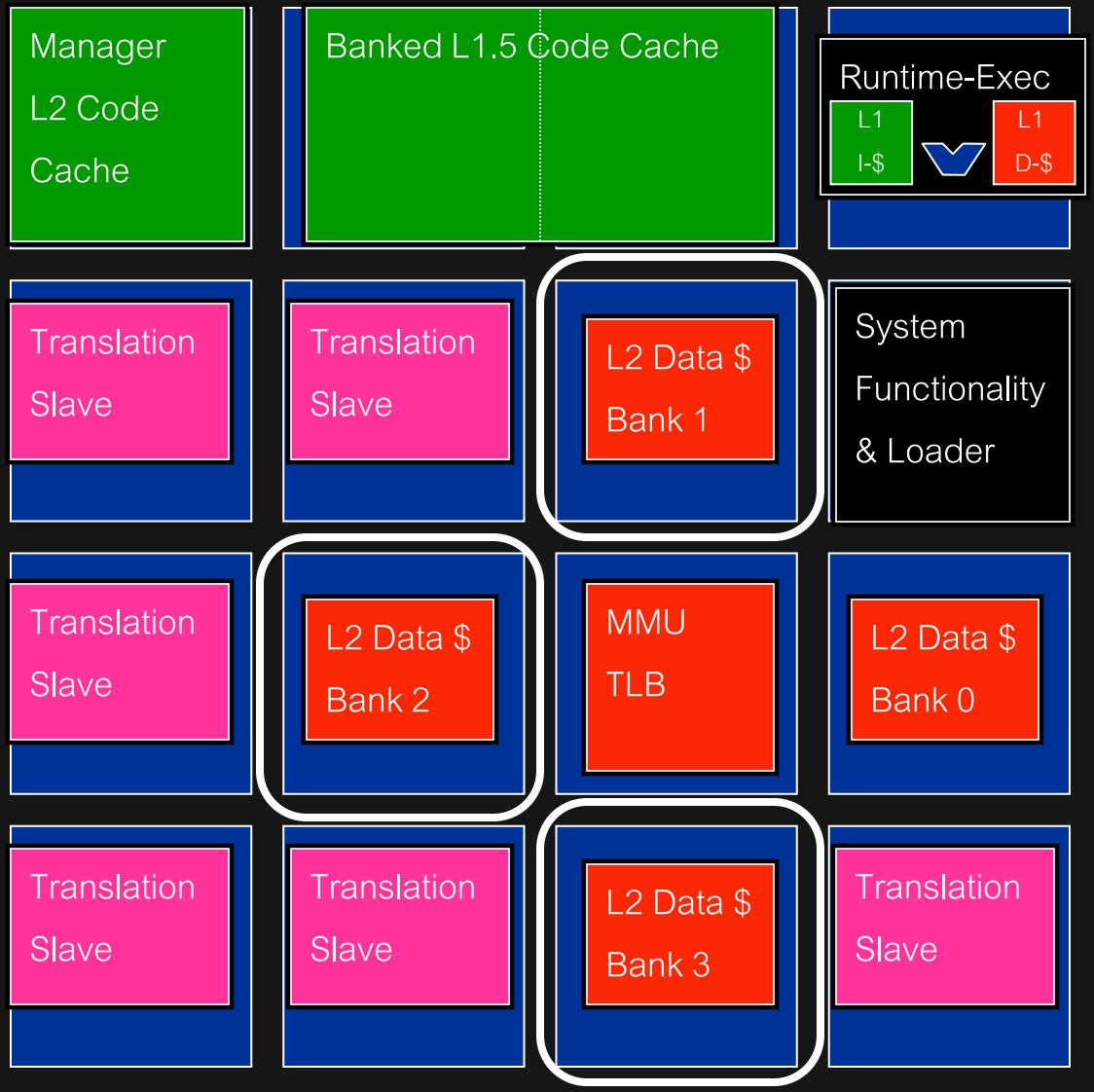

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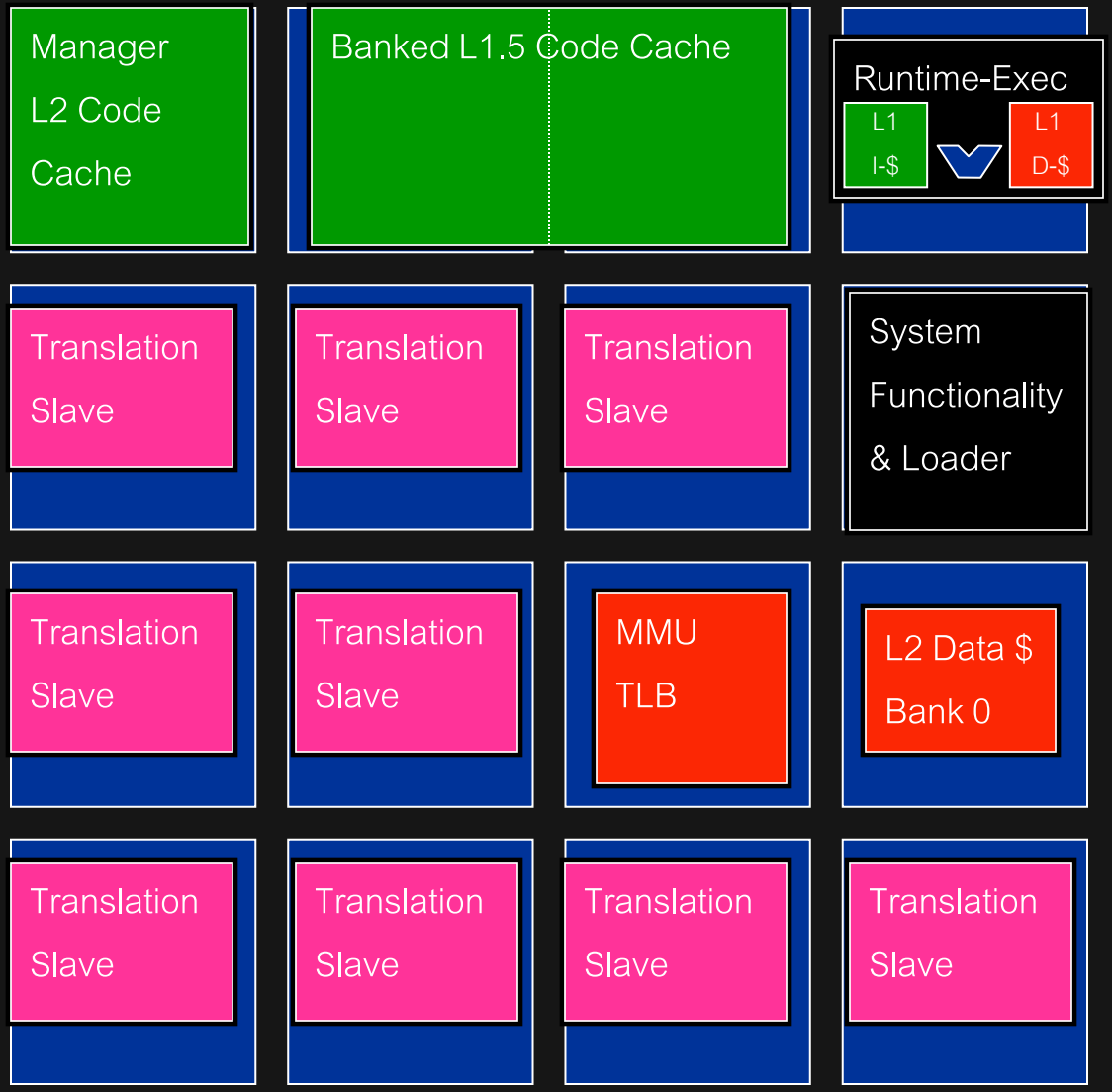

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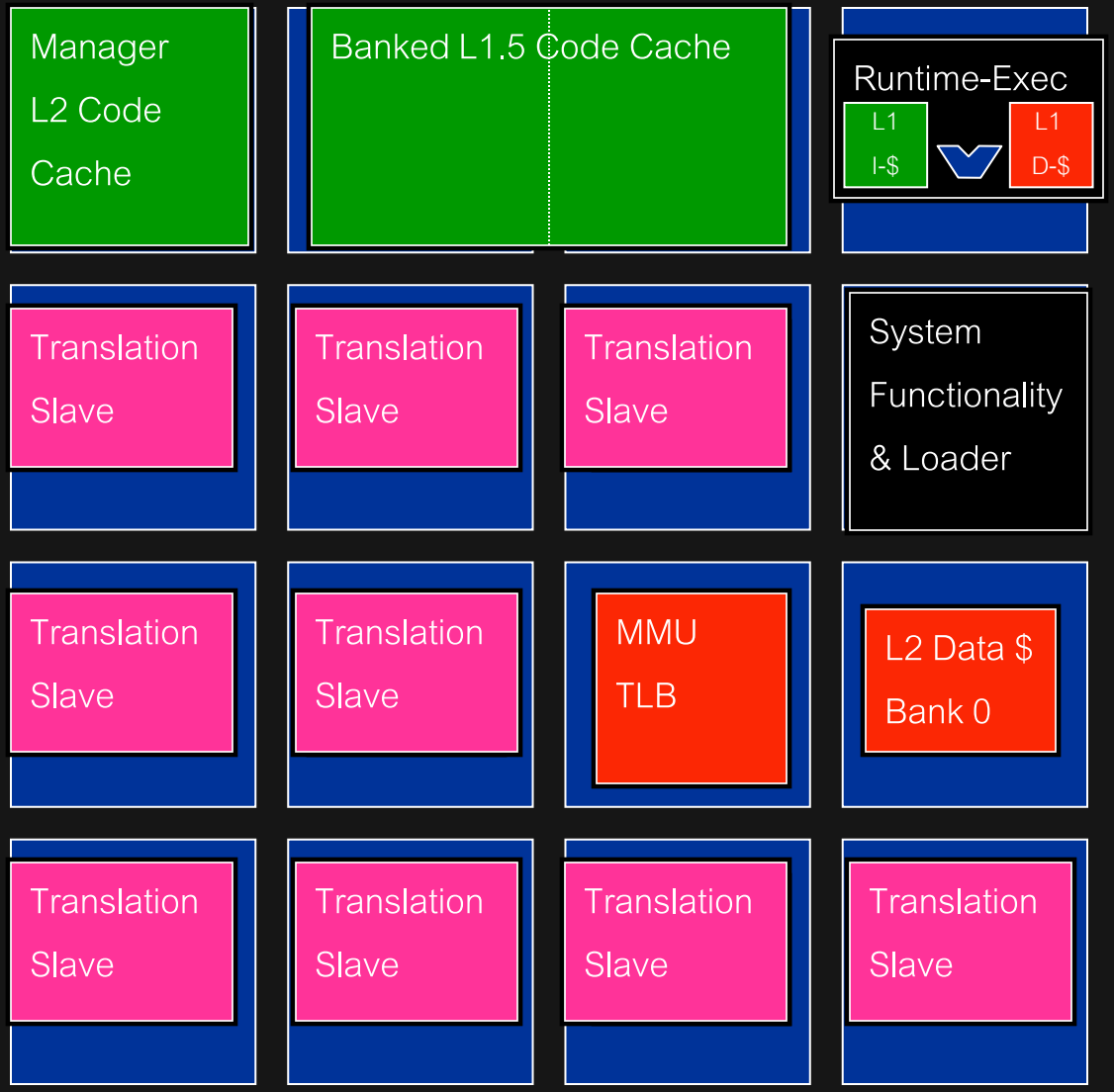

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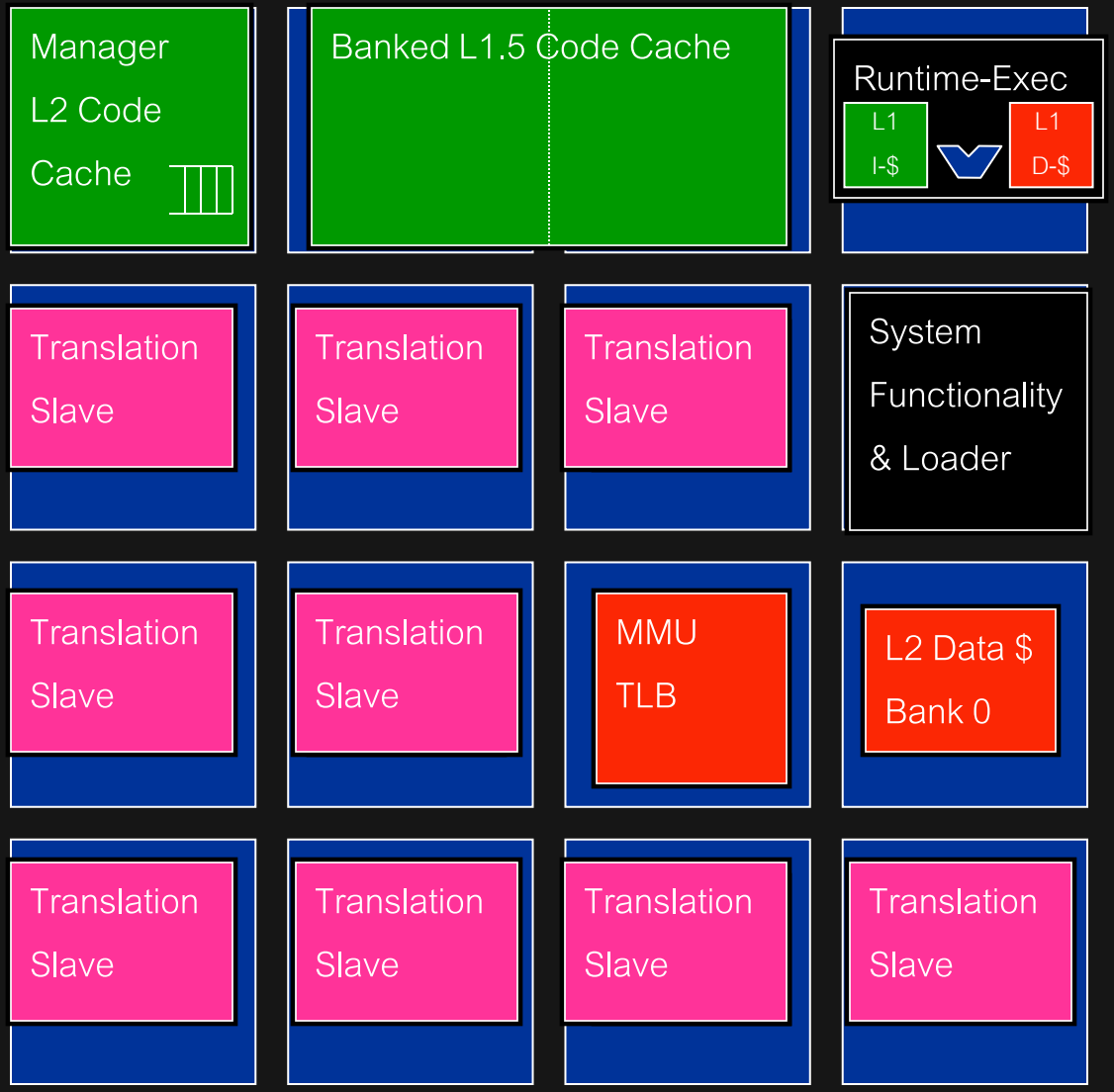
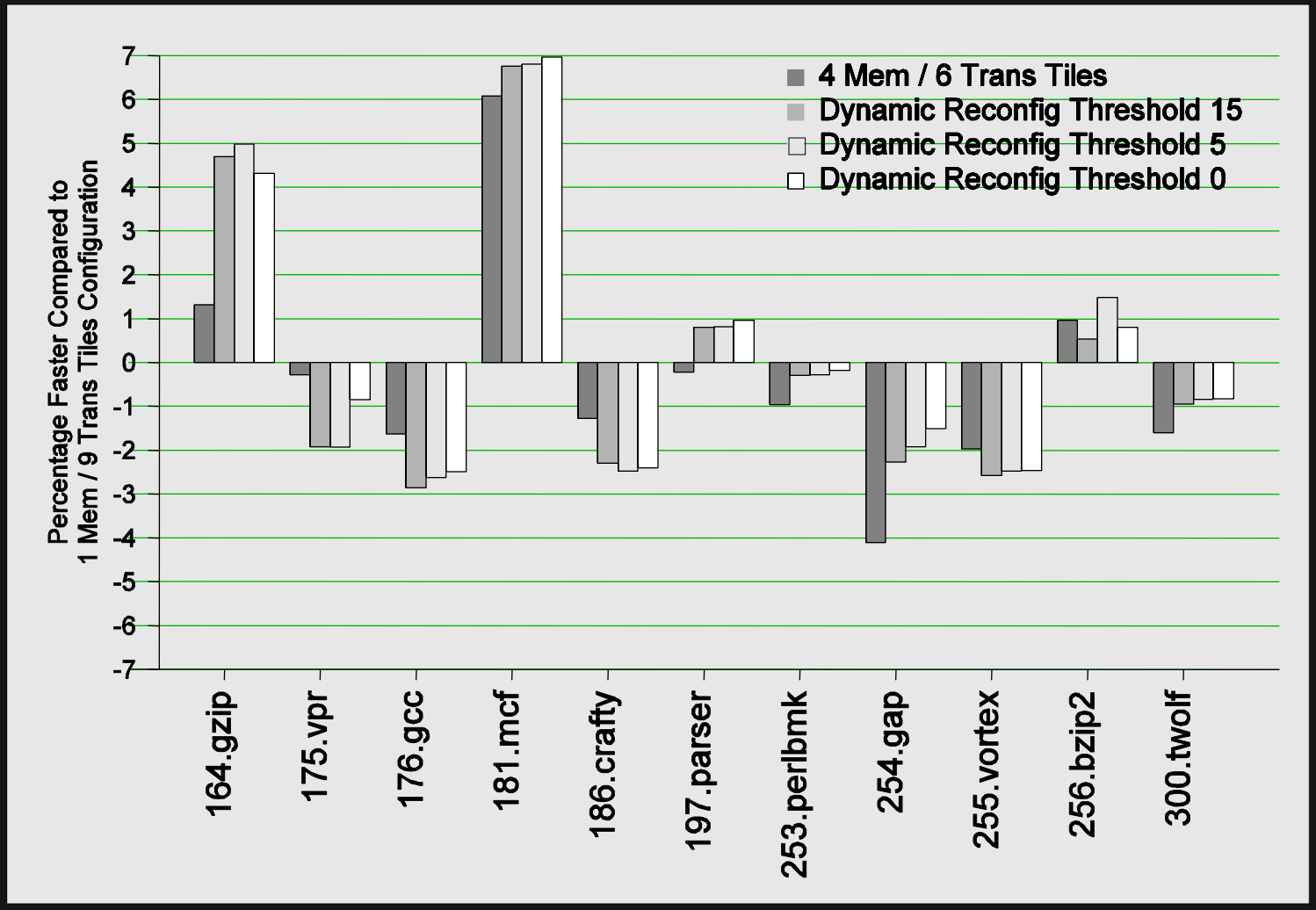
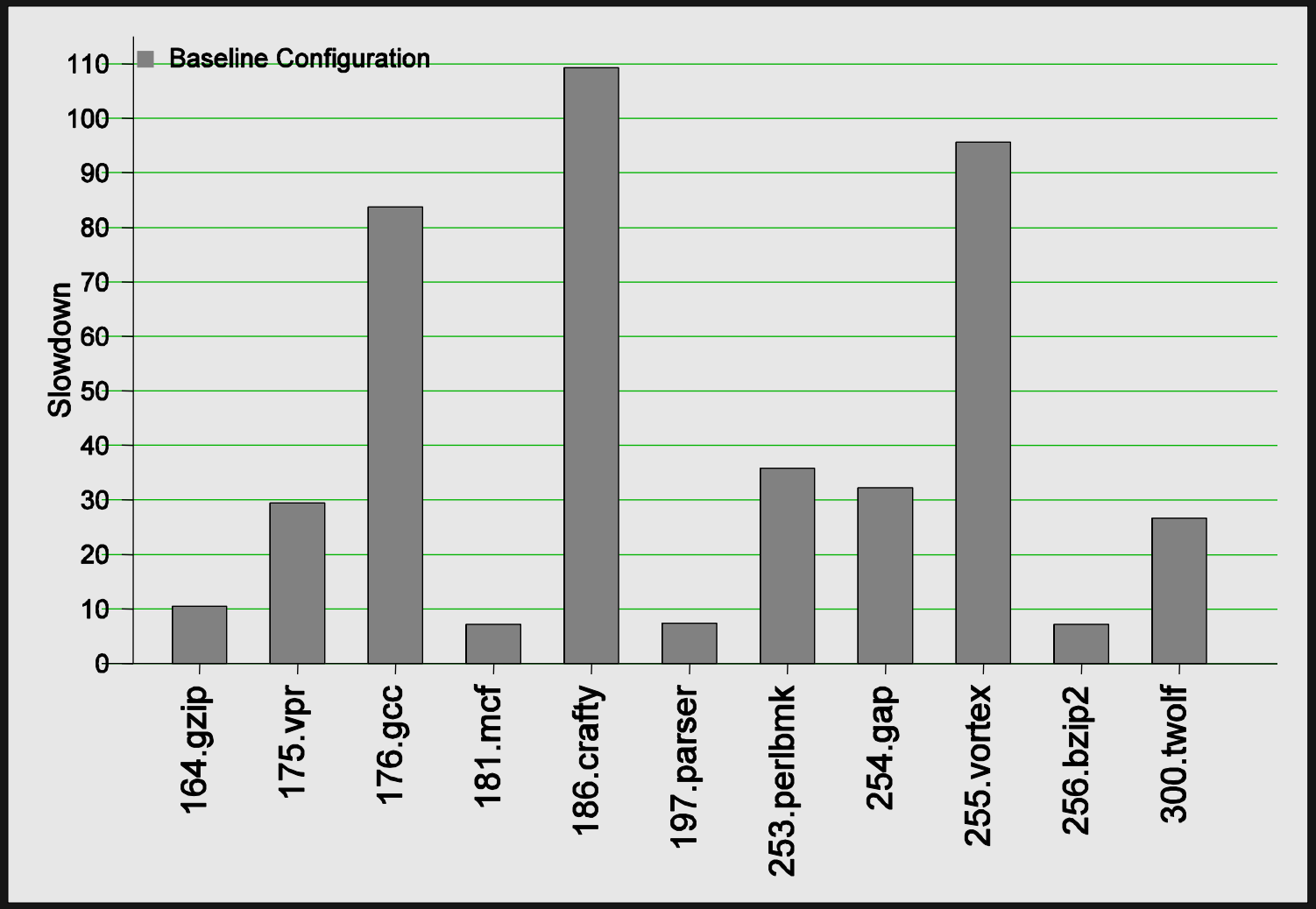


# 3. Reconfiguration Zoom



# Baseline Performance Analysis



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| Intrinsic | Raw Emulator | | Pentium III | |
|---|---|---|---|---|
| | latency | occupancy | latency | occupancy |
| L1 Cache Hit | 6 | 4 | 3 | 1 |
| L2 Cache Hit | 87 | 87 | 7 | 1 |
| L2 Cache Miss | 151 | 87 | 79 | 1 |

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Code Cache Misses 1 – 20x slowdown

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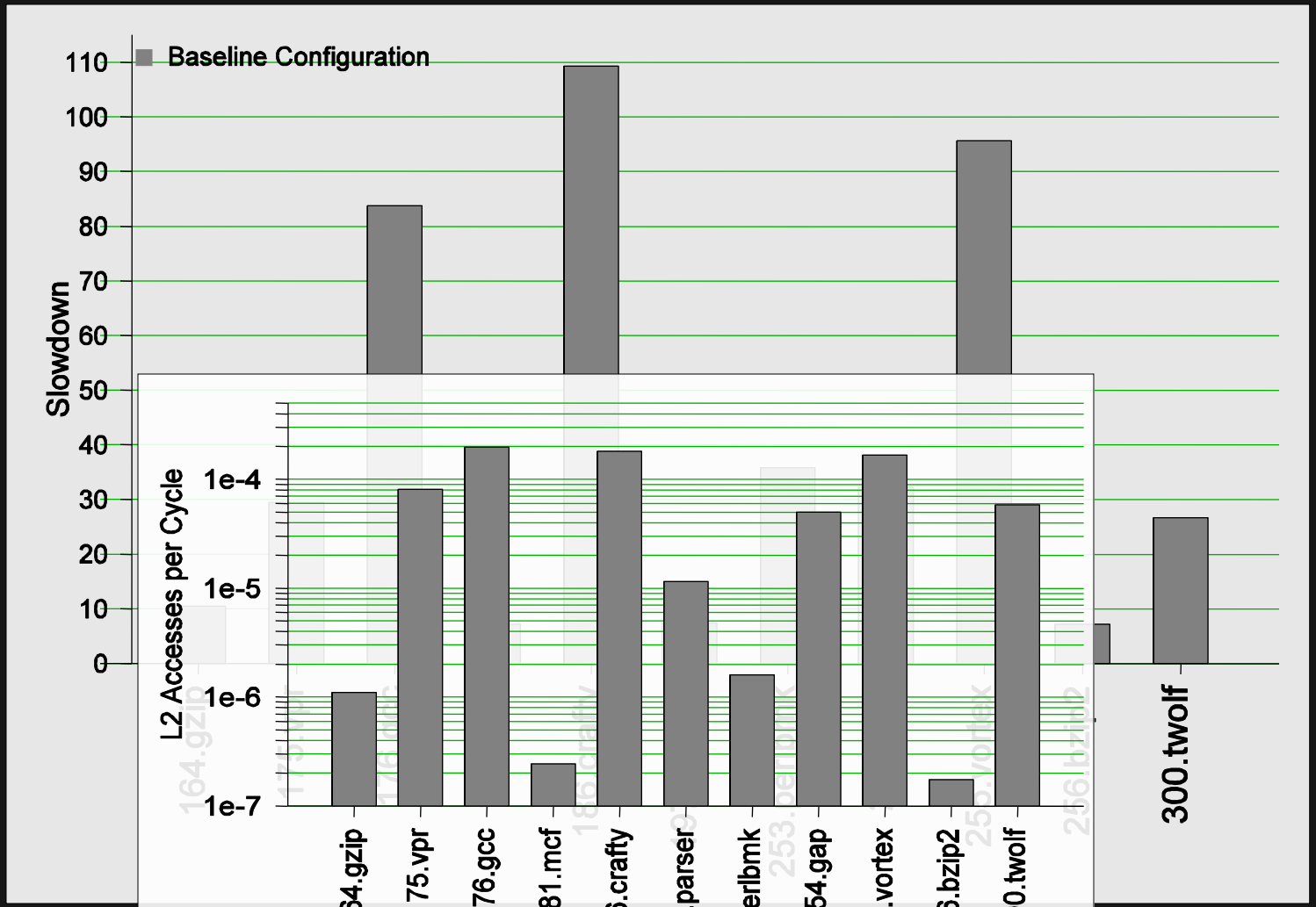

# Future Work

Hardware additions to facilitate parallel emulation

x86 Server farm on a chip

- Inter-Virtual Processor dynamic load balancing

Differing forms of Dynamic Reconfiguration

- Vary number of functional units

# Questions ?

# Extras